MAXIM

CMOS Octal 8-Bit D/A Converter

AD7228

General Description

Maxim's AD7228 contains eight 8-bit voltage output digital-to-analog converters (DACs) with separate input latches and output buffers for simple microprocessor and TTL/CMOS interfacing. The AD7228 maintains 8-bit accuracy over the full operating temperature range without external trimming.

Internally, data transfer into the data registers is via a common 8-bit TTL/CMOS compatible input bus. Logic inputs A2, A1, and A0 control which DAC is loaded after $\overline{WR}$ goes low.

Applications

Minimum Component Count Analog Systems

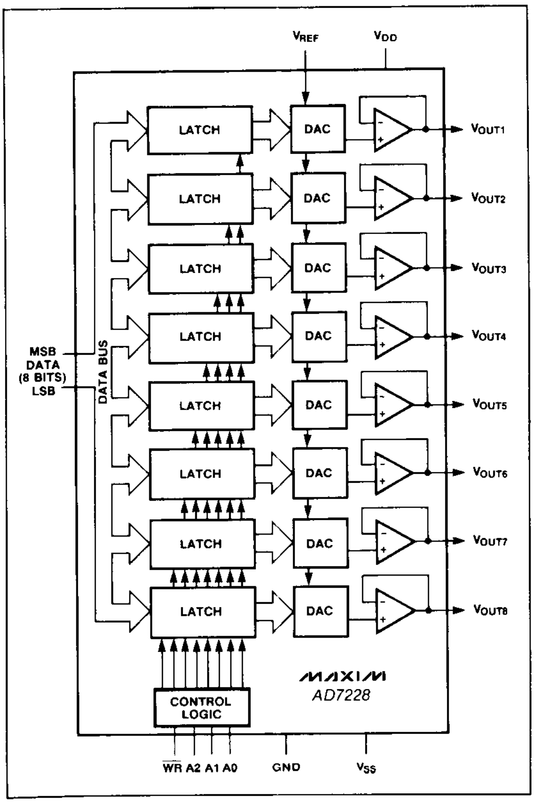
Digital Offset/Gain Adjustment

Industrial Process Control

Arbitrary Function Generators

Automatic Test Equipment

Typical Operating Circuit



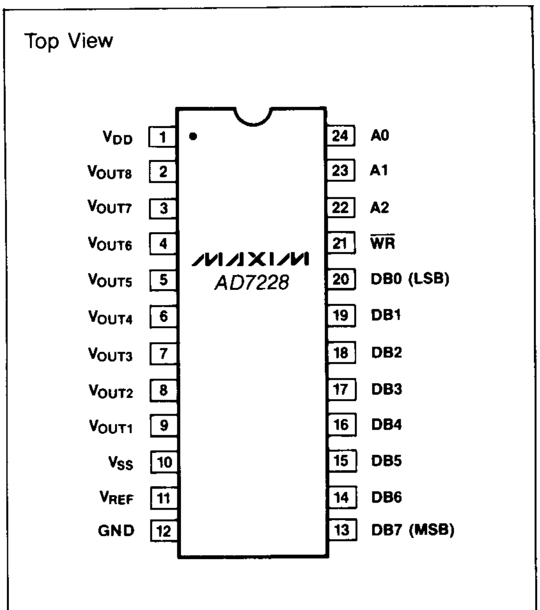
Features

- ◆ Buffered Voltage Output
- ◆ μP Compatible
- ◆ TTL/CMOS Logic Compatible
- ◆ Requires No External Adjustments
- ◆ 24-Pin Narrow DIP Package
- ◆ Operates from Single or Dual Supplies

Ordering Information

PART	TEMP. RANGE	PACKAGE	ERROR
AD7228KN	0°C to +70°C	Plastic DIP	±2 LSB
AD7228LN	0°C to +70°C	Plastic DIP	±1 LSB
AD7228KCWG	0°C to +70°C	Wide SO	±2 LSB
AD7228LCWG	0°C to +70°C	Wide SO	±1 LSB
AD7228K/D	0°C to +70°C	Dice	±2 LSB
AD7228KP	0°C to +70°C	PLCC	±2 LSB
AD7228LP	0°C to +70°C	PLCC	±1 LSB
AD7228BQ	-25°C to +85°C	CERDIP	±2 LSB
AD7228CQ	-25°C to +85°C	CERDIP	±1 LSB
AD7228TQ	-55°C to +125°C	CERDIP	±2 LSB
AD7228UQ	-55°C to +125°C	CERDIP	±1 LSB

Pin Configuration



See page 11 for Plastic Chip Carrier Configuration

CMOS Octal 8-Bit D/A Converter

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .... -0.3V, +17V
V_{DD} to V_{SS} .... -0.3V, +24V
V_{SS} to GND .... -7V, V_{DD}
Digital Input Voltage to GND .... -0.3V, V_{DD}
V_{REF} to GND .... -0.3V, V_{DD}
V_{OUT} to GND (Note 1) .... V_{SS}, V_{DD}
Power Dissipation (Any Package) to +75°C 1000mW
Derating above +75°C .... 12mW/°C

Operating Temperature Ranges
AD7228K, L .... 0°C to +70°C
AD7228B, C .... -25°C to +85°C
AD7228T, U .... -55°C to +125°C
Storage Temperature .... -65°C to +165°C
Lead Temperature (Soldering 10 sec.) .... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supply Operation

(V_{DD} = +10.8V to +16.5V, V_{SS} = -5V ±10%, GND = 0V, V_{REF} = +2V to +10V, R_L = 2k, C_L = 100pF, T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution				8			Bits
Total Unadjusted Error		V_{DD} = 15V ± 10% V_{REF} = 10V	K,B,T L,C,U			±2 ±1	LSB
Relative Accuracy	INL		K,B,T L,C,U			±1 ±1/2	LSB
Differential Nonlinearity	DNL	Guaranteed Monotonic				±1	LSB
Full Scale Error			K,B,T L,C,U			±1 ±1/2	LSB
Full Scale Tempco		V_{REF} = 10V			5		ppm/°C
Zero Code Error		T_A = 25°C	K,B,T L,C,U			±25 ±15	mV
		T_A = T_{MIN} to T_{MAX}	K,B,T L,C,U			±30 ±20	mV
Zero Code Tempco					30		µV/°C
REFERENCE INPUT							
Reference Input Range		(Note 2)		2		10	V
Reference Input Resistance				2			kΩ
Reference Input Capacitance		(Note 3) DAC loaded with 1s				500	pF
AC Feedthrough		(Note 4)			-70		dB
DIGITAL INPUTS							
Input High Voltage	V_{INH}			2.4			V
Input Low Voltage	V_{INL}					0.8	V
Digital Input Leakage Current		V_{IN} = 0V or V_{DD}				±1	µA
Digital Input Capacitance		(Note 3)				8	pF

Note 1: The outputs may be shorted to GND provided that the power dissipation of the package is not exceeded. Typical short circuit current to GND is 25mA.
Note 2: V_{OUT} must be less than V_{DD} by 3.5V to ensure correct operation.
Note 3: Sample tested at +25°C to ensure compliance.
Note 4: V_{REF} = 10kHz, 8V peak-to-peak sine wave.
Note 5: Code transition all 0s to all 1s. V_{REF} = 0V; $\overline{WR}$ = V_{DD}.
Note 6: Code transition all 0s to all 1s. V_{REF} = 10V; $\overline{WR}$ = 0V.

ELECTRICAL CHARACTERISTICS—Dual Supply Operation (Continued)

(V_{DD} = +10.8V to +16.5V, V_{SS} = -5V ±10%, GND = 0V, V_{REF} = +2V to +10V, R_L = 2k, C_L = 100pF, T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (Note 3)							
Voltage Output Slew Rate				2			V/µs
V_{OUT} Settling Time		To ±1/2 LSB, V_{REF} = 10V				5	µs
Digital Feedthrough		(Note 5)			50		nV-sec
Digital Crosstalk		(Note 6)			50		nV-sec
Output Load Resistance		V_{OUT} = 10V		2			kΩ
POWER REQUIREMENTS							
Positive Supply Range	V_{DD}	For specified performance		10.8		16.5	V
Negative Supply Range	V_{SS}	For specified performance		-4.5		-5.5	V
Positive Supply Current (Note 7)	I_{DD}	T_A = 25°C	All			16	mA
		T_A = T_{MIN} to T_{MAX}	K,B,L,C			20	
			T,U			22	
Negative Supply Current (Note 7)	I_{SS}	T_A = 25°C	All			14	mA
		T_A = T_{MIN} to T_{MAX}	K,B,L,C			18	
			T,U			20	
SWITCHING CHARACTERISTICS (Note 3)							
Address to $\overline{WR}$ Setup	t_1			0			ns
Address to $\overline{WR}$ Hold	t_2			0			ns
Data to $\overline{WR}$ Setup	t_3	T_A = 25°C	All	70			ns
		T_A = T_{MIN} to T_{MAX}	K,L,B,C	90			
			T,U	100			
Data to $\overline{WR}$ Hold	t_4			10			ns
$\overline{WR}$ Pulse Width	t_5	T_A = 25°C	All	95			ns
		T_A = T_{MIN} to T_{MAX}	K,L,B,C	120			
			T,U	150			

ELECTRICAL CHARACTERISTICS—Single +15V Supply Operation

(V_{DD} = +15V ±10%, V_{SS} = GND = 0V, V_{REF} = +10V, R_L = 2k, C_L = 100pF, T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution				8			Bits
Total Unadjusted Error			K,B,T			±2	LSB
			L,C,U			±1	
Differential Nonlinearity		Guaranteed Monotonic				±1	LSB
REFERENCE INPUT All specifications are the same as for dual supplies.							
DIGITAL INPUTS All specifications are the same as for dual supplies.							
DYNAMIC PERFORMANCE All specifications are the same as for dual supplies.							
POWER REQUIREMENTS							
Positive Supply Range	V_{DD}	For specified performance		13.5		16.5	V
Positive Supply Current (Note 7)	I_{DD}	T_A = 25°C	All			16	mA
		T_A = T_{MIN} to T_{MAX}	K,B,L,C			20	
			T,U			22	
SWITCHING CHARACTERISTICS All specifications are the same as for dual supplies.							

ELECTRICAL CHARACTERISTICS—+5V Supply Operation

(V_{DD} = +5V ± 5%, V_{SS} = 0 to -5V ±10%, GND = 0V, V_{REF} = +1.25V, R_L = 2k, C_L = 100pF, T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution				8			Bits
Differential Nonlinearity		Guaranteed Monotonic				±1	LSB
Full Scale Error			K,B,T L,C,U			±4 ±2	LSB
Zero Code Error		T_A = 25°C	K,B,T L,C,U			40 30	mV
REFERENCE INPUT							
Reference Input Range		(Note 2)		1.2		1.3	V
Reference Input Resistance				2			kΩ
Reference Input Capacitance		(Note 3) DAC loaded with 1s				500	pF
DIGITAL INPUTS All specifications are the same as for dual supplies.							
DYNAMIC PERFORMANCE All specifications are the same as for dual supplies.							
POWER REQUIREMENTS							
Positive Supply Range	V_{DD}	For Spec Performance		4.75		5.25	V
Positive Supply Current (Note 7)	I_{DD}	T_A = 25°C	All			16	mA
		T_A = T_{MIN} to T_{MAX}	K,B,L,C T,U			20 22	
Negative Supply Current (Note 7)	I_{SS}	T_A = 25°C	All			14	mA
		T_A = T_{MIN} to T_{MAX}	K,B,L,C T,U			18 20	
SWITCHING CHARACTERISTICS (Note 3)							
Address to $\overline{WR}$ Setup	t_1			0			ns
Address to $\overline{WR}$ Hold	t_2			0			ns
Data to $\overline{WR}$ Setup	t_8	T_A = 25°C	All	100			ns
		T_A = T_{MIN} to T_{MAX}	K,L,B,C T,U	140 175			
Data to $\overline{WR}$ Hold	t_4			10			ns
$\overline{WR}$ Pulse Width	t_5	T_A = 25°C	All	125			ns
		T_A = T_{MIN} to T_{MAX}	K,L,B,C T,U	160 200			

Note 1: The outputs may be shorted to GND provided that the power dissipation of the package is not exceeded. Typical short circuit current to GND is 25mA.
Note 2: V_{OUT} must be less than V_{DD} by 3.5V to ensure correct operation.
Note 3: Sample tested at +25°C to ensure compliance.
Note 4: V_{REF} = 10kHz, 8V peak-to-peak sine wave.
Note 5: Code transition all 0s to all 1s. V_{REF} = 0V; $\overline{WR}$ = V_{DD}.
Note 6: Code transition all 0s to all 1s. V_{REF} = 10V; $\overline{WR}$ = 0V.
Note 7: Outputs unloaded.

Digital Inputs and Interface Logic

The digital inputs are compatible with both TTL and 5V CMOS logic, however the power supply current (I_{DD}) is somewhat dependent on input logic level. Supply current is specified for TTL input levels (worst case) but is reduced (by about 450μA) when the logic inputs are driven near GND or greater than 4 volts above GND.

Table 1 shows control logic truth table for $\overline{WR}$, A2, A1, and A0 operation. When $\overline{WR}$ is low, the input latch of the selected DAC is transparent, and the DAC's output responds to the activity on the data bus. The data is latched into the addressed DAC's latch on the rising edge of the $\overline{WR}$ signal. Figure 1 shows the timing diagram for the AD7228.

Table 1. Control Logic Truth Table

$\overline{WR}$	A2	A1	A0	OPERATION
H	X	X	X	No operation Device not selected
L	L	L	L	DAC 1 Transparent
R	L	L	L	DAC 1 Latched
L	L	L	H	DAC 2 Transparent
L	L	H	L	DAC 3 Transparent
L	L	H	H	DAC 4 Transparent
L	H	L	L	DAC 5 Transparent
L	H	L	H	DAC 6 Transparent
L	H	H	L	DAC 7 Transparent
L	H	H	H	DAC 8 Transparent

H = High State, L = Low State, X = Don't Care, R = Rising Edge

Detailed Description

The AD7228 has eight matched voltage output digital-to-analog converters (DACs) The DACs are "inverted" R-2R ladder networks which convert 8 digital bits into equivalent analog output voltages in proportion to the applied reference voltage. All 8 DACs in the AD7228 share the same reference input (V_{REF}) and GND. A simplified circuit diagram of one of the eight DACs is provided in Figure 2.

V_{REF} Input

The voltage at V_{REF} sets the full-scale output of the DACs. The input impedance of the V_{REF} pin is code dependent. The lowest value, approximately 2 kohms, occurs when the input code of all eight DACs is 01010101. The maximum value of infinity occurs when all of the input codes of the eight DACs is 00000000. Because the input resistance at V_{REF} is code dependent, the DACs' reference source should not have an output impedance more than 4 ohms. The capacitance at V_{REF} is also code dependent and typically varies from 120pF to 350pF.

V_{OUT1}, V_{OUT2}, V_{OUT3}, V_{OUT4}, V_{OUT5}, V_{OUT6}, V_{OUT7}, and V_{OUT8} can be represented by a digitally programmable voltage source as:

$$V_{OUT} = Nb \times V_{REF}/256$$

where Nb is the numeric value of the DAC's binary input code.

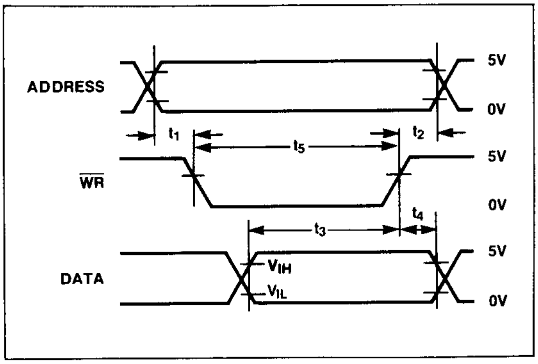


Figure 1. Write Cycle Timing Diagram

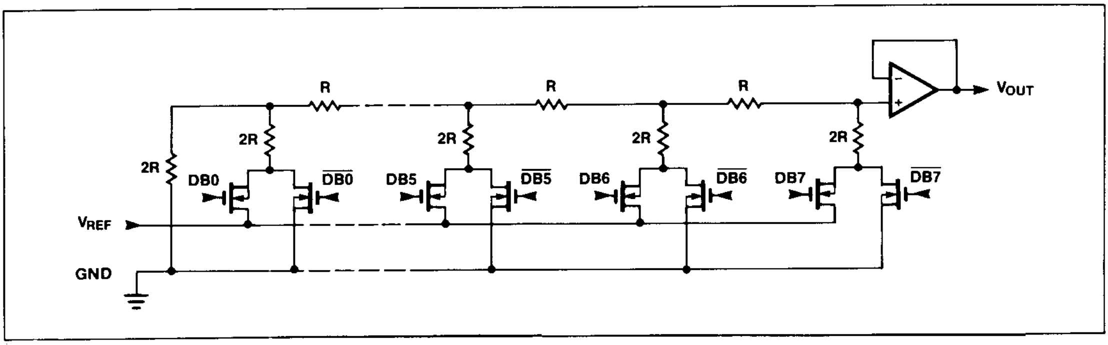


Figure 2. DAC Circuit Diagram

Output Buffer Amplifiers

All voltage outputs are internally buffered by precision unity gain followers which slew at greater than 2V/μs. The output settles to ±1/2 LSB in less than 5μs when driving 2kΩ in parallel with 100pF with a full scale transition (0V to +10V or +10V to 0V) The buffers will also drive 2kΩ in parallel with 500pF to 10V levels without oscillation. Typical dynamic response and settling performance of the AD7228 are shown in Figures 3 and 4.

A simplified circuit diagram of an output buffer is shown in Figure 5. Input common mode range to GND is provided by a PMOS input structure. The output circuitry incorporates both a constant current source and an actively driven n-channel device. The actively driven n-channel device aids in discharging large output capacitances.

The AD7228 can operate from either a single supply or dual supplies. The output buffer amplifiers are the only part of the AD7228 that receive V_{SS} power. Operating the AD7228 from dual supplies will improve the negative going output settling time near GND. In addition, the output amplifier can sink 500μA when operating with dual supplies. The use of dual supplies also extends the input reference voltage range. When operating with a single supply, the output sink current decreases when the output approaches 0 volts (see Figure 6).

The output amplifier broadband noise is approximately $50\mu V_{RMS}$ and is not strongly power supply voltage dependent. The output impedance of the output buffer is approximately 1Ω.

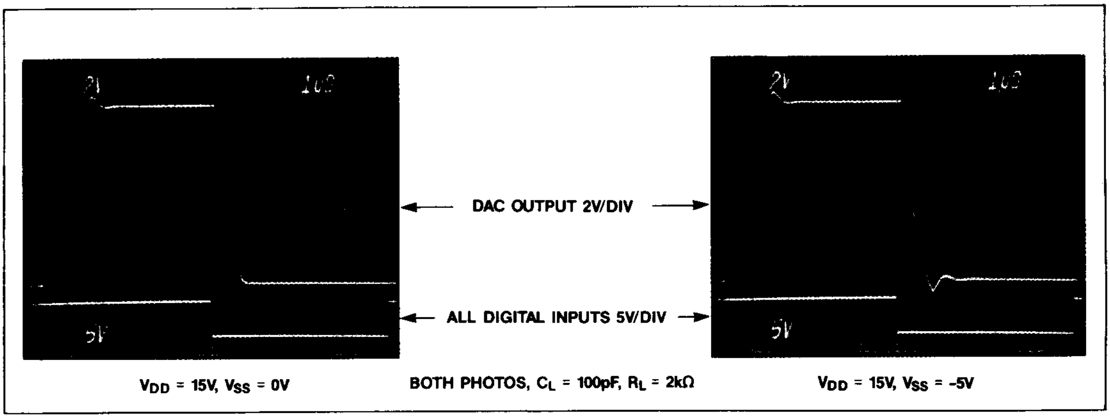


Figure 3. Dynamic Response

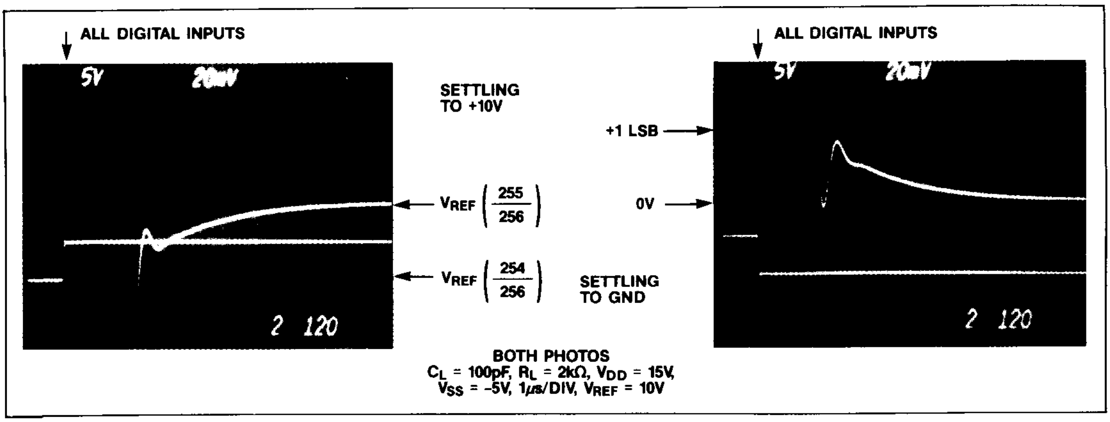


Figure 4. Dynamic Response

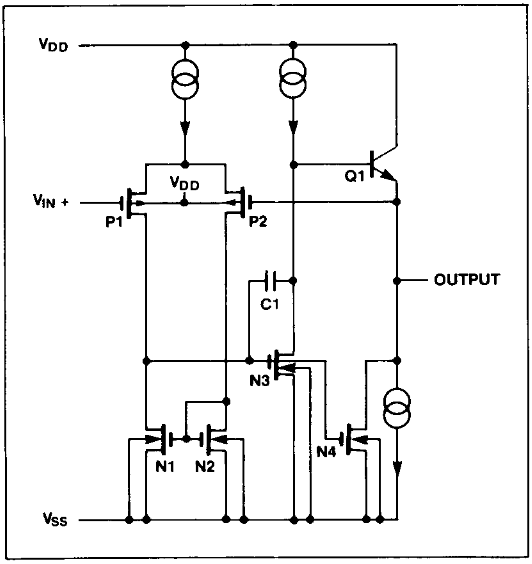


Figure 5. Output Buffer Amplifier

Applications Information

Power Supply and Reference Operating Ranges

The AD7228 is fully specified to operate between +12V ±10% and +15V ±10% (10.8V to 16.5V), and with V_{SS} from 0V to -5.5V. 8 bit performance is guaranteed for single supply operation (V_{SS} = 0V), however, zero code error is improved with V_{SS} = -5V.

For adequate DAC and buffer operation, V_{REF} must always be below V_{DD} by at least 3.5V.

Power Supply Management

Careful PCB layout techniques should be used to minimize crosstalk between V_{REF}, GND, and the digital inputs. This is particularly important if the reference input is driven from an AC source. Bypass capacitors (0.1µF in parallel with 6.8µF) should be used between V_{DD} and GND (also between V_{SS} and GND if V_{SS} is -5V).

Unipolar Output

In unipolar operation, the reference voltage is the same polarity as the output voltage. Since the reference voltage must always be positive with respect to GND, the output voltage is also positive with respect to GND. An example of a unipolar circuit configuration is shown in Figure 7. The unipolar code is given in Table 2.

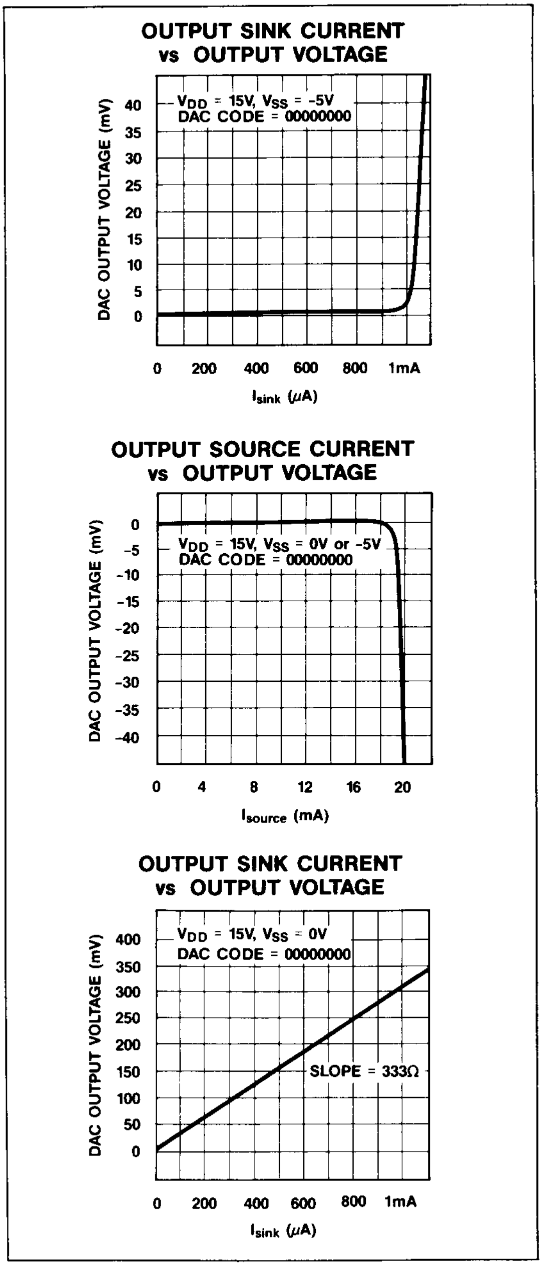


Figure 6. Output Sink/Source Current vs. Output Voltage

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Table 2. Unipolar Code Table

DAC CONTENTS MSB	LSB	ANALOG OUTPUT
1 1 1 1	1 1 1 1	$+V_{REF}\left(\frac{255}{256}\right)$
1 0 0 0	0 0 0 1	$+V_{REF}\left(\frac{129}{256}\right)$
1 0 0 0	0 0 0 0	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0 1 1 1	1 1 1 1	$+V_{REF}\left(\frac{127}{256}\right)$
0 0 0 0	0 0 0 1	$+V_{REF}\left(\frac{1}{256}\right)$
0 0 0 0	0 0 0 0	0V

Note: $1\text{ LSB} = (V_{REF})(2^{-8}) = +V_{REF}\left(\frac{1}{256}\right)$

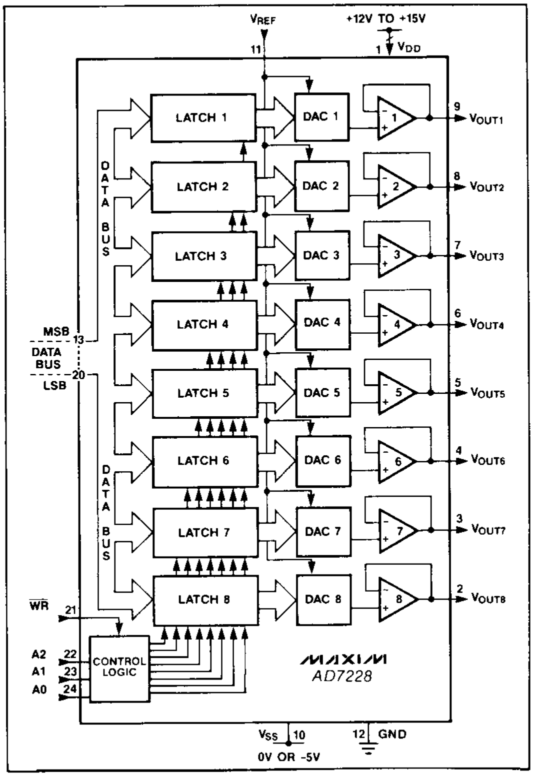

Figure 7. Unipolar Output Circuit

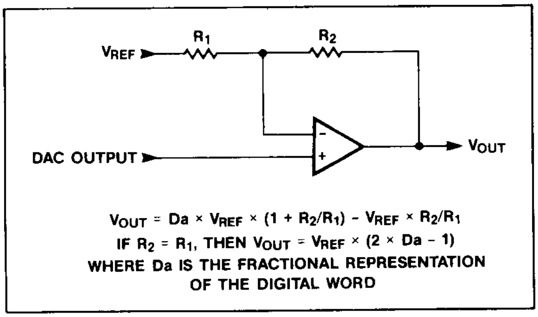

Figure 8. Bipolar Output Circuit

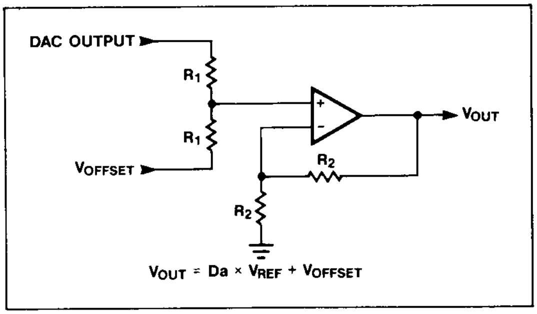

Figure 9. Offset Circuit

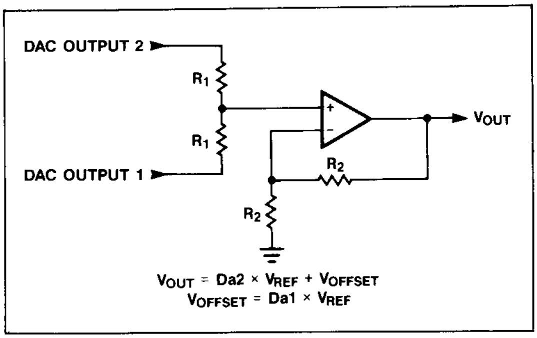

Figure 10. Offset Circuit

Bipolar Output

Each DAC output may be configured for bipolar operation using the circuit in Figure 8. One op amp and two resistors are needed per channel. Table 3 shows the digital code versus output voltage for Figure 8 assuming R1=R2.

Table 3. Bipolar Code Table

DAC CONTENTS MSB	LSB	ANALOG OUTPUT
1 1 1 1	1 1 1 1	$+V_{REF}\left(\frac{127}{128}\right)$
1 0 0 0	0 0 0 1	$+V_{REF}\left(\frac{1}{128}\right)$
1 0 0 0	0 0 0 0	0V
0 1 1 1	1 1 1 1	$-V_{REF}\left(\frac{1}{128}\right)$
0 0 0 0	0 0 0 1	$-V_{REF}\left(\frac{127}{128}\right)$
0 0 0 0	0 0 0 0	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

Offsetting DAC Outputs

Each DAC can be offset using the circuit shown in Figure 9. If the op amp does not have a negative supply, then its common mode voltage range and output voltage range must include GND. Also, one DAC can provide the output offset for another DAC as shown in Figure 10.

Using an AC Reference

In applications where V_{REF} has AC signal components, the AD7228 has multiplying capabilities within the limits of the V_{REF} input range specifications. Figure 11 shows a technique for applying an AC signal to the AD7228. Since all eight DACs share a common reference, they all will be AC modulated. Output distortion is typically less than 0.1% for frequencies up to 50kHz.

Generating V_{SS}

The performance of the AD7228 is specified with and without a V_{SS} supply. When the improved performance of dual supply operation is desired, but only a single supply is available, a negative supply can be generated using any of the circuits shown in Figure 12.

Digital Interface Applications

Figures 13 through 16 shown examples of interfacing the AD7228 to most popular microprocessors.

5V Operation

The AD7228 can also be used with a single 5V power supply or a ± 5V power supply. The timing specifications are degraded, and the reference voltage range is reduced. The DNL of each DAC remains at ± 1 LSB guaranteeing monotonicity. For devices with a negative offset and no negative supply there is a possibility, near zero, that the DAC will not change when the DAC code is incremented. Once the DAC has reached the offset voltage of the output buffer, the DAC will begin to increment in a normal fashion. Since the LSB voltage is only a few millivolts, care should be used in decoupling supplies, ground loops, etc.

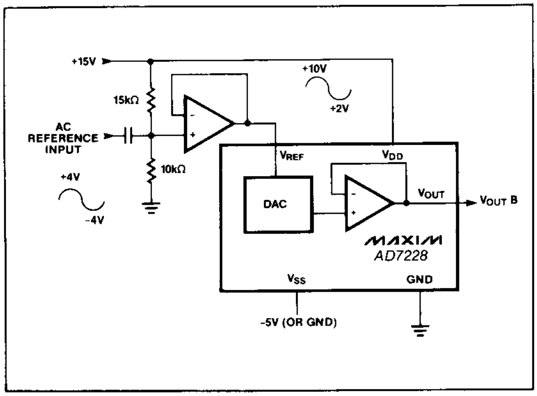

Figure 11. AC Reference Input Circuit

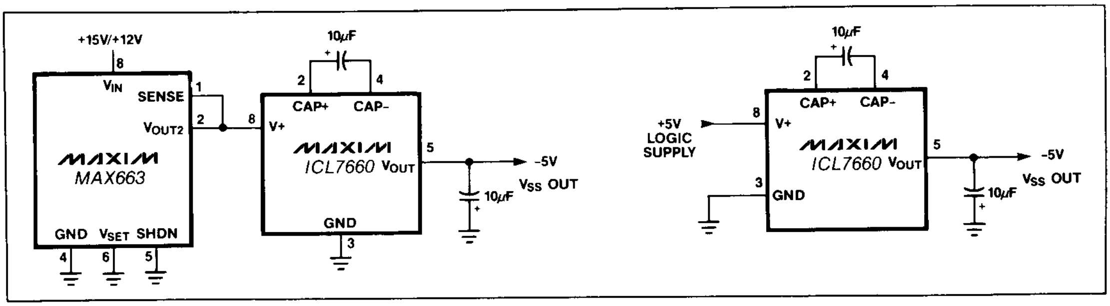

Figure 12. Generating -5V for V_{SS}

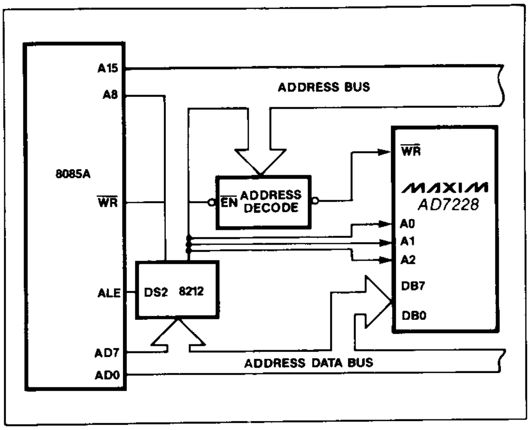

Figure 13. AD7228 to 8085A Interface

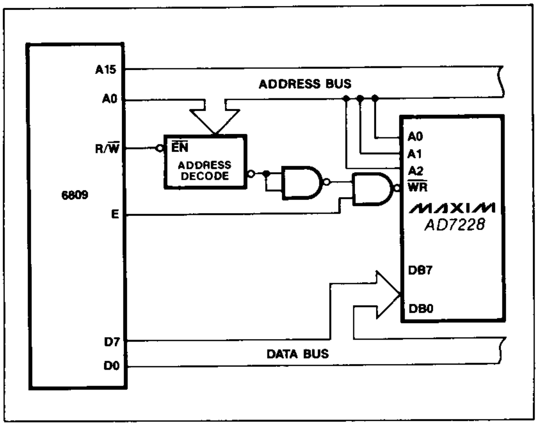

Figure 14. AD7228 to 6809 Interface

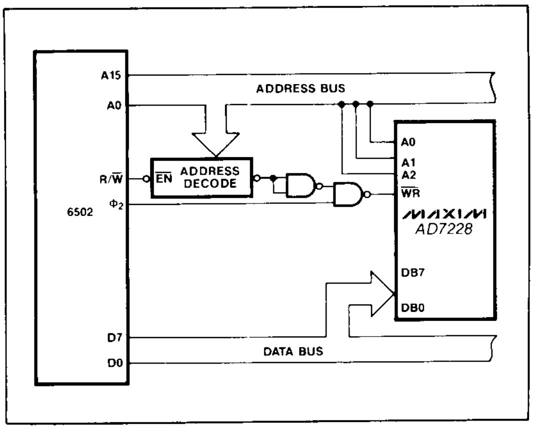

Figure 15. AD7228 to 6502 Interface

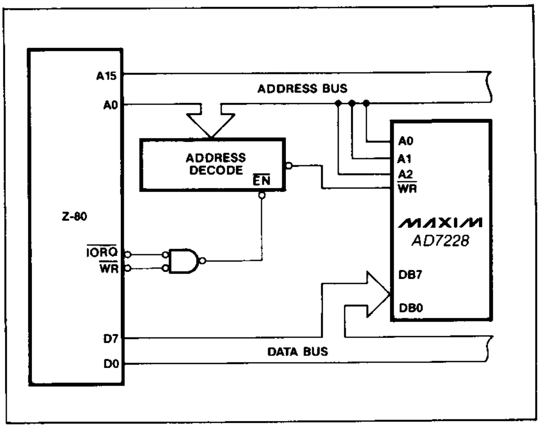

Figure 16. AD7228 to Z-80 Interface

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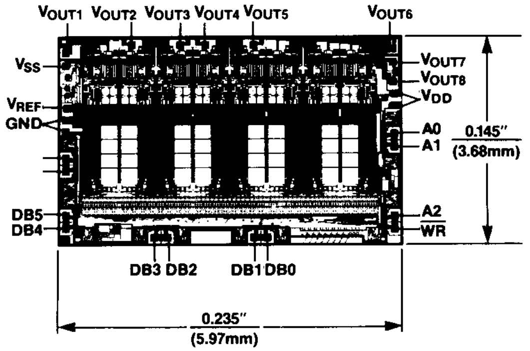
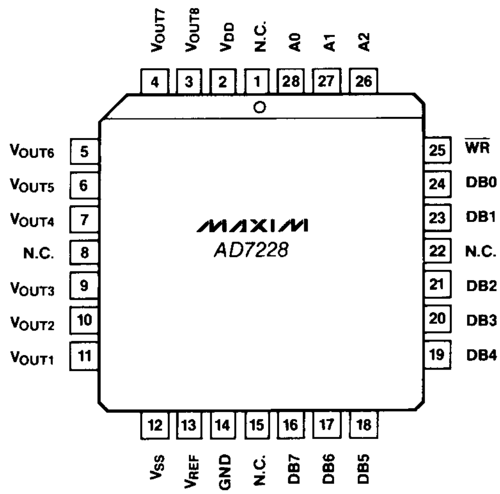
Chip Topography



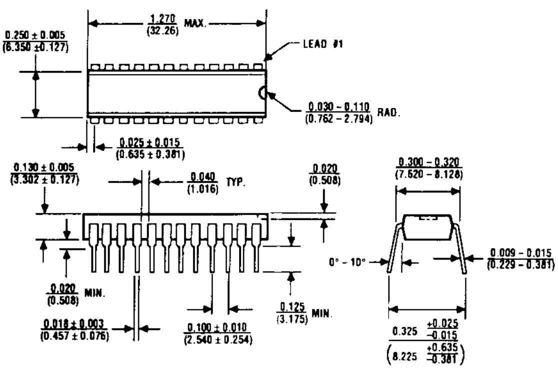
Pin Configuration (continued)

Top View



28 Lead Plastic Chip Carrier (Quad Pak)

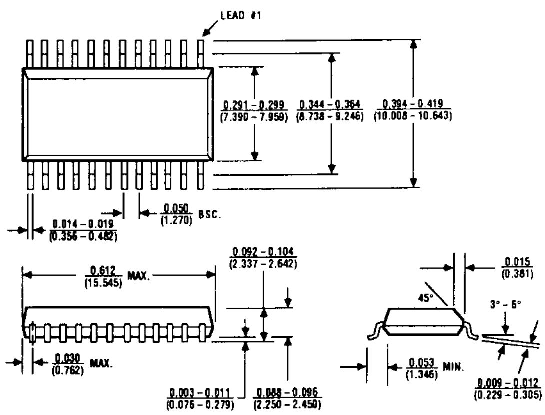
Package Information



24 Lead Plastic Narrow DIP (NG)

θ_{JA} = 120°C/W

θ_{JC} = 60°C/W



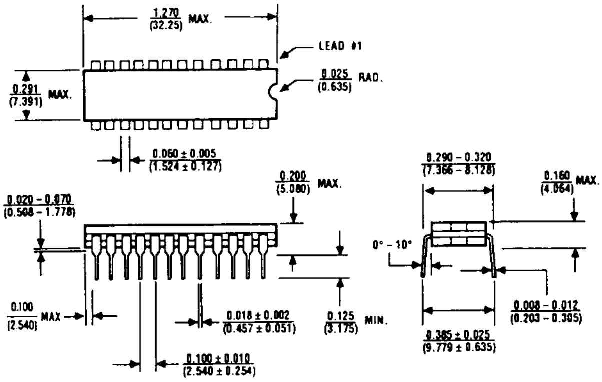
24 Lead Small Outline, Wide (WG)

θ_{JA} = 85°C/W

θ_{JC} = 45° C/W

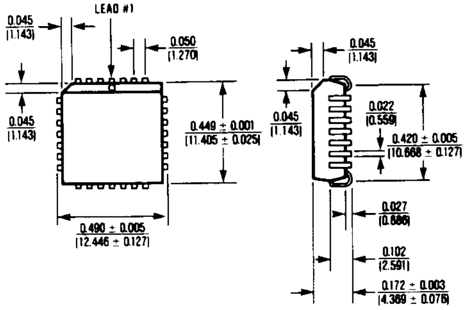
CMOS Octal 8-Bit D/A Converter

Package Information (continued)



24 Lead Narrow CERDIP (RG)

θ_{JA} = 80°C/W
θ_{JC} = 40°C/W



28 Lead Plastic Chip Carrier (Quad Pak) (QI)

θ_{JA} = 100°C/W
θ_{JC} = 45°C/W

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