

PRELIMINARY

July 1995

100V/2A Peak, Low Cost, High Frequency Half-Bridge Driver

Features

- Drives N-Channel MOSFET Half Bridge
- Space Saving SO8 Package
- Bootstrap Supply Max Voltage to 116VDC
- On-Chip 1Ω Bootstrap Diode
- Fast Propagation Times Needed for Multi-MHz Circuits
- Drives 1000pF Load at 1MHz with Rise and Fall Times of Typically 10ns
- CMOS Input Thresholds for Improved Noise Immunity
- Independent Inputs for Non-Half-Bridge Topologies
- No Start-Up Problems
- Outputs Unaffected by Supply Glitches, HS Ringing Below Ground, or HS Slewing at High dv/dt
- Low Power Consumption
- Wide Supply Range
- Supply Undervoltage Protection
- 2Ω Output Resistance

Applications

- Telecom Half-Bridge Power Supplies
- Avionic DC-DC Converters
- Two-Switch Forward Converters
- Active Clamp Forward Converters

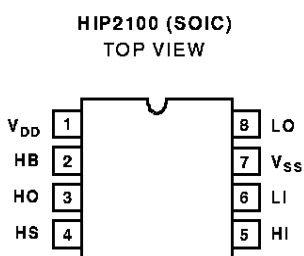
Description

The HIP2100 is a high frequency, 100V Half Bridge N-Channel MOSFET driver IC, available in 8 lead plastic SOIC. The low-side and high-side gate drivers are independently controlled and matched to 5ns. This gives the user maximum flexibility in dead-time selection and driver protocol. Undervoltage protection on both the low-side and high-side supplies force the outputs low. An on-chip diode eliminates the discrete diode required with other driver ICs. A new level-shifter topology yields the low-power benefits of pulsed operation with the safety of DC operation. Unlike some competitors, the high-side output returns to its correct state after a momentary undervoltage of the high-side supply.

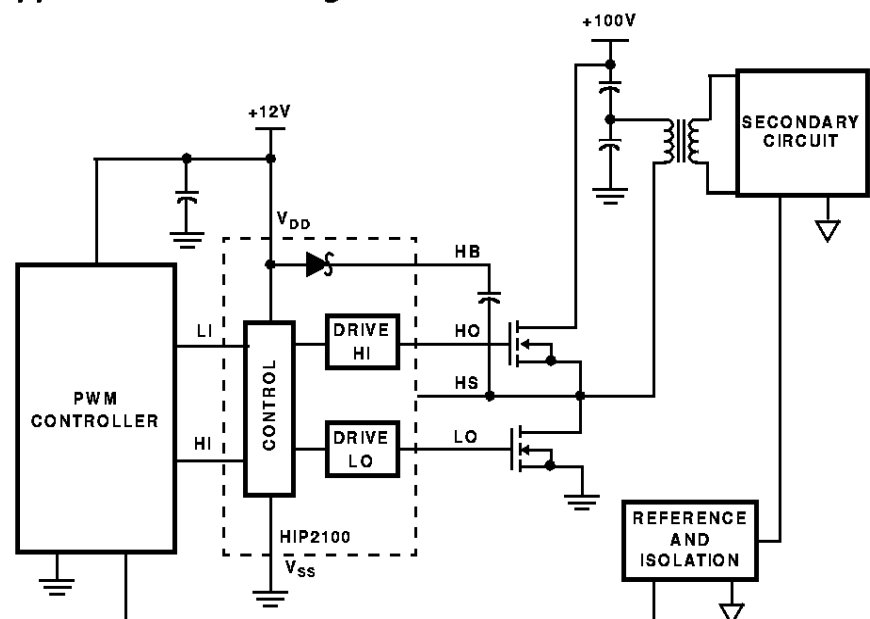
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP2100IB	-40°C to +85°C	8 Lead Plastic SOIC (N)

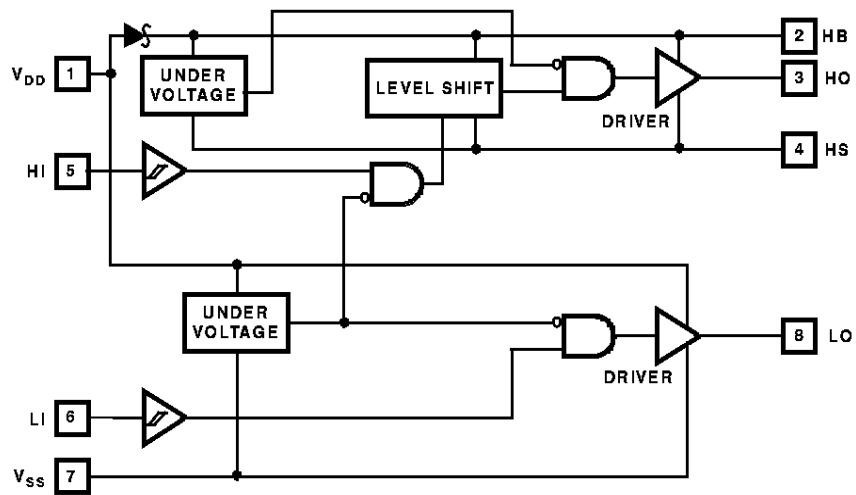
Pinout



Application Block Diagram



Functional Block Diagram



Other Applications

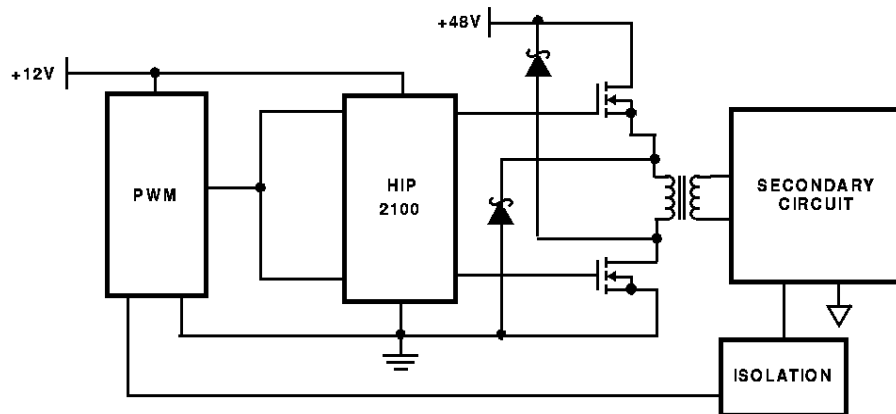


FIGURE 1. TWO-SWITCH FORWARD CONVERTER

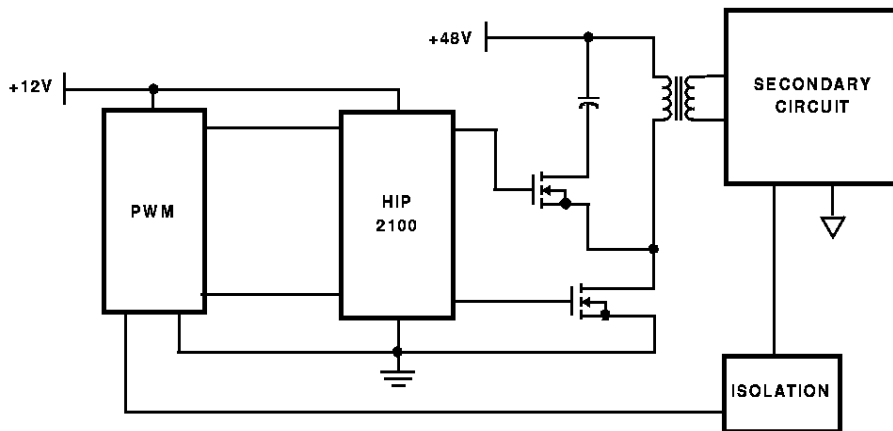


FIGURE 2. FORWARD CONVERTER WITH AN ACTIVE CLAMP

Specifications HIP2100

Absolute Maximum and Thermal Ratings

Supply Voltage, V_{DD} , V_{HB} - V_{HS}	-0.3V to 18V	Thermal Resistance, θ_{JA} 8 Lead SOIC	160°C/W
LI and HI Voltages	-3V to V_{DD} +0.3V	Thermal Resistance, θ_{JC} 8 Lead SOIC in Thermal Conductive Media	70°C/W
Voltage on LO	-0.3V to V_{DD} +0.3V	HS Slew Rate	10V/ns
Voltage on HO	V_{HS} -0.3V to V_{HB} +0.3V	Storage Temperature Range	-65°C to +150°C
Voltage on HS (Continuous)	-1V to 110V	Junction Temperature Range	-55°C to +150°C
Voltage on HB	+118V	Lead Temperature (Soldering 10s - Lead Tips Only)	+300°C
Average Current in V_{DD} to HB diode	100mA	Maximum Power Dissipation at +25°C in Free Air	780mW
NOTE: All Voltages Relative to Pin 4, V_{SS} Unless Otherwise Specified		ESD Classification	Class 1 (1kV)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the recommended operating conditions of this specification is not implied.

Recommended Operating Conditions

Supply Voltage, V_{DD}	+9V to +16.5V	Voltage on HS	(Repetitive Transient) -5V to 105V
Voltage on HS	-1V to 100V	Voltage on HB. V_{HS} +8V to V_{HS} +16.5V and V_{DD} -1V to V_{DD} +100V	

Electrical Specifications $V_{DD} = V_{HB} = 12V$, $V_{SS} = V_{HS} = 0V$, No Load on LO or HO, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	$T_J = 25^\circ C$			$T_J = -40^\circ C$ TO $+125^\circ C$		UNITS
			MIN	TYP	MAX	MIN	MAX	
SUPPLY CURRENTS								
V_{DD} Quiescent Current	I_{DD}	LI = HI = 0V	-	0.1	0.15	-	0.2	mA
V_{DD} Operating Current	I_{DDO}	f = 500kHz	-	1.5	2.5	-	3	mA
Total HB Quiescent Current	I_{HB}	LI = HI = 0V	-	0.1	0.15	-	0.2	mA
Total HB Operating Current	I_{HBO}	f = 500kHz	-	1.5	2.5	-	3	mA
HB to V_{SS} Current, Quiescent	I_{HBS}	$V_{HS} = V_{HB} = 116.5V$	-	0.05	1	-	10	μA
INPUT PINS								
Low Level Input Voltage Threshold	V_{IL}		4	5.4	-	3	-	V
High Level Input Voltage Threshold	V_{IH}		-	5.8	8	-	9	V
Input Voltage Hysteresis	V_{IHYS}		-	0.4	-	-	-	V
Input Pulldown Resistance	R_I		-	200	-	100	500	K Ω
UNDER VOLTAGE PROTECTION								
V_{DD} Rising Threshold	V_{DDR}		7	7.3	8	6.5	8.5	V
V_{DD} Threshold Hysteresis	V_{DDH}		-	0.5	-	-	-	V
HB Rising Threshold	V_{HBR}		6.5	6.9	7.5	6	8	V
HB Threshold Hysteresis	V_{HBBH}		-	0.4	-	-	-	V
BOOT STRAP DIODE								
Low-Current Forward Voltage	V_{DL}	$I_{VDD-HB} = 100\mu A$	-	0.45	0.55	-	0.7	V
High-Current Forward Voltage	V_{DH}	$I_{VDD-HB} = 100mA$	-	0.7	0.8	-	1	V
Dynamic Resistance	R_D	$I_{VDD-HB} = 100mA$	-	0.8	1	-	1.5	Ω
LO GATE DRIVER								
Low Level Output Voltage	V_{OLL}	$I_{LO} = 100mA$	-	0.25	0.3	-	0.4	V
High Level Output Voltage	V_{OHL}	$I_{LO} = -100mA$, $V_{OHL} = V_{DD} - V_{LO}$	-	0.25	0.3	-	0.4	V
Peak Pullup Current	I_{OHL}	$V_{LO} = 0V$	-	2	-	-	-	A
Peak Pulldown Current	I_{OLL}	$V_{LO} = 12V$	-	2	-	-	-	A
HO GATE DRIVER								
Low Level Output Voltage	V_{OLH}	$I_{HO} = 100mA$	-	0.25	0.3	-	0.4	V
High Level Output Voltage	V_{OHH}	$I_{HO} = -100mA$, $V_{OHH} = V_{HB} - V_{HO}$	-	0.25	0.3	-	0.4	V
Peak Pullup Current	I_{OHH}	$V_{HO} = 0V$	-	2	-	-	-	A
Peak Pulldown Current	I_{OLH}	$V_{HO} = 12V$	-	2	-	-	-	A

Specifications HIP2100

Switching Specifications $V_{DD} = V_{HB} = 12V$, $V_{SS} = V_{HS} = 0V$, No Load on LO or HO, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	$T_J = 25^\circ C$			$T_J = -40^\circ C$ TO $+125^\circ C$		UNITS
			MIN	TYP	MAX	MIN	MAX	
Lower Turn-Off Propagation Delay (LI Falling to LO Falling)	t_{LPHL}		-	20	35	-	45	ns
Upper Turn-Off Propagation Delay (HI Falling to HO Falling)	t_{HPHL}		-	20	35	-	45	ns
Lower Turn-On Propagation Delay (LI Rising to LO Rising)	t_{LPLH}		-	20	35	-	45	ns
Upper Turn-On Propagation Delay (HI Rising to HO Rising)	t_{HPLH}		-	20	35	-	45	ns
Delay Matching: Lower Turn-On and Upper Turn-Off	t_{MON}		-	2	8	-	10	ns
Delay Matching: Lower Turn-Off and Upper Turn-On	t_{MOFF}		-	2	8	-	10	ns
Either Output Rise/Fall Time	t_{RC}, t_{FC}	$C_L = 1000pF$	-	10	-	-	-	ns
Either Output Rise/Fall Time (3V to 9V)	t_R, t_F	$C_L = 0.1\mu F$	-	0.5	0.6	-	0.8	us
Either Output Rise Time Driving DMOS	t_{RD}	$C_L = IRFR120$	-	20	-	-	-	ns
Either Output Fall Time Driving DMOS	t_{FD}	$C_L = IRFR120$	-	10	-	-	-	ns
Minimum Input Pulse Width that Changes the Output	t_{PW}		-	-	-	-	50	ns
Bootstrap Diode Turn-On or Turn-Off Time	t_{BS}		-	10	-	-	-	ns

Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	V_{DD}	Positive Supply to lower gate drivers. De-couple this pin to V_{SS} (Pin 7). Bootstrap diode connected to HB (pin 2).
2	HB	High-Side Bootstrap supply. External bootstrap capacitor is required. Connect positive side of bootstrap capacitor to this pin. Bootstrap diode is on-chip.
3	HO	High-Side Output. Connect to gate of High-Side power MOSFET.
4	HS	High-Side Source connection. Connect to source of High-Side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
5	HI	High-Side input.
6	LI	Low-Side input.
7	V_{SS}	Chip negative supply, generally will be ground.
8	LO	Low-Side Output. Connect to gate of Low-Side power MOSFET.

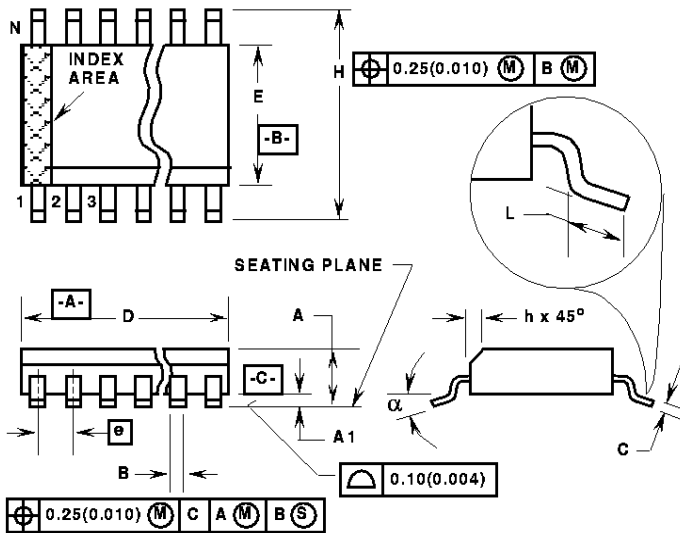
Timing Diagrams

FIGURE 3. TBD

FIGURE 4. TBD

FIGURE 5. TBD

Small Outline Plastic Packages (SOIC)



**M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
alpha	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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