

AN6856

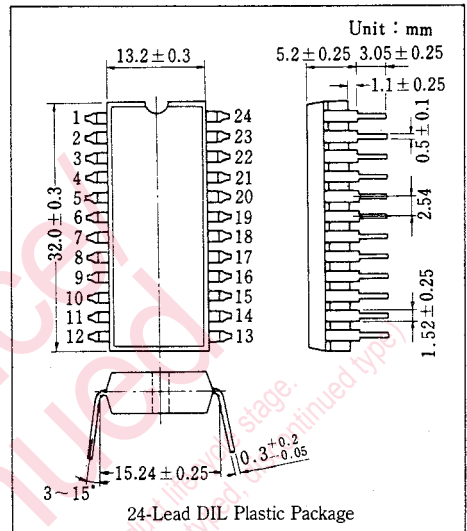
High Speed 6-bit AD Converter

Outline

The AN6856 is an A/D-converting parallel 6-bit monolithic bipolar IC with a high speed and low power consumption. It is suitable for high-speed data conversion such as video band signal digitizing, etc., and computer input data conversion.

Features

- 6-bit resolution (with overflow)
- High speed : maximum conversion speed 35 MSPS
- Sample & hold circuits are not necessary
- Input dynamic range is $2V_{P-P}$
- Low power dissipation : 250mW typ.
- Digital inputs and outputs are ECL compatible
- 6-bit parallel output (Pure binary)



Quick Reference Data ($V_{EE} = -5.2V$, $T_a = 0 \sim 70^\circ C$)

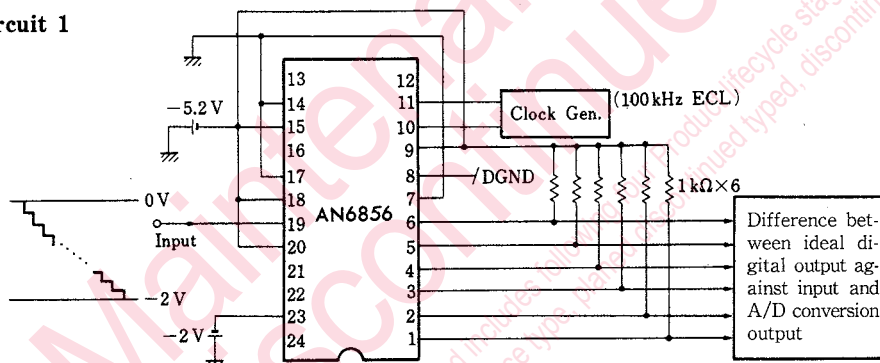
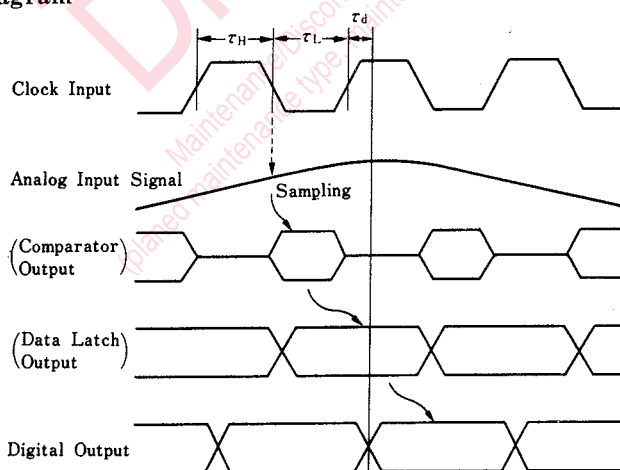
Item	Symbol	Condition	Value	Unit
Resolution	RES		6	bit
Input dynamic range	$V_{i(max.)}$		2	V
Linearity error	LE	$V_{IN} = 2V_{P-P}$	$\pm \frac{1}{2}$	LSB
Max. conversion speed	$f_{MSPS(max.)}$		35	MSPS

Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	1st bit (MSB)	13	Output Inversion
2	2nd bit	14	Ref. High Level
3	3rd bit	15	V_{EE}
4	4th bit	16	NC
5	5th bit	17	Analog GND
6	6th bit (LSB)	18	V_{EE}
7	Analog GND	19	Analog Input
8	Digital GND	20	V_{EE}
9	V_{EE}	21	NC
10	Clock Input (positive)	22	NC
11	Clock Input (Negative)	23	Ref. Low Level
12	Clock Output	24	Over Flow Output

■ Electrical Characteristics ($V_{EE} = -5.2V$, $T_a = 25^\circ C$)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Supply current	I_{EE}		$V_{EE} = -5.2V$		45	65	mA
Reference resistance current	$I_{Bias(RT)}$		$V_{RT} = 0V$		12.5	20	mA
	$I_{Bias(RB)}$		$V_{RB} = -2V$		-12.5	-20	mA
Equivalent input impedance	R_i		$V_{EE} = -5.2V$	40			k Ω
Input capacitance *1	C_i		Total of V_{IN}		25	40	pF
Input bias current *1	I_{Bias}		$V_{EE} = -5.2V$		45	90	μA
Clock input current	$I_{\phi H}$		I_{36} when $V_{36} = 0V$, I_{37} when $V_{37} = 0V$			+0.6	mA
	$I_{\phi L}$		I_{36} when $V_{36} = -5.2V$, I_{37} when $V_{37} = -5.2V$	-0.01			mA
Digital output voltage	V_{OH}		$V_{EE} = -5.2V$, $I_{OH} = -2mA$	-0.96			V
	V_{OL}		$V_{EE} = -5.2V$, $I_{OH} = -2mA$			-1.65	V
Digital output delay time	τ_d				10	15	ns
Linearity error	LE	1				$\pm \frac{1}{2}$	LSB

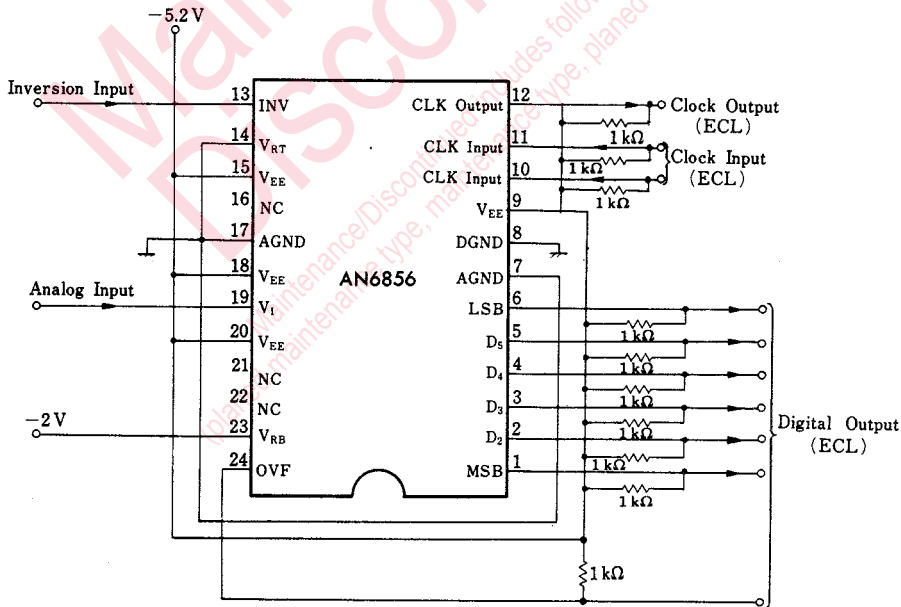
■ Test Circuit 1

■ Sampling Diagram


Note) There are no external terminals for comparator output and data latch output, because they are internal signals.

■ Output Cord Table

Comparator No.	Comparator Threshold Voltage		Digital Output													
	Input 2.0000 V FS 31.250 mV _{STEP}	Input 1920 mV FS 30 mV _{STEP}	INV. terminal "L" Over M Flow					INV. terminal "H" Over M Flow								
			1	2	3	4	5	6	1	2	3	4	5	6		
001	-0.0312V	-0.0300V	0	0	0	0	0	0	1	1	1	1	1	1		
002	-0.0625	-0.0600	0	0	0	0	0	1	1	1	1	1	1	0		
⋮	⋮	⋮	0	0	0	0	0	1	0	1	1	1	1	0	1	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		
031	-0.9687	-0.9300	0	0	1	1	1	1	0	1	1	0	0	0	0	1
032	-1.0000	-0.9600	0	0	1	1	1	1	1	1	1	0	0	0	0	0
033	-1.0312	-0.9900	0	1	0	0	0	0	0	1	0	1	1	1	1	1
⋮	⋮	⋮	0	1	0	0	0	0	1	1	0	1	1	1	1	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
063	-1.9687	-1.8900	0	1	1	1	1	1	0	1	0	0	0	0	0	1
064	-2.0000	-1.9200	0	1	1	1	1	1	1	1	0	0	0	0	0	0
			1	1	1	1	1	1	1	0	0	0	0	0	0	0

■ External Connection Diagram



Note) Separate Analog GND and Digital GND from each other on the printed circuit board as much as possible.

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