



Mosaic  
Semiconductor  
Inc.

**PUMA 2U1000**

**PUMA 2U1000-12/15/17/20**

Issue 1.1 : February 1990

**ADVANCE PRODUCT INFORMATION**

1,048,576 bit CMOS High Speed UV EPROM

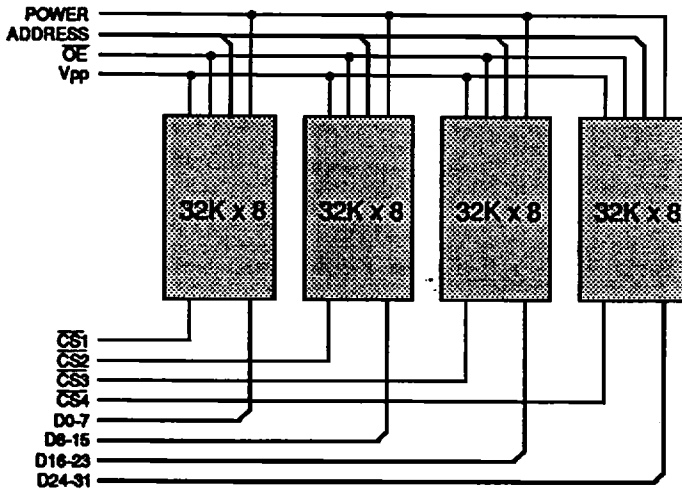
**Features**

- User Configurable as 8,16 or 32 bit wide.
- Very Fast access times of 120/150/170/200 nS.
- Operating Power 800mW (typ), 32 bit mode.  
430mW (typ), 16 bit mode.  
245mW (typ), 8 bit mode.
- Low Power Standby 4mW (typ).

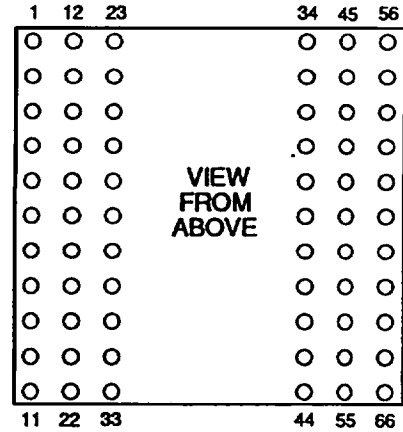
V<sub>PP</sub> Program Voltage of 12.5V.

- Pin grid array gives 2:1 improvement over DIL.
- Package Suitable for Thermal Ladder Applications.
- On board decoupling capacitors.
- May be screened as BS9400 & MIL-STD-883C.

**Block Diagram**



**Pin Definition**

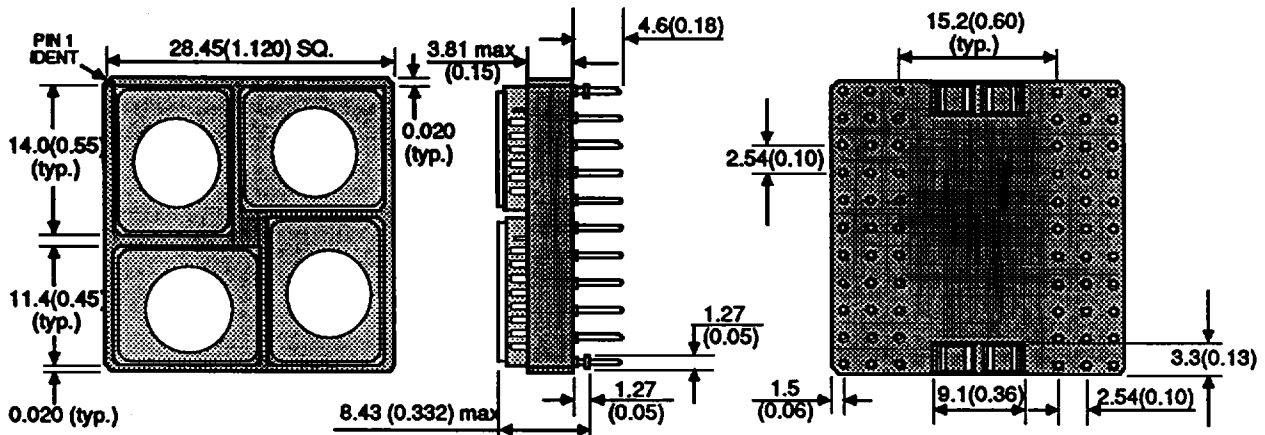


For pinout see page 7

**Pin Functions**

- A0-14 Address Inputs
- D0-D32 Data Inputs/Outputs
- CS1-4 Chip Select
- OE Output Enable
- NC No Connect
- V<sub>CC</sub> Power (+5V)
- V<sub>PP</sub> Programming Voltage
- GND Ground

**Package Details** Dimensions in mm (inches).



**Absolute Maximum Ratings <sup>(1)</sup>**

Supply Voltage <sup>(2)</sup>	$V_{CC}$	-0.6 to +7	V
Programming Voltage	$V_{PP}$	-0.6 to +14	V
Input Voltage <sup>(2),(3)</sup>	$V_{IN}$	-0.6 to +7	V
Operating Temperature	$T_{OPR}$	-60 to +140	°C
Storage Temperature	$T_{STG}$	-65 to +150	°C

- Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.  
 (2) Pulse Width: -2.0V for less than 20ns.  
 (3) With Respect to GND.

**Recommended Operating Conditions**

		<i>min</i>	<i>typ</i>	<i>max</i>	
DC Logic Supply Voltage	$V_{CC}$	4.75	5.0	6.3	V
DC EPROM Program Voltage	$V_{PP}$	12.2	-	12.5	V
Input High Voltage	$V_{IH}$	2.0	-	$V_{CC}+1$	V
Input Low Voltage	$V_{IL}$	0.3	-	0.8	V
Operating Temperature <sup>(1)</sup>	$T_A$	0	-	70	°C
	$T_{AI}$	-40	-	85	°C (1000I)
	$T_{AM}$	-55	-	125	°C (1000M,1000MB)

- Note: (1) Programming would normally take place at 25°C  
 (2) When programming a 0.1µF high frequency by-pass capacitor is required across  $V_{PP}$  and GND to suppress noise transients

**Operating Modes**

The Table below show the logic inputs required to control the operating modes of each EPROM on the PUMA2U1000.

Mode	$\overline{CS}$	$\overline{OE}$	$V_{pp}$	$V_{cc}$	Outputs
Read	0	0	5V	5V	Data out
Output Disable	0	1	5V	5V	Floating
Standby	1	X	5V	5V	Floating
Program	0	1	12.5V	6V	Data in
Program Verify <sup>(1)</sup>	X	0	12.5V	6V	Data out
Optional Prog. Verify	0	0	12.5V	6V	Data out
Program Inhibit	1	1	12.5V	6V	Floating

- 1 =  $V_{IH}$   
 0 =  $V_{IL}$   
 X =  $V_{IH}$  or  $V_{IL}$

Note (1) 32 bit mode only.  
 See page 6

**Device Identifier Mode**

The Identifier Mode allows the reading out of binary codes, which identify manufacturer and type of device, from the outputs of each EPROM. By this mode, the device can be automatically matched to the correct programming algorithm using a suitable EPROM Programmer. The table below shows the outputs of a single EPROM with the PUMA 2U1000 in 8 bit Mode.

PINS	A9	A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX DATA
IDENTIFIER											
Manufacturer Code	12.0V	$V_H$	0	0	1	0	1	0	0	1	29
Device Code		$V_H$	1	0	0	0	1	1	0	0	8C

- Notes (1) A1 - A8, A10 - A14,  $\overline{CS1}$  and  $\overline{OE}$  are all held at  $V_{IL}$

### READ OPERATION

#### DC Electrical Characteristics ( $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_{CC} = 5V \pm 5\%$ )

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	$I_{IN1}$	$V_{IN} = 5.25V$ , Address & $\overline{OE}$	-	-	40	$\mu\text{A}$
	$I_{IN2}$	$\overline{CE1} - \overline{CE4}$	-	-	10	$\mu\text{A}$
Output Leakage Current	$I_{OUT}$	$V_{OUT} = 5.25V/0.45V$	-	-	40	$\mu\text{A}$
$V_{PP}$ Leakage Current	$I_{PP}$	$V_{PP} = 5.5V$	-	-	40	$\mu\text{A}$
Standby Power	$I_{SB1}$	$\overline{CS} = V_{IH}$	-	-	12	mA
Supply Current	$I_{sb2}$	$\overline{CS} = V_{CC} \pm 0.3V$ , $I_{OUT} = 0\text{mA}$	-	-	800	$\mu\text{A}$
Operating Power	$I_{CC}$	$f = 5\text{MHz}$ , $I_{OUT} = 0\text{mA}$ (3)	49	86	160	mA
Supply Current						
Input Low Voltage	$V_{IL}$	Note (1)	-0.6	-	0.8	V
Input High Voltage	$V_{IH}$	Note (2)	2.0	-	$V_{CC} + 1$	V
Output Low Voltage	$V_{OL}$	$I_{OL} = 2.1\text{mA}$	-	-	0.45	V
Output High Voltage	$V_{OH}$	$I_{OH} = -400\mu\text{A}$	2.4	-	-	V

Notes (1) -1.0V for pulse width  $\leq 50$  ns  
 (2)  $V_{CC} + 1.5V$  for pulse width  $\leq 20$  ns. If  $V_{IH}$  is over the specified max. value, READ operation cannot be guaranteed.  
 (3) For these currents min, typ and max values are given for 8, 16 and 32 bit mode operation respectively. Values are min.

#### Capacitance ( $T_A = 25^\circ\text{C}$ , $f = 1\text{MHz}$ )

Parameter	Symbol	Test Condition	typ	max	Unit
Input Capacitance:	$C_{IN}$	$V_{IN} = 0V$ , 8 bit mode	16	24	pF
Output Capacitance:	$C_{OUT}$	$V_{OUT} = 0V$ , 8 bit mode	32	48	pF

Note: Capacitance calculated not measured.

#### AC Characteristics

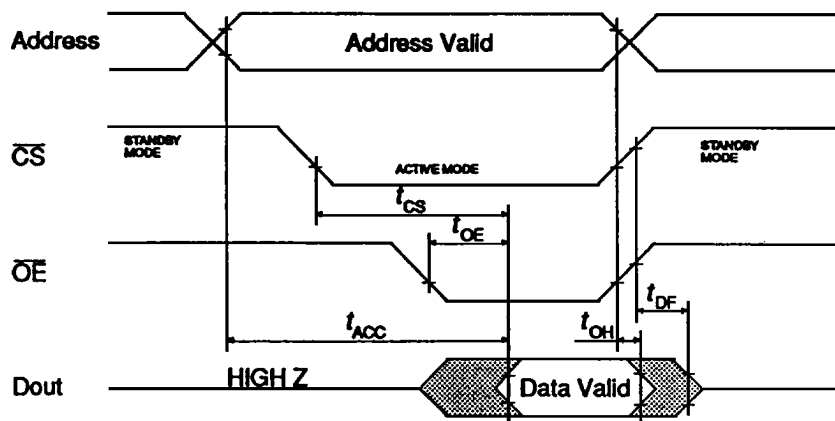
Parameter	Symbol	-12		-15		-17		-20		Unit
		min	max	min	max	min	max	min	max	
Address to Output Delay	$t_{ACC}$	-	120	-	150	-	170	-	200	ns
$\overline{CS}$ to Output Delay	$t_{CS}$	-	120	-	150	-	170	-	200	ns
$\overline{OE}$ to Output Delay	$t_{OE}$	-	60	-	70	-	70	-	75	ns
$\overline{OE}$ or $\overline{CS}$ High to Output Float	$t_{DF}$	-	45	-	50	-	50	-	55	ns
Output Hold from Address, $\overline{CS}$ or $\overline{OE}$	$t_{OH}$	-	0	-	0	-	0	-	0	ns

NOTE :  $T_{DF}$  not measured but guaranteed by design.

#### AC Test Conditions

- \* Input pulse levels: 0.45V to 2.4V
- \* Input and Output timing reference levels: 0.8V and 2.0V
- \* Input rise and fall times:  $\leq 20\text{ns}$
- \* Output load : 1 TTL gate plus 100pF.

#### Read Cycle Timing Waveform



## PROGRAMMING OPERATION

DC Electrical Characteristics ( $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$ ,  $V_{CC} = 6\text{V} \pm 0.25\text{V}$ ,  $V_{PP} = 12.5\text{V} \pm 0.5\text{V}$ )

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	$I_{IN}$	$V_{IH} = 5.25\text{V}$	-	-	40	$\mu\text{A}$
Operating Power						
Supply Current	$I_{CC}$	Note (7)	36	64	120	mA
$V_{PP}$ Supply Current	$I_{PP1}$	Single Byte Programming (7)	25	50	100	mA
Input Low Voltage	$V_L$	Note (5)	-0.6	-	0.8	V
Input High Voltage	$V_H$	Note (6)	2.0	-	$V_{CC} + 1$	V
Output Low Voltage (Verify)	$V_{OL}$	$I_{OL} = 2.1\text{mA}$	-	-	0.45	V
Output High Voltage (Verify)	$V_{OH}$	$I_{OH} = -400\mu\text{A}$	2.4	-	-	V

- Notes
- (1)  $V_{CC}$  must be applied before  $V_{PP}$  and removed after  $V_{PP}$ .
  - (2)  $V_{PP}$  must not exceed 13V including overshoot.
  - (3) Device reliability may be affected if device is installed or removed while  $V_{PP} = 12.5\text{V}$
  - (4) The transitions  $V_{IL}$  to 12.5V or 12.5V to  $V_{IH}$  are not allowed while  $\text{CS} = \text{Low}$ .
  - (5) -0.6V for pulse width  $\leq 20$  ns.
  - (6) If  $V_{IH}$  is over the specified maximum value, programming operation cannot be guaranteed.
  - (7) For  $V_{CC}$  and  $V_{PP}$  Supply Currents, min, typ and max values are given for 8, 16 and 32 bit mode operation respectively. Each individual value shown is a maximum.
  - (8) When programming a 0.1 $\mu\text{F}$  high frequency by-pass capacitor is required across  $V_{PP}$  and GND to suppress noise transients

## AC Characteristics

Parameter	Symbol	min	typ	max	Unit
Address Setup Time	$t_{AS}$	2	-	-	$\mu\text{s}$
OE Setup Time	$t_{OES}$	2	-	-	$\mu\text{s}$
Data Setup Time	$t_{DS}$	2	-	-	$\mu\text{s}$
Address Hold Time	$t_{AH}$	0	-	-	$\mu\text{s}$
Data Hold Time	$t_{DH}$	2	-	-	$\mu\text{s}$
OE High to Output Float Delay (1)	$t_{DF}$	0	-	130	ns
$V_{PP}$ Setup Time	$t_{VPS}$	2	-	-	$\mu\text{s}$
$V_{CC}$ Setup Time	$t_{VCS}$	2	-	-	$\mu\text{s}$
PGM Initial Program Pulse Width (2)	$t_{PW}$	0.95	-	1.05	ms
PGM Overprogram Pulse Width (3)	$t_{OPW}$	2.85	-	78.75	ms
Data Valid from OE	$t_{OE}$	-	-	150	ns
CS to Output Delay (4)	$t_{CE}$	-	-	500	ns
$V_{PP}$ Recovery Time (4)	$t_{VR}$	2	-	-	ns
$V_{PP}$ Hold Time (4)	$t_{VPH}$	2	-	-	$\mu\text{s}$

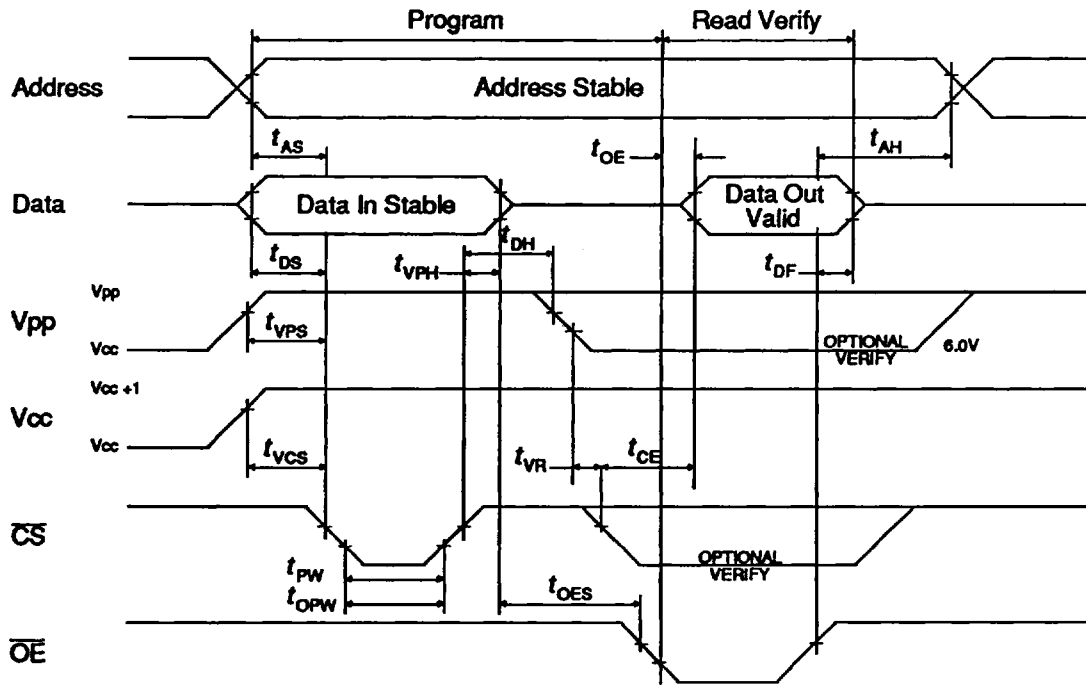
- Notes
- (1) Defines the time at which the output achieves the open circuit condition and is no longer driven. This parameter is not measured but guaranteed by design.
  - (2) Initial program pulse width tolerance is  $1\text{ ms} \pm 5\%$ .
  - (3) Length of this pulse may vary as a function of the iteration counter value n.
  - (4) Optional verify mode.

## AC Test Conditions

- \* Input pulse levels: 0.45V to 2.4V
- \* Input rise and fall times:  $\leq 20\text{ns}$
- \* Input and Output timing reference levels: 0.8V and 2.0V

**Programming Cycle Timing Waveform**

**Single Byte Programming**



## HIGH PERFORMANCE PROGRAMMING ALGORITHM

The PUMA2U1000 can be programmed using one of the algorithms shown below. This allows faster programming times without stressing the device or causing deterioration in Data Retention Time.

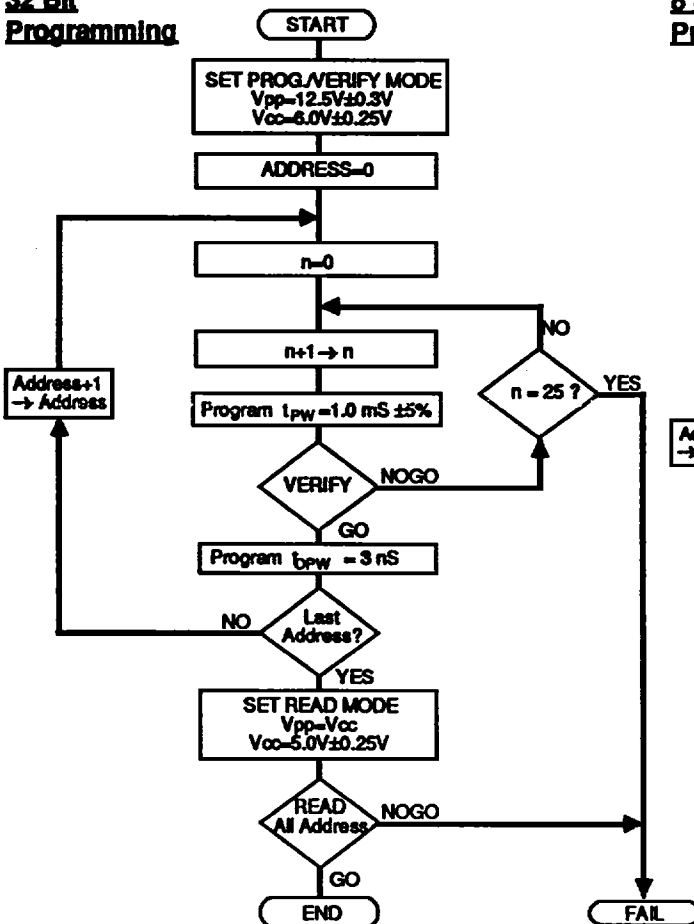
Although the flow charts specifically refers to a single EPROM, all four devices on the PUMA tile can be programmed simultaneously in 32 bit mode, in pairs in 16 bit mode or singly in 8 bit mode. Obviously 32 bit mode is potentially the fastest programming time, but this makes greater demands on the  $V_{PP}$  Supply Current.

### Programming Algorithm

Two  $\overline{CS}$  pulse widths are used to program, initial and overprogram. The address inputs are set to address the desired byte.  $V_{CC}$  is raised to 6.0V and  $\overline{OE}/V_{PP}$  is raised to 12.5V. The first  $\overline{CS}$  pulse is 1ms. The programmed byte is then verified. If the byte is programmed successfully, then an overprogram  $\overline{CS}$  pulse is applied for 3ms.

If the byte fails to program after the first 1ms pulse, then up to 25 successive 1ms pulses are applied with

#### 32 Bit Programming



a verification after each pulse. When the byte passes verification, the overprogram pulse width is 3X (times) the number of 1ms pulses required earlier (75ms max).

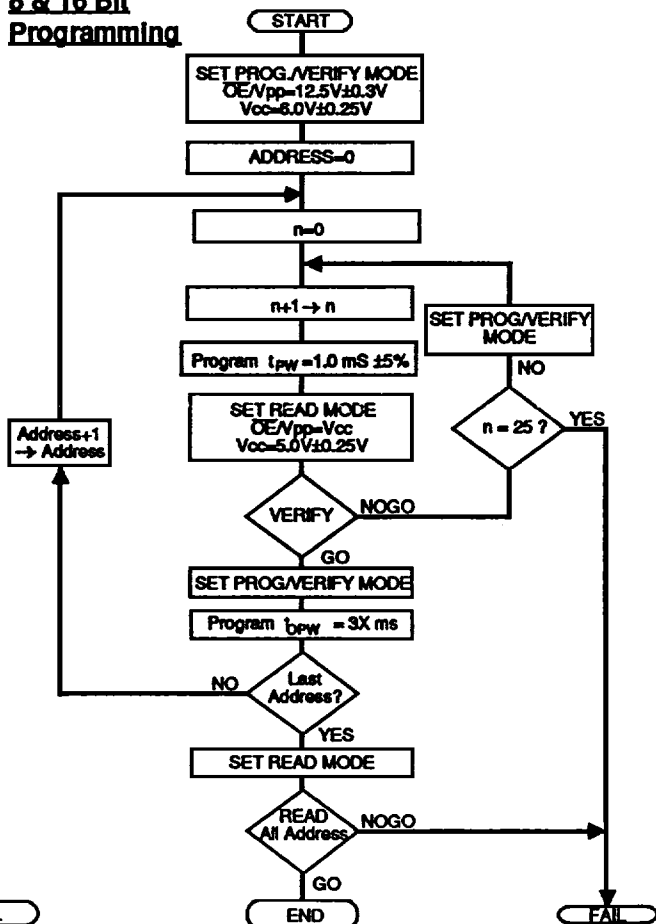
**IMPORTANT.** The Verify mode of each EPROM on the PUMA 2U1000 can only be correctly used if it is operating in 32 bit mode. When configured in 16 or 8 bit mode (i.e. if any data outputs of the EPROMs are commoned) then in order to check correct programming of a byte on a particular device it must be placed in Read mode first. This is because during Verify the  $\overline{CS}$  input is a Don't Care (see page 2) and so either 2 (16 bit) or 4 (8 bit) devices would be trying to drive the Data Bus at the same time.

If the part fails to verify after 25 1ms pulses have been applied, it is considered as failed. After the first byte is programmed, the address inputs are set to the next address repeating the algorithm until all required addresses are programmed. Then  $V_{CC}$  and  $\overline{OE}/V_{PP}$  are lowered to 5.0V. All bytes subsequently are read to compare with the original data to determine if the device passes or fails.

Notes:

1.  $V_{CC}$  must be applied simultaneously or before  $\overline{OE}/V_{PP}$  and removed simultaneously or after  $\overline{OE}/V_{PP}$ .

#### 8 & 16 Bit Programming



**ERASE**

Erasure of the PUMA 2U1000 is performed by exposure to ultraviolet light of 2537 Å at a minimum intensity of 15WS/cm<sup>2</sup>, for approximately 15 - 20 minutes.

Note that sunlight and fluorescent light may contain sufficient ultraviolet light to erase the programmed information. For this reason, and anyway for any operation in the READ mode, the transparent lids on this device should be covered with an opaque label.

**Connection Table**

<i>PGA Pin No.</i>	<i>Signal Name</i>	<i>PGA Pin No.</i>	<i>Signal Name</i>	<i>PGA Pin No.</i>	<i>Signal Name</i>	<i>PGA Pin No.</i>	<i>Signal Name</i>	<i>PGA Pin No.</i>	<i>Signal Name</i>
1	D8	2	D9	3	D10	4	A13	5	Vpp
6	NC	7	NC	8	NC	9	D0	10	D1
11	D2	12	A14	13	$\overline{CS2}$	14	GND	15	D11
16	A10	17	A11	18	A12	19	Vcc	20	$\overline{CS1}$
21	NC	22	D3	23	D15	24	D14	25	D13
26	D12	27	$\overline{OE}$	28	NC	29	A14	30	D7
31	D6	32	D5	33	D4	34	D24	35	D25
36	D26	37	A6	38	A7	39	NC	40	A8
41	A9	42	D16	43	D17	44	D18	45	Vcc
46	$\overline{CS4}$	47	A14	48	D27	49	A3	50	A4
51	A5	52	A14	53	$\overline{CS3}$	54	GND	55	D19
56	D31	57	D30	58	D29	59	D28	60	A0
61	A1	62	A2	63	D23	64	D22	65	D21
66	D20								

**Note:**

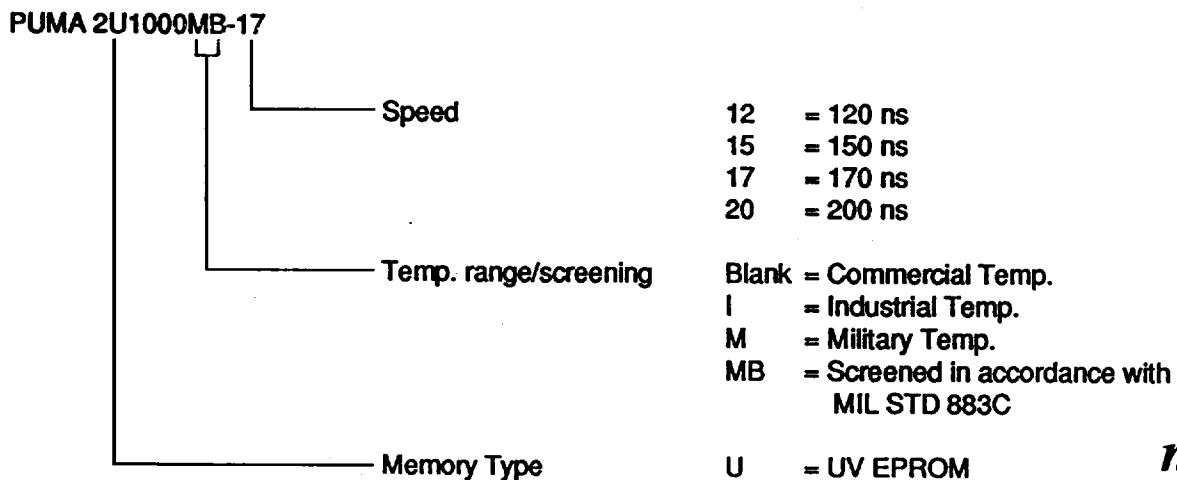
Pins 12, 29, 47 and 52 (A14) are not connected together on the PUMA substrate - they must be connected externally.

**Military Screening Procedure**

Module Screening Flow for high reliability product is in accordance with MIL-STD-883C method 5004 Level B and is detailed below:

MB MODULE SCREENING FLOW		
SCREEN	TEST METHOD	LEVEL
<b>Visual and Mechanical</b> External visual Temperature cycle	2017 Condition B (or manufacturers equivalent) 1010 Condition C (10 Cycles, -65°C to +150°C)	100% 100%
<b>Burn-In</b> Pre Burn-in Electrical Burn-In	Per Applicable device Specifications at Ta = +25°C (optional) Method 1015, Condition D, Ta = +125°C	100% 100%
<b>Final Electrical Tests</b> Static (dc) Functional Switching (ac)	Per applicable Device Specification a) @ Ta=+25°C and power supply extremes b) @ temperature and power supply extremes a) @ Ta=+25°C and power supply extremes b) @ temperature and power supply extremes a) @ Ta=+25°C and power supply extremes b) @ temperature and power supply extremes	100% 100% 100% 100% 100% 100%
<b>Percent Defective Allowable (PDA)</b>	Calculated at Post Burn-in at Ta=+25°C	10%
<b>Quality Conformance</b>	Per applicable Device Specification	Sample
<b>External Visual</b>	2009 Per HMP or customer specification	

**Ordering Information**



Mosaic Semiconductor Inc.

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