HARRIS SEMICONDUCTOR

HIP4010

ADVANCE INFORMATION

April 1994

Power Full Bridge Driver for Low Voltage Motor Drive with Direction and Brake Control

Features

- Two Independent Complementary MOS Output Half Bridge Drivers for Operation with Low Power Supply Voltages
- Load Switching Capabilities . . . . . to 0.5A with +5V Power Supply
- Single Supply Range . . . . . +3V to +7V
- Split Supply Option with a Negative Reference for the H-Switch Power Drivers
- Low Standby Current
- CMOS/TTL Compatible Input Logic
- Over-Temperature Protection
- Current-Overload Protection
- Over-Current Fault Flag Output
- Direction, Braking and PWM Control

Applications

- DC Motor Driver
- Relay Driver
- Solenoid Driver
- Stepper Motor Controller
- Air Core Gauge Instrument Driver
- Speedometer Displays
- Tachometer Displays
- Remote Power Switch
- +3V to +6V Battery Operated Switch Circuits
- Logic and Microcontroller Operated Switch

Description

In the Functional Block Diagram of the HIP4010 the four switches and a load are arranged in an H-Configuration so that the drive voltage from terminals OUTA and OUTB can be cross-switched to change the direction of current flow in the load. This is commonly known as 4-quadrant load control. As shown in the Block Diagram, switches Q1 and Q4 are conducting or in an ON state when current flows from V_{DDA} through Q1, through the load, and then through Q4 to terminal V_{SSB}; where load terminal OUTA is at a positive potential with respect to OUTB. Switches Q1 and Q4 are operated synchronously by the control logic. The control logic switches Q3 and Q2 to an open or OFF state when Q1 and Q4 are switched ON. To reverse the current flow in the load, the switch states are reversed where Q1 and Q4 are OFF while Q2 and Q3 are ON. Consequently, current then flows from V_{DDB} through Q3, through the load, and through Q2 to terminal V_{SSA}, and load terminal OUTB is then at a positive potential with respect to OUTA.

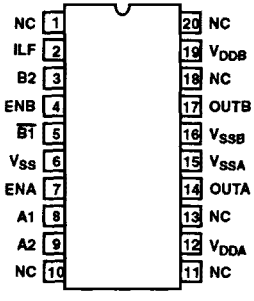
The positive power supply terminals are V_{DDA} and V_{DDB} and are internally connected on the chip. Terminals ENA and ENB are ENABLE Inputs for the Logic A and B Input Controls. The ILF output is an Over-Current Limit Fault Flag Output and indicates a fault condition for either Output A or B or both. While V_{DDA}, V_{DDB} and V_{SS} are the Power Supply reference terminals for the A and B Control Logic Inputs and ILF Output, the V_{SSA} and V_{SSB} Power Supply terminals are separate and independent from V_{SS} and may be more negative than the V_{SS} ground reference terminal. This is accomplished with the use of level shifting in the gate drive circuitry to the NMOS (low-side) output stages.

Ordering Information

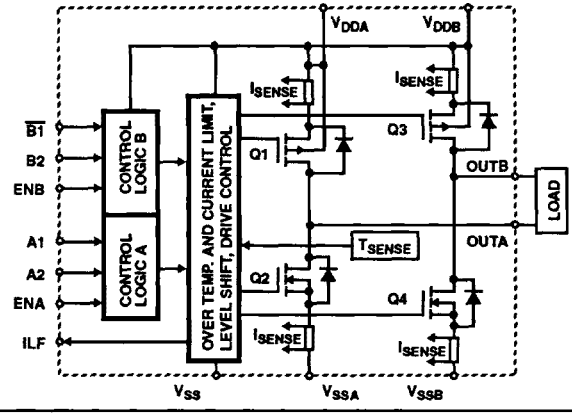
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP4010IB	-40°C to +85°C	20 Lead Plastic SOIC (W)

Pinout

HIP4010 (SOIC)
TOP VIEW



Block Diagram



6 FULL BRIDGE

File Number 3176.1

Absolute Maximum Ratings

Supply Voltage; V_{DDA} and V_{DDB} to V_{SS} or V_{SSA} or V_{SSB} ..... +7V
Neg. Output Supply Voltage, (V_{SSA},V_{SSB}) ..... (Note 1)
DC Logic Input Voltage (Each Input)
..... (V_{SS}-0.5V) to (V_{DDA}, V_{DDB} +0.5V)
DC Logic Input Current (Each Input) .....±20mA
ILF Fault Output Current.....±20mA
Output Load Current, (Self Limiting, See Elec. Spec.)..... $\pm I_{O(LIMIT)}$

Reliability Information

Thermal Resistance, θ_{JA} ..... 90°C/W
Power Dissipation
At +25°C (Free Air) 1.39W
Above +25°C ..... Derate Linearly at 11.1mW/°C
Storage Temperature Range.....-65°C to +150°C
Maximum Junction Temperature ..... +150°C
Lead Temperature (Soldering 10s) ..... +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions T_A = +25°C, V_{SUPPLY} = V_{DDA} = V_{DDB} = +5V, V_{SSA} = V_{SSB} = V_{SS} = 0V; Unless Otherwise Specified

Typical Operating Supply Voltage Range ..... +3 to +7V
Minimum Logic Supply Voltage (V_{DD} -V_{SS})..... +2V
Typical NMOS Driver $R_{DS(ON)}$, 0.5A Load 0.8Ω
Typical PMOS Driver $R_{DS(ON)}$, 0.5A Load.....1.0Ω
Input Low Voltage, V_{IL}.....0V to +0.8V
Input High Voltage, V_{IH} ..... +2.0V to V_{DD}
Input Resistance 0.5TΩ

Electrical Specifications T_A = +25°C; V_{SUPPLY} = V_{DDA} = V_{DDB} = +5V, V_{SSA} = V_{SSB} = V_{SS} = 0V; Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{LEAK}		-	40	50	pA
Input Voltage Range	V_{IN}		0	-	5	V
Low Level Input Voltage	V_{IL}		-	-	0.8	V
High Level Input Voltage	V_{IH}		2	-	-	V
ILF Output Low, Sink Current	I_{OH}	V_{OUT} = 0.4V	3	8	-	mA
ILF Output High, Source Current	I_{OL}	V_{OUT} = 4.6V	-	-4.5	-1.5	mA
ILF Output Low (Sink) Current;	I_{OH}	V_{SUPPLY} =+3V, V_{OUT} = 0.4V	1.5	3	-	mA
ILF Output High (Source) Current);	I_{OL}	V_{SUPPLY} =+3V, V_{OUT} = 2.6V	-	-1.6	-0.8	mA
Input Capacitance	C_{IN}		-	TBE	-	pF
Idle Supply Current; No Load	I_{SUPPLY}		-	0.8	1.5	mA
OUTA, OUTB Voltage High	V_{OH}	I_{SOURCE} = 0.5A	4.2	4.5	-	V
OUTA, OUTB Voltage Low	V_{OL}	I_{SINK} = 0.5A	-	0.4	0.6	V
OUTA, OUTB Source Current Limiting	$I_{O(LIMIT)}$		500	550	620	mA
OUTA, OUTB Sink Current Limiting	$-I_{O(LIMIT)}$		500	550	620	mA
OUTA, OUTB Voltage High	V_{OH}	V_{SUPPLY} =+3V, I_{SOURCE} = 0.3A	2.25	2.5	-	V
OUTA, OUTB Voltage Low	V_{OL}	V_{SUPPLY} =+3V, I_{SINK} = 0.3A	-	0.5	0.65	V
Response Time: V_{EN} to V_{OUT} Turn-on: Prop Delay Rise Time Turn-off: Prop Delay Fall Time	 t_{PLH} t_R t_{PHL} t_F	I_O = 0.5A (Note 2)	-	 4 TBE 0.25 TBE	-	µs

NOTES:

1. V_{SS} is the required common ground reference for the logic input switching. The load currents may be switched near the common ground reference by using a split supply for V_{DDA} and V_{DDB} to V_{SSA} and V_{SSB}. For an uneven split in the supply voltage, the Maximum Negative Output Supply Voltage to V_{SSA} and V_{SSB} is limited by the Maximum V_{DDA} and V_{DDB} to V_{SSA} and V_{SSB} ratings. For all operating conditions the required positive voltages on V_{DDA} and V_{DDB} must be equal and common.
2. Refer to the TRUTH TABLE and the V_{EN} to V_{OUT} SWITCHING WAVEFORMS. Current, I_O refers to I_{OUTA} or I_{OUTB} as the Output Load current. Note that ENA controls OUTA and ENB controls OUTB. Each Half H-Switch has independent control from the respective A1, A2, ENA or $\overline{B1}$, B2, ENB inputs. Refer to the TERMINAL INFORMATION TABLE for external pin connections to establish mode control switching. Figure 1 shows a typical application circuit used to control a DC Motor.

TERMINAL INFORMATION TABLE

V_{DDA}, V_{DDB}	Positive Power Supply pins; internally connected and must be externally connect to the same Positive Supply (V+).
V_{SSA}	Negative Power Supply pin; Negative or Ground return for Switch Driver A.
V_{SSB}	Negative Power Supply pin; Negative or Ground return for Switch Driver B.
V_{SS}	Common Ground pin for the Input Logic Control circuits.
A1, $\overline{B1}$	Input pins used to control the direction of output load current to/from OUTA and OUTB, respectively. When connected, A1 and $\overline{B1}$ can be controlled from the same logic signal to change the directional rotation of a motor.
A2, B2	Input pins used to force a low state on OUTA and OUTB, respectively. When connected, A2 and B2 can be controlled from the same logic signal to activate Dynamic Braking of a motor.
ENA, ENB	Input pins used to Enable Switch Driver A and Switch Driver B, respectively. When Low, the respective output is in a high impedance (Z) off-state. Since each Switch Driver is independently controlled, OUTA and OUTB may be a separately PWM controlled as Half H-Switch Drivers.
OUTA, OUTB	Respectively, Switch Driver A and Switch Driver B Output pins.
ILF	Current Limiting Fault Output Flag pin; when in a high logic state, signifies that Switch Driver A or B or both are in a Current Limiting Fault Mode.

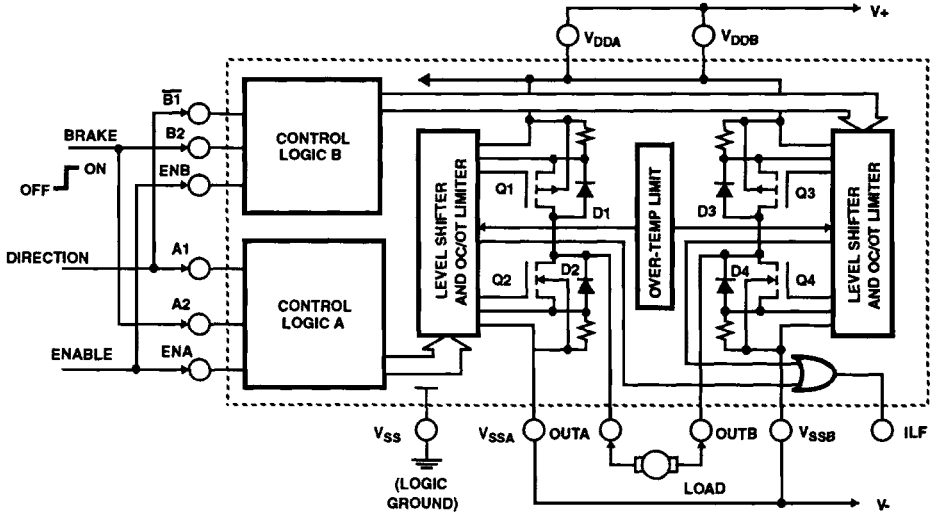
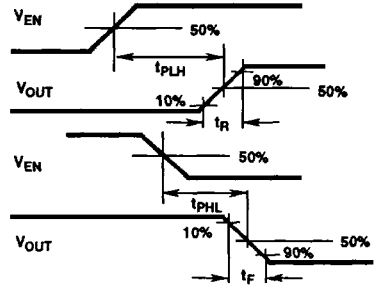


FIGURE 1. TYPICAL HIP4010 MOTOR CONTROL APPLICATION CIRCUIT SHOWING DIRECTIONAL AND BRAKING CONTROL

TRUTH TABLE

SWITCH DRIVER A				SWITCH DRIVER B			
INPUTS			OUTPUT	INPUTS			OUTPUT
A1	A2	ENA	OUTA	B1	B2	ENB	OUTB
H	L	H	OH	L	L	H	OH
L	L	H	OL	H	L	H	OL
H	H	H	OL	L	H	H	OL
L	H	H	OL	H	H	H	OL
X	X	L	Z	X	X	L	Z

L = Low logic level; H = High logic level
Z = High Impedance (off state)
OH = Output High (sourcing current to the output terminal)
OL = Output Low (sinking current from the output terminal)
X = Don't Care



SWITCHING WAVEFORMS

Applications

The HIP4010 is designed to detect load current feedback from sampling resistors of low value in the source connections of the output drivers to V_{DDA}, V_{DDB}, V_{SSA} and V_{SSB} (See Figure 1). When the sink or source current at OUTA or OUTB exceeds the preset OC (Over-Current) limiting value of 550mA typical, the current is held at the limiting value. If the OT (Over-Temperature) Protection limit is exceeded, temperature sensing BiMOS circuits limit the junction temperature to 150°C typical.

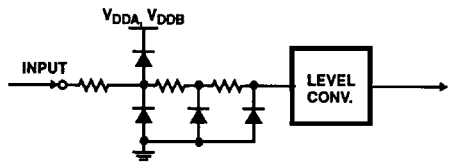
The circuit of Figure 1 shows a Low Voltage motor-driver application for the HIP4010 as a Full H-Switch. The left (A) and right (B) H-Switch's are controlled from the A and B inputs via the A and B CONTROL LOGIC to the MOS output transistors Q1, Q2, Q3 and Q4. The circuit is intended to safely start, stop, and control rotational direction for a motor requiring no more than 0.5A of supply current. The stop function includes a Dynamic Braking feature.

With the ENABLE Inputs Low, the MOS transistors Q1 and Q3 are OFF; which cuts-off supply current to OUTA and OUTB. With the BRAKE terminal Low and ENABLE Inputs High, either Q1 and Q4 or Q3 and Q2 will be driven into conduction by the DIRECTION Input Control terminal. The MOS output transistor pair chosen for conduction is determined by the logic level applied to the DIRECTION control; resulting in either clockwise (CW) or counter-clockwise (CCW) shaft rotation.

When the BRAKE terminal is switched high (while holding the ENABLE input high), the gates of both Q2 and Q4 are driven high. Current flowing through Q2 (from the motor terminal OUTA) at the moment of Dynamic Braking will continue to flow through Q2 to the V_{SSA} and V_{SSB} external connection, and then continue through diode D4 to the motor terminal OUTB. As such, the resistance of the motor winding (and the series-connected path) dissipates the kinetic energy stored in the system. Reversing rotation, current flowing through Q4 (from the motor terminal OUTB), at the moment of Dynamic Braking, would continue to flow through Q4 to the V_{SSB} and V_{SSA} tie, and then continue through diode D2 to the motor terminal OUTA, to dissipate the stored kinetic energy as previously described.

Where V_{DDA} and V_{DDB} to V_{SS} are the Power Supply reference terminals for the Control Logic, the lowest practical supply voltage for proper logic control should be no less than 2.0V. The V_{SSA} and V_{SSB} terminals are separate and independent from V_{SS} and may be more negative than the V_{SS} ground reference terminal. However, the maximum supply level from V_{DDA} and V_{DDB} to V_{SSA} or V_{SSB} must not be greater than the Absolute Maximum Supply Voltage rating of 7V.

Terminals A1, $\overline{B1}$, A2, B2, ENA and ENB are internally connected to protection circuits intended to guard the CMOS gate-oxides against damage due to electrostatic discharge. (See Figure 3) Inputs ENA, ENB, A1, $\overline{B1}$ A2 and B2 have CD74HCT4000 Logic Interface Protection and Level Converters for TTL or CMOS input Logic. These inputs are designed to typically provide ESD protection up to 2kV. However, these devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.



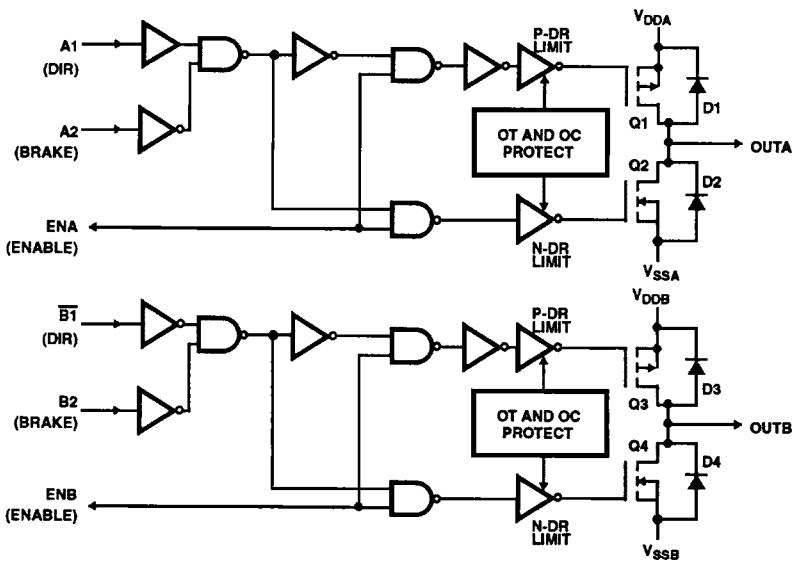


FIGURE 2. EQUIVALENT CONTROL LOGIC A AND B SHOWN DRIVING THE OUTA AND OUTB OUTPUT DRIVERS