Data Sheet
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microelectronics group

Lucent Technologies
Bell Labs Innovations

T7295-6 DS3/SONET STS-1 Integrated Line Receiver

Features

- Fully integrated receive interface supports **both** DS3 and STS-1 rate signals
- Integrated equalization (optional) and timing recovery
- Loss-of-signal and loss-of-lock alarms
- Variable input sensitivity control
- 5 V power supply
- Intended for use in systems that must comply with ITU-T G.703, ITU-T G.824, Bellcore TR-NWT-000499, ANSI T1.104, and ANSI T1.102
- Direct replacement for either the T7295-3 or T7295-5 devices

Description

The T7295-6 DS3/SONET STS-1 Integrated Line Receiver is a fully integrated receive interface that terminates a bipolar DS3 (44.736 Mbits/s) or SONET STS-1 (51.84 Mbits/s) signal transmitted over coaxial cable. Another version of this device is available for operation at the E3 (34.368 Mbits/s) data rate.

The device also provides the functions of receive equalization (optional), automatic-gain control (AGC), clock recovery and data retiming, and loss-of-signal and loss-of-frequency-lock detection. The digital system interface is dual rail, with received positive and negative 1s appearing as unipolar digital signals on separate output leads. The on-chip equalizer is designed for cable distances of 0 ft. to 450 ft. from the cross connect frame to the device. High input sensitivity allows for significant amounts of flat loss within the system. An input reference clock provides the frequency reference for the device to operate at both the DS3 and SONET STS-1 rates. Figure 1 shows the block diagram of the device.

The T7295-6 device is manufactured using linear CMOS technology and is packaged in a 20-pin, plastic DIP or a 20-pin, plastic SOJ package for surface mounting.

Description (continued)

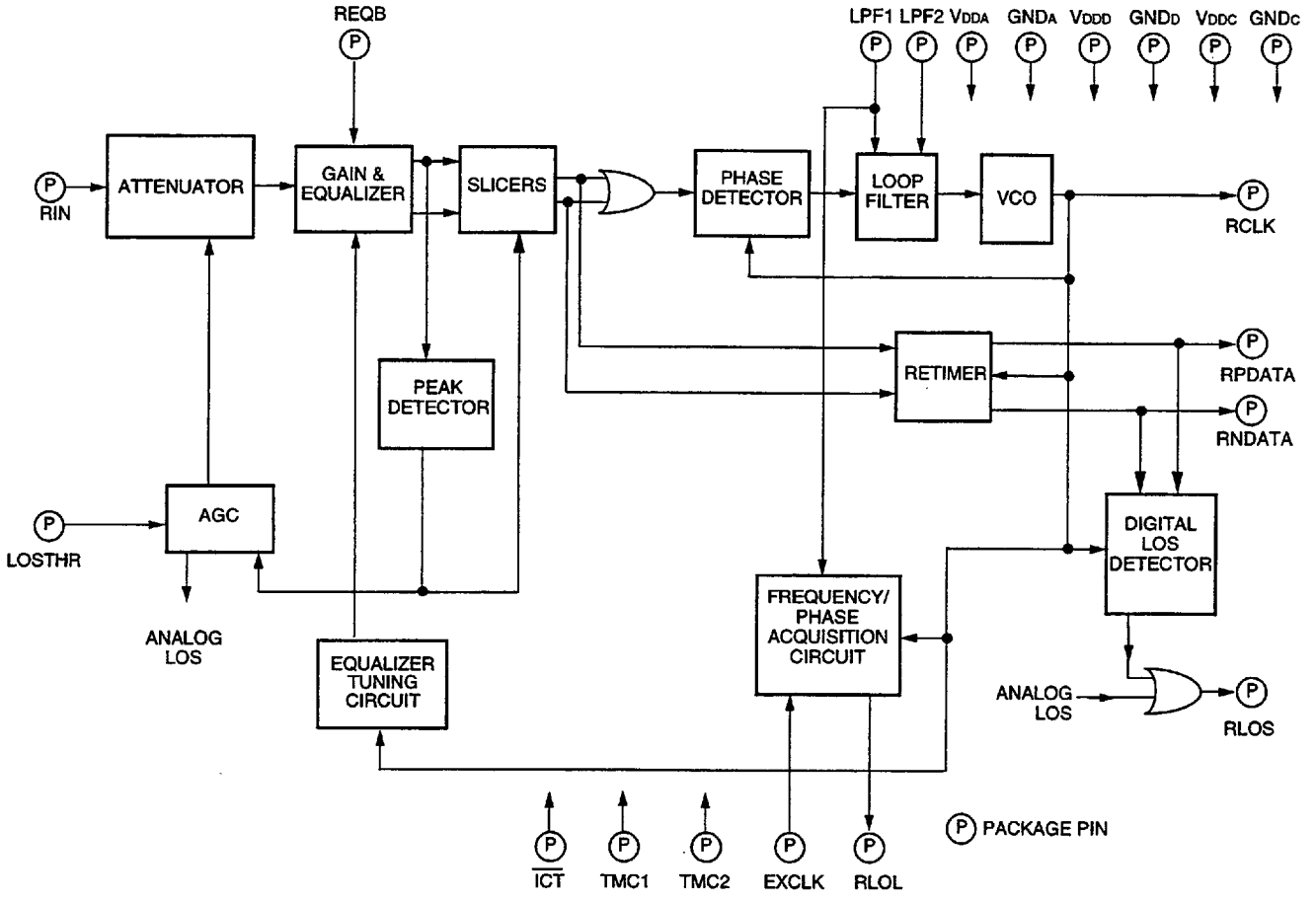

Figure 1. Block Diagram

Pin Information

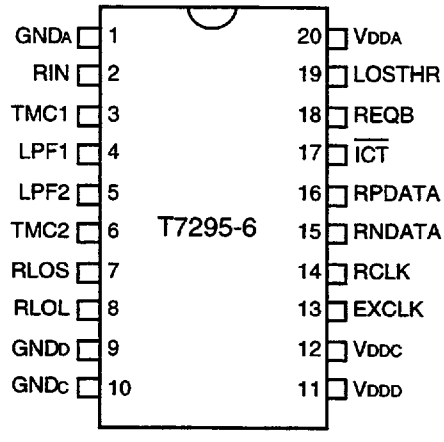

Figure 2. Pin Assignment

Pin Information (continued)

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Description
1	GNDA	—	**Analog Ground.**
2	RIN	I	**Receive Input.** Analog receive input. This pin is internally biased at about 1.5 V in series with 50 kΩ.
3, 6	TMC1—TMC2	I	**Test Mode Control 1 and 2.** Internal test modes are enabled within the device by using TMC1 and TMC2. Users must tie these pins to the ground plane.
4, 5	LPF1—LPF2	I	**PLL Filter 1 and 2.** An external capacitor (0.1 µF ± 20%) is connected between these pins. The capacitor should be mounted as close to the pins as possible (within 0.5 inches is recommended).
7	RLOS	O	**Receive Loss of Signal.** This pin is set high on loss of the data signal at the receive input.
8	RLOL	O	**Receive PLL Loss of Lock.** This pin is set high on loss of PLL frequency lock.
9	GNDD	—	**Digital Ground for PLL Clock.** Ground lead for all circuitry running synchronously with PLL clock.
10	GNDC	—	**Digital Ground for EXCLK.** Ground lead for all circuitry running synchronously with EXCLK.
11	VDDD	—	**5 V Digital Supply (±10%) for PLL Clock.** Power for all circuitry running synchronously with PLL clock.
12	VDDC	—	**5 V Digital Supply (±10%) for EXCLK.** Power for all circuitry running synchronously with EXCLK.
13	EXCLK	I	**External Reference Clock.** A valid DS3 (44.736 MHz ± 100 ppm) or STS-1 (51.84 MHz ± 100 ppm) clock must be provided at this input. EXCLK must be an independent clock to help guarantee device performance for all specifications. The duty cycle of EXCLK, referenced to VDD/2 levels, must be 40% to 60% with a maximum rise and fall time (10% to 90%) of 5 ns.
14	RCLK	O	**Receive Clock.** Recovered clock signal to the terminal equipment.
15	RNDATA	O	**Receive Negative Data.** Negative pulse data output to the terminal equipment.
16	RPDATA	O	**Receive Positive Data.** Positive pulse data output to the terminal equipment.
17	$\overline{\text{ICT}}$	I	**In-Circuit Test Control (Active-Low).** If $\overline{\text{ICT}}$ is forced low, all digital output pins (RCLK, RPDATA, RNDATA, RLOS, RLOL) are placed in a high-impedance state to allow for in-circuit testing. A nominal 50 kΩ pull-up is provided on this pin.
18	REQB	I	**Receive Equalization Bypass.** A high on this pin bypasses the internal equalizer. A low places the equalizer in the data path.
19	LOSTHR	I	**Loss-of-Signal Threshold Control.** The voltage forced on this pin controls the input loss-of-signal threshold. Three settings are provided by forcing GND, VDD/2, or VDD. This pin must be set to the desired level upon powerup and should not be changed during operation.
20	VDDA	—	**5 V Analog Supply (±10%).**

Application

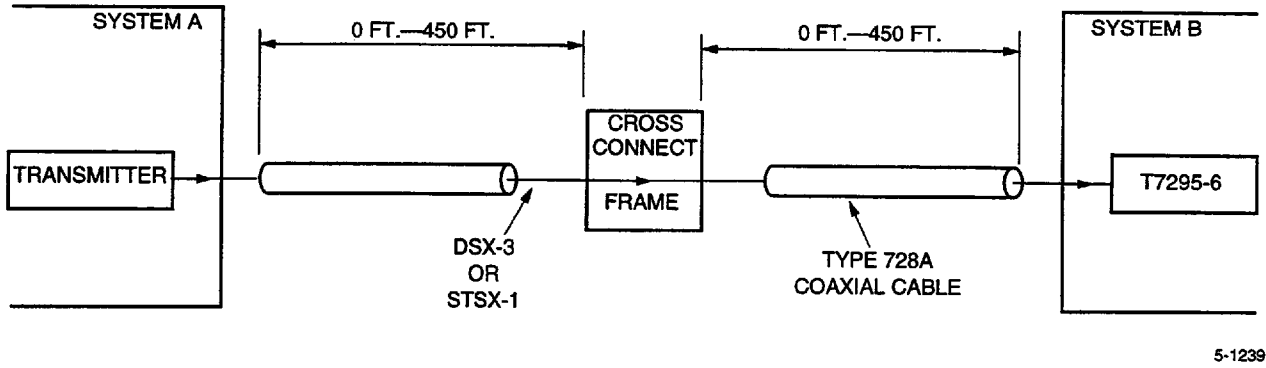

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Figure 3. Application Diagram

The T7295-6 accepts a single-ended input signal as shown in Figure 4.

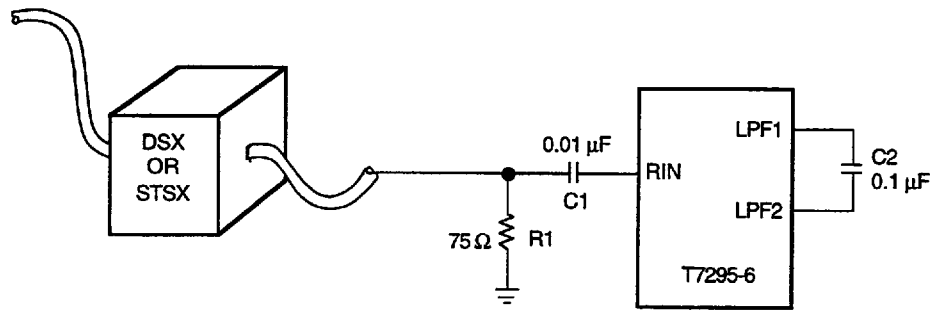

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Figure 4. Input Configuration

Overview

Receive Path Configurations

Receive Signal Path

In the receive signal path (see Figure 1), the internal equalizer can be included by setting REQB = 0 or bypassed by setting REQB = 1. The equalizer bypass option allows easy interfacing of the T7295-6 device into systems already containing external equalizers. Figure 5 illustrates the receive path options.

In case 1, the signal from the cross connect feeds directly into the T7295-6 input. In this mode, the user sets REQB = 0, engaging the equalizer in the data path. Table 2 and the following sections describe the receive signal requirements.

In case 2, external line build-out (LBO) and equalizer networks precede the T7295-6 device. In this mode, the signal at the T7295-6 input is already equalized, and the on-chip filters are bypassed by setting REQB = 1. The signal at the T7295-6 input must meet the amplitude limits described in Table 2.

In applications where the T7295-6 device is used to monitor transmitter outputs directly, the receive equalizer should be bypassed. Again, the signal at the T7295-6 input must meet the amplitude limits described in Table 2.

Table 2. Receive Input Signal Amplitude Requirements

Although system designers typically use power in dBm to describe input levels, the T7295-6 responds to peak input signal amplitude. Therefore, the T7295-6 input signal limits are given in mV pk. Conversion factors are as follows:

At DSX-3: 390 mV pk ≅ 0 dBm
At DSX-3 + 450 ft. of cable: 310 mV pk ≅ 0 dBm.

The maximum input amplitude under all conditions is 850 mV pk.

Data Rate	REQB	LOSTHR	Minimum Signal*	Unit
DS3	0	0	80	mV pk
		$V_{DD}/2$	60	mV pk
		V_{DD}	40	mV pk
	1	0	80	mV pk
		$V_{DD}/2$	80	mV pk
		V_{DD}	80	mV pk
STS-1	0	0	110	mV pk
		$V_{DD}/2$	80	mV pk
		V_{DD}	60	mV pk
	1	0	110	mV pk
		$V_{DD}/2$	110	mV pk
		V_{DD}	110	mV pk

* Minimum signals are for SOJ devices. Due to increased package parasitics, add 3 dB to all table values for DIP devices.

Overview (continued)

Receive Path Configurations (continued)

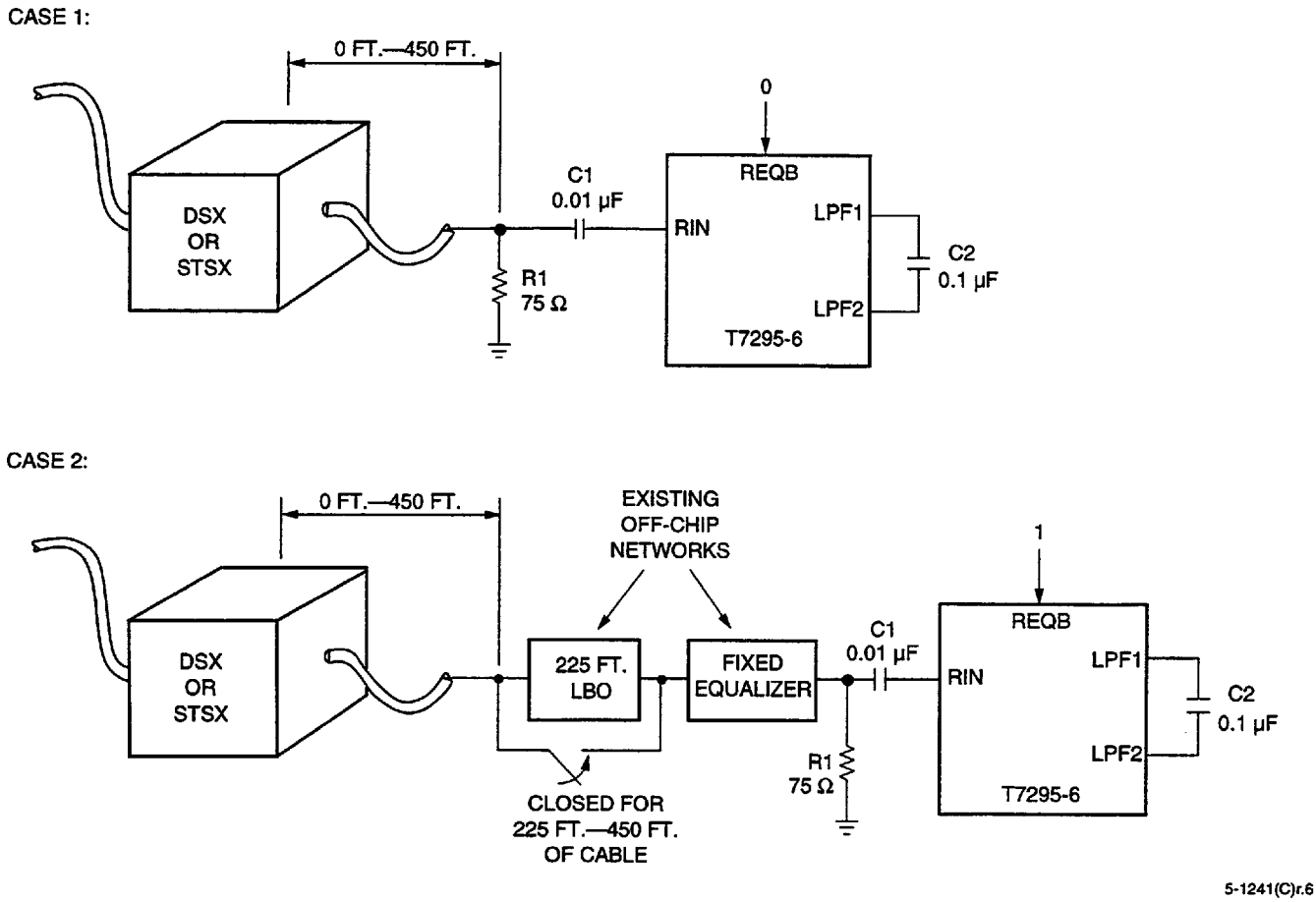

Figure 5. Receiver Configurations

DS3 Signal Requirements at the DSX

For DS3 operation, pulse characteristics are specified at the DSX-3, which is an interconnection and test point referred to as the cross connect. The cross connect exists at the point where the transmitted signal reaches the distribution frame jack. The T7295-6 can receive through 450 ft. of 728A cable from the DSX-3 in DS3 mode. Table 3 lists the signal requirements.

Currently, two isolated pulse template requirements exist: the ANSI TI.404 pulse template (see Table 4 and Figure 6) and the Bellcore TR-NWT-000499 pulse template (see Table 5 and Figure 7). The T7295-6 correctly decodes any transmitted signal that meets one of these templates at the cross connect.

Overview (continued)

DS3 Signal Requirements at the DSX (continued)

Table 3. DSX-3 Interconnection Specification

Parameter	Specification
Line Rate	44.736 Mbits/s ± 20 ppm.
Line Code	Bipolar with three-0 substitution (B3ZS).
Test Load	75 Ω ± 5%.
Pulse Shape	An isolated pulse must fit the template in Figure 6 or Figure 7.* The pulse amplitude may be scaled by a constant factor to fit the template. The pulse amplitude must be between 0.36 V pk and 0.85 V pk, measured at the center of the pulse.
Power Levels	For an all-1s transmitted pattern, the power at 22.368 MHz ± 0.002 MHz must be –1.8 dBm to +5.7 dBm, and the power at 44.736 MHz ± 0.002 MHz must be –21.8 dBm to –14.3 dBm.†‡

* The proposed G.703 states that the voltage in a time slot containing a zero must not exceed ±5% of the peak pulse amplitude, except for the residue of preceding pulses.
† The power levels specified by the proposed G.703 are identical except that the power is to be measured in 3 kHz bands.
‡ The all-1s pattern must be a pure all-1s signal, without framing or other control bits.

Table 4. DSX-3 Pulse Template Boundaries for ANSI T1.404 (See Figure 6.)

Lower Curve		Upper Curve	
Time	**Equation**	**Time**	**Equation**
$T \le -0.36$	–0.03	$T \le -0.68$	+0.03
$-0.36 \le T \le +0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right] - 0.03$	$-0.68 \le T \le +0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right] + 0.03$
$+0.36 \le T$	–0.03	$+0.36 \le T$	$0.05 + 0.407e^{-1.84[T-0.36]}$

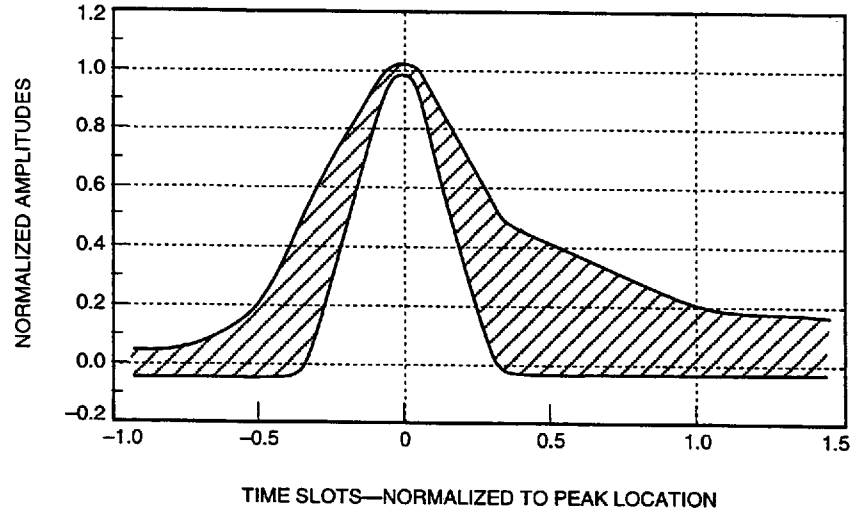

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Figure 6. DSX-3 Isolated Pulse Template for ANSI T1.404

Overview (continued)

DS3 Signal Requirements at the DSX (continued)

Table 5. DSX-3 Pulse Template Boundaries for Bellcore TR-NWT-000499 (See Figure 7.)

Lower Curve		Upper Curve	
Time	**Equation**	**Time**	**Equation**
$-0.85 \le T \le -0.36$	-0.03	$-0.85 \le T \le -0.68$	$+0.03$
$-0.36 \le T \le +0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right] - 0.03$	$-0.68 \le T \le +0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right] + 0.03$
$+0.36 \le T \le +1.4$	-0.03	$+0.36 \le T \le +1.4$	$0.08 + 0.407e^{-1.84[T-0.36]}$

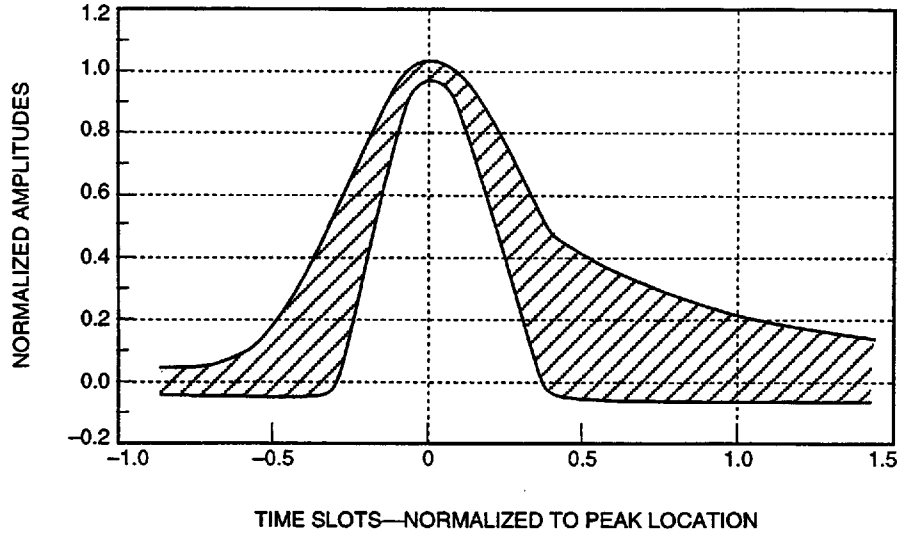

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Figure 7. DSX-3 Isolated Pulse Template for Bellcore TR-NWT-000499

Overview (continued)

STS-1 Signal Requirements at the STSX

For STS-1 operation, pulse characteristics are specified at the STSX-1, which is an interconnection and test point referred to as the cross connect. The cross connect exists at the point where the transmitted signal reaches the distribution frame jack. The T7295-6 can receive through 450 ft. of 728A cable from the STSX-1 in STS-1 mode. A pulse template is specified per ANSI T1.102 standards (see Figure 8). The T7295-6 correctly decodes any transmitted signal that meets the mask shown in Figure 8 at the STSX-1.

Table 6. STSX-1 Interconnection Specification

Parameter	Specification
Line Rate	51.84 Mbits/s.
Line Code	Bipolar with three-0 substitution (B3ZS).
Test Load	75 Ω ± 5%.
Power Levels	A wideband power level measurement at the STSX-1 interface using a low-pass filter with a 3 dB cutoff frequency of at least 200 MHz is within –2.7 dBm and +4.7 dBm.

Table 7. STSX-1 Pulse Template Boundaries for ANSI T1.102 (See Figure 8.)

Lower Curve		Upper Curve	
Time	**Equation**	**Time**	**Equation**
$-0.85 \le T \le -0.38$	-0.03	$-0.85 \le T \le -0.68$	$+0.03$
$-0.38 \le T \le +0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right] - 0.03$	$-0.68 \le T \le +0.26$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right] + 0.03$
$+0.36 \le T \le +1.4$	-0.03	$+0.26 \le T \le +1.4$	$0.1 + 0.61e^{-2.4[T - 0.26]}$

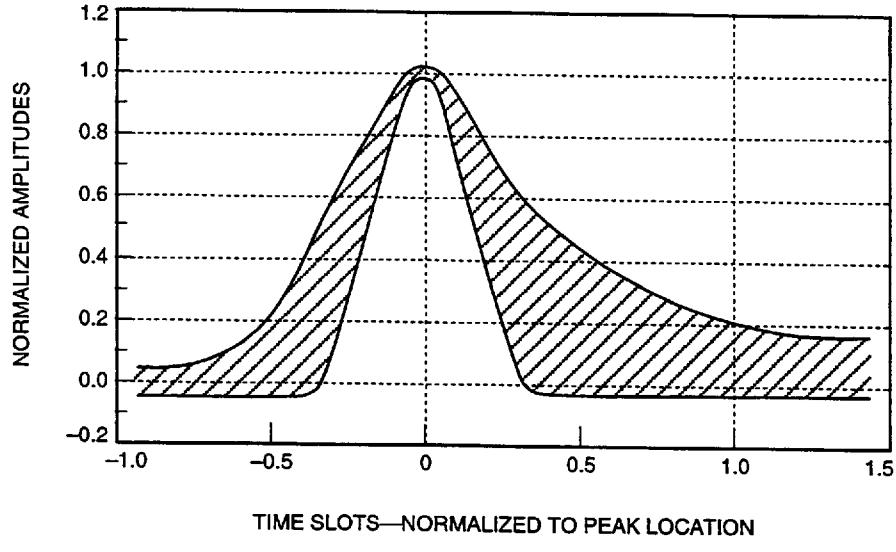

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Figure 8. STSX-1 Isolated Pulse Template for ANSI T1.102

Overview (continued)

Input Capacitance

The input capacitance at the RIN pin is typically 2.8 pF (SOJ package) and 3.6 pF (DIP package).

Cable Loss Characteristics

The signal at the cross connect may travel through a distribution frame, coaxial cable, connectors, splitters, and backplanes before reaching the T7295-6 device. This section defines the maximum distribution frame and cable loss from the cross connect to the T7295-6 input.

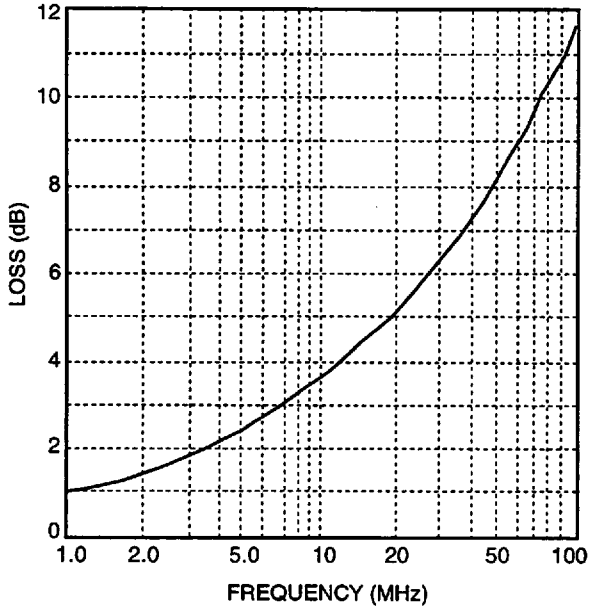


Figure 9. Loss Characteristic of 728A Coaxial Cable (450 ft.)

The distribution frame jack may introduce 0.6 dB ± 0.55 dB of loss. This loss may be any combination of flat or shaped (cable) loss.

The maximum cable distance between the point where the transmitted signal exits the distribution frame jack and the T7295-6 device is 450 ft. (see Figure 3). The coaxial cable (Type 728A) used to specify that this distance limitation has the loss and phase characteristics shown in Figure 9 and Figure 10. Other cable types also may be acceptable if distances are scaled to maintain cable loss equivalent to Type 728A cable loss.

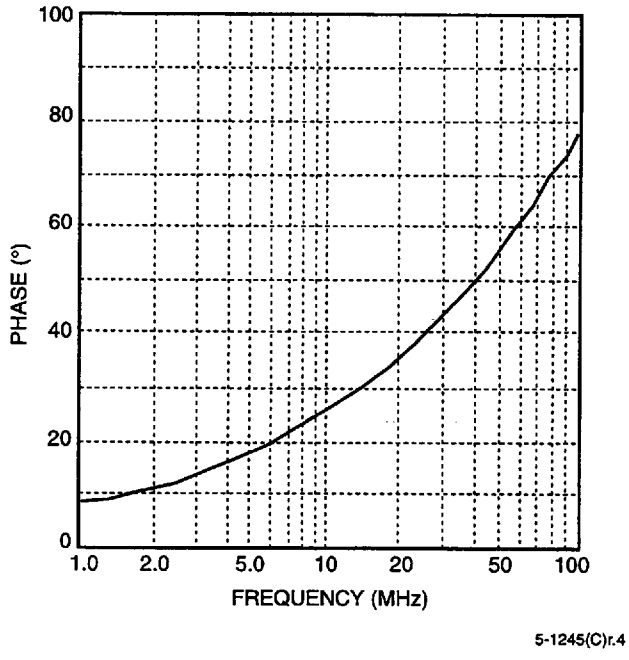


Figure 10. Phase Characteristic of 728A Coaxial Cable (450 ft.)

Timing Recovery

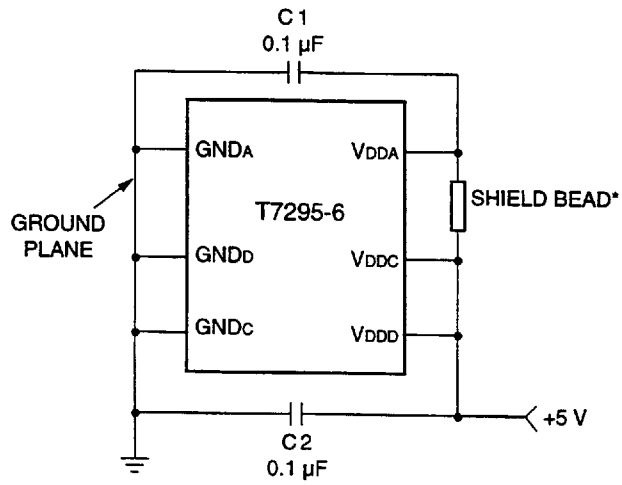
Output Jitter

The total jitter appearing on the RCLK output during normal operation consists of two components. First, some jitter appears on RCLK because of jitter on the incoming signal. (The next section discusses the jitter transfer characteristic, which describes the relationship between input and output jitter.) Second, noise sources, both within the T7295-6 device and those that are coupled into the device through the power supplies, and data pattern dependent jitter, due to misequalization of the input signal, all create jitter on RCLK. The magnitude of this internally generated jitter is a function of the PLL bandwidth, which, in turn, is a function of the input 1s density. For higher 1s densities, the amount of generated jitter decreases. Generated jitter also depends on the quality of the power supply bypassing networks used. Figure 11 shows the suggested bypassing network, and Table 8 lists the typical generated jitter performance achievable with this network.

Table 8. Generated Jitter and Jitter Transfer Characteristic

Parameter	Typ	Max	Unit
Generated Jitter*			
All-1s Pattern	1.0	—	ns pk-pk
Repetitive 100 Pattern	1.5	—	ns pk-pk
Jitter Transfer Characteristic†			
Peaking	0.05	0.1	dB
f3dB	205	—	kHz

* Repetitive input data pattern at nominal DSX-3 level with V_{DD} = 5 V, T_A = 25 °C.
† Repetitive 100 input at nominal DSX-3 level with V_{DD} = 5 V, T_A = 25 °C.



* Recommended shield beads are the *FairRite*† 2643000101 (through hole), or the *FairRite* 2743019446 (surface mount), or equivalents. 5-1246(C)r.4
† *FairRite* is a registered trademark of FairRite Products Corporation.

Figure 11. Recommended Power Supply Bypassing Network

Timing Recovery (continued)

Jitter Transfer Characteristic

The jitter transfer characteristic indicates the fraction of input jitter that reaches the RCLK output as a function of input jitter frequency. Table 8 shows important jitter transfer characteristic parameters. Figure 12 shows a typical characteristic, with the operating conditions as described in Table 8. Although existing standards do not specify jitter transfer characteristic requirements, the T7295-6 information is provided here to assist in evaluation of the device.

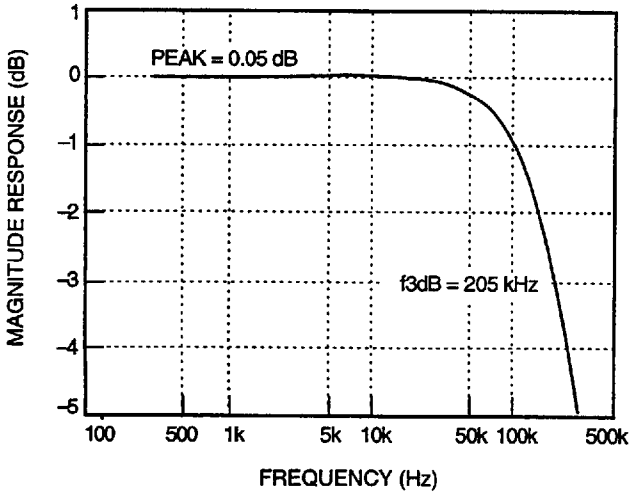


Figure 12. Typical PLL Jitter Transfer Characteristic

Jitter Accommodation

Under all allowable operating conditions, the jitter accommodation of the T7295-6 device exceeds all system requirements for error-free operation (BER < $1e^{-9}$) shown in Figure 13. The typical (V_{DD} = 5.0 V, T_A = 25 °C, DSX-3 nominal signal level) jitter accommodation of the T7295-6 is also shown in Figure 13. Table 9 shows the typical jitter tolerance for the T7295-6 at selected jitter frequencies.

Table 9. T7295-6 Typical Jitter Tolerance

Jitter Frequency (Hz)	Jitter Amplitude (U.I.)
5 k	10
10 k	5
60 k	1
300 k	0.5
1 M	0.4

Timing Recovery (continued)

Jitter Accommodation (continued)

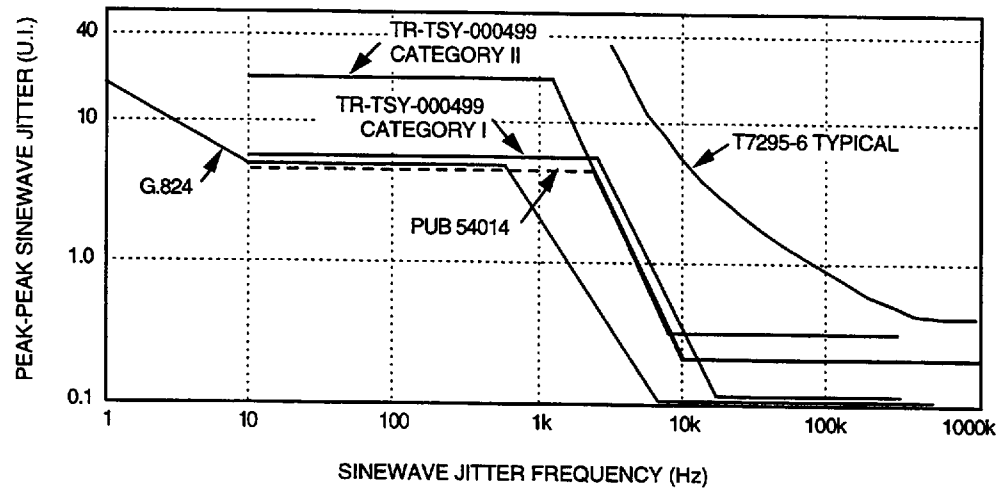


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Figure 13. Input Jitter Tolerance at Nominal DSX-3 Level

False Lock Immunity

False lock is defined as the condition where a PLL recovered clock obtains stable phase lock at a frequency not equal to the incoming data rate. The T7295-6 device uses a combination frequency/phase-lock architecture to prevent false lock. An on-chip frequency comparator continuously compares the EXCLK reference to the PLL clock. If the frequency difference between the EXCLK and PLL clock exceeds approximately ±0.5%, correction circuitry forces reacquisition of the proper frequency and phase.

Acquisition Time

If a valid input signal is already present at the receive input, the maximum time between the application of device power and error-free operation is 20 ms. If power has already been applied, the interval between the application of valid data (or the return of valid data following a loss of signal) and error-free operation is 4 ms.

Loss-of-Lock Detection

As stated above, the PLL acquisition aid circuitry monitors the PLL clock frequency relative to the EXCLK frequency. The RLOL alarm is activated if the difference between the PLL clock and the EXCLK frequency exceeds approximately ±0.5%. This will not occur until at least 250 bit periods after loss of input data.

A high RLOL output indicates that the acquisition circuit is working to bring the PLL into proper frequency lock. RLOL remains high until frequency lock has occurred; however, the minimum RLOL pulse width is 32 clock cycles.

Phase Hits

In response to a phase hit in the input data, the T7295-6 returns to error-free operation in less than 2 ms. During the reacquisition time, RLOS may temporarily be indicated.

Timing Recovery (continued)

Loss-of-Signal Detection

Figure 1 shows that analog and digital methods of loss-of-signal (LOS) detection are combined to create the RLOS alarm output. RLOS is set if either the analog or digital detection circuitry indicates that LOS has occurred.

Analog Detection

The analog LOS detector monitors the peak input signal amplitude. RLOS makes a high-to-low transition (input signal regained) when the input signal amplitude exceeds the loss-of-signal threshold defined in Table 10. The RLOS low-to-high transition (input signal lost) occurs at a level typically 1.0 dB below the high-to-low transition level. This hysteresis prevents RLOS chattering. Once set, the RLOS alarm remains high for at least 32 clock cycles, allowing for system detection of a loss-of-signal condition without the use of an external latch.

To allow for varying levels of noise and crosstalk in different applications, three loss-of-signal threshold settings are available using the LOSTHR pin. Setting LOSTHR = V_{DD} provides the lowest loss-of-signal threshold; LOSTHR = $V_{DD}/2$ (can be produced by using two 50 kΩ ± 10% resistors as a voltage divider between V_{DDD} and GND_D) provides an intermediate threshold; and LOSTHR = GND provides the highest threshold. The LOSTHR pin must be set to its desired value at powerup and must not be changed during operation.

Digital Detection

In addition to the signal amplitude monitoring of the analog LOS detector, the digital LOS detector monitors the recovered data 1s density. The RLOS alarm goes high if 160 ± 32 or more consecutive 0s occur in the receive data stream. The alarm goes low when at least ten 1s occur in a string of 32 consecutive bits. This hysteresis minimizes RLOS chattering and guarantees a minimum RLOS pulse width of 32 clock cycles.

Note, however, that RLOS chatter can still occur. When REQB = 1, input signal levels above the analog RLOS threshold can still be low enough to result in a high bit error rate. The resultant data stream (containing) errors can temporarily activate the digital LOS detector, and RLOS chatter can occur. Therefore, RLOS should not be used as a bit error rate monitor.

RLOS chatter can also occur when RLOL is activated (high).

Table 10. Analog Loss-of-Signal Thresholds (RLOS High-to-Low Transition Threshold)

Data Rate	REQB	LOSTHR	Min Threshold	Max Threshold	Unit
DS3	0	0	60	220	mV pk
		$V_{DD}/2$	40	145	mV pk
		V_{DD}	25	90	mV pk
	1	0	45	175	mV pk
		$V_{DD}/2$	30	115	mV pk
		V_{DD}	20	70	mV pk
STS-1	0	0	75	275	mV pk
		$V_{DD}/2$	50	185	mV pk
		V_{DD}	30	115	mV pk
	1	0	55	220	mV pk
		$V_{DD}/2$	35	145	mV pk
		V_{DD}	25	90	mV pk

Notes:
The RLOS alarm is an indication of the presence of an input signal, not a bit error rate indication. Table 2 gives the minimum input amplitude needed for error-free operation (BER < 1 e^{-9}). Independent of the RLOS state, the device will attempt to recover correct timing and data.

The RLOS low-to-high transition typically occurs 1 dB below the high-to-low transition.

Timing Recovery (continued)

Recovered Clock and Data Timing

Table 14 and Figure 14 summarize the timing relationships between the high-speed logic signals RCLK, RPDATA, and RNDATA. The duty cycle is referenced to a $V_{DD}/2$ threshold level. RPDATA and RNDATA change on the rising edge of RCLK and are valid during the falling edge of RCLK. A positive pulse at the T7295-6 input creates a high level on RPDATA and a low level on RNDATA. A negative pulse creates a high level on RNDATA and a low level on RPDATA, and a received zero produces low levels on both RPDATA and RNDATA.

In-Circuit Test Capability

When pulled low, the $\overline{ICT}$ pin forces all digital output buffers (RCLK, RPDATA, RNDATA, RLOS, RLOL pins) into a high output impedance state. This feature allows in-circuit testing to be done on neighboring devices without concern for T7295-6 device buffer damage. When forced high, the $\overline{ICT}$ pin does not affect device operation. An internal pull-up device (nominally 50 kΩ) is provided on this pin; therefore, users can leave this pin unconnected for normal operation. Test equipment can pull $\overline{ICT}$ low during in-circuit testing without damaging the device. This is the only pin for which internal pull-up/pull-down is provided.

Board Layout Considerations

Power Supply Bypassing

Figure 11 illustrates the recommended power supply bypassing network. A 0.1 µF (C2) capacitor bypasses the digital supplies. The analog supply V_{DDA} is bypassed by using a 0.1 µF (C1) capacitor and a shield bead that removes significant amounts of high-frequency noise generated by the system and by the device logic. Good-quality, high-frequency (low lead inductance) capacitors should be used. Finally, it is most important that all ground connections be made to a low-impedance ground plane.

Receive Input

The connections to the receive input pin must be carefully considered. Noise coupling must be minimized along the path from the signal entering the board to the input pin. Any noise coupled into the T7295-6 input directly degrades the signal-to-noise ratio of the input signal and may degrade sensitivity.

PLL Filter Capacitor

The PLL filter capacitor between pins LPF1 and LPF2 must be placed as close to the chip as possible (within 0.5 inches is recommended). The LPF1 and LPF2 pins are adjacent, allowing for short-lead lengths with no crossovers to the external capacitor. Noise coupling into the LPF1 and LPF2 pins may degrade PLL performance. A ceramic capacitor with the value 0.1 µF ± 20% is acceptable.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability. External leads can be soldered safely at temperatures up to 300 °C.

Parameter	Symbol	Min	Max	Unit
dc Supply Voltage Range	V_{DD}	–0.5	6.5	V
Power Dissipation, Package Limit	P_D	—	700	mW
Storage Temperature Range	T_{stg}	–40	125	°C

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent Technologies Microelectronics Group employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters:

HBM ESD Threshold	
Device	**Voltage**
T7295-6	>1000 V

Electrical Characteristics

Table 11. Logic Interface Characteristics

–40 °C ≤ T_A ≤ +85 °C, V_{DD} = 5 V ± 10%

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Voltage: Low High	 V_{IL} V_{IH}	 — —	 GND_D 0.7V_{DDD}	 0.5 V_{DDD}	 V V
Input Leakage	I_L	–0.5 to V_{DD} + 0.5 V (all input pins except 2 and 17) Pin 17, 0 V Pin 2, V_{DD} Pin 2, GND_D	–10 20 10 –50	10 500 100 –5	µA µA µA µA
Output Voltage: Low High	 V_{OL} V_{OH}	 –5.0 mA 5.0 mA	 GND_D V_{DDD} – 0.5	 0.4 V_{DDD}	 V V
Input Capacitance	C_I	—	—	10	pF
Load Capacitance	C_L	—	—	10	pF

Electrical Characteristics (continued)

Table 12. Power Dissipation

T_A = –40 °C to +85 °C, V_{DD} = 5 V ± 10%

Typical values are for V_{DD} = 5.0 V, 25 °C, and random data.

Maximum values are for V_{DD} = 5.5 V, all-1s data.

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Current	I_{DD}				
DS3					
REQB = 0		—	82	106	mA
REQB = 1		—	79	103	mA
STS-1					
REQB = 0		—	87	111	mA
REQB = 1		—	83	108	mA

Timing Characteristics

Table 13. External Reference Clock Requirements

Parameter	Min	Typ	Max	Unit
Rise and Fall Time (10% to 90%)	—	—	5.0	ns
Duty Cycle (at V_{DD}/2)	40	—	60	%

Table 14. System Interface Timing Characteristics (See Figure 14.)

T_A = –40 °C to +85 °C, V_{DD} = 5 V ± 10%

All timing characteristics are measured with 10 pF loading.

Symbol	Parameter	Min	Typ	Max	Unit
tRCH1RCH2	Receive Clock Rise Time (10% to 90%)	—	—	3.5	ns
tRCL2RCL1	Receive Clock Fall Time (10% to 90%)	—	—	2.5	ns
tRDVRCL	Receive Data Setup Time	5.0	—	—	ns
tRCLRDX	Receive Data Hold Time	8.5	—	—	ns
tRCHRDV	Receive Propagation Delay	0.6	—	3.7	ns
—	Receive Clock Duty Cycle	45	50	55	%

Note: The propagation delay from the analog input RIN to the system data outputs RPDATA/RNDATA is 3.5 RCLK cycles for both the DS3 and STS-1 data rates.

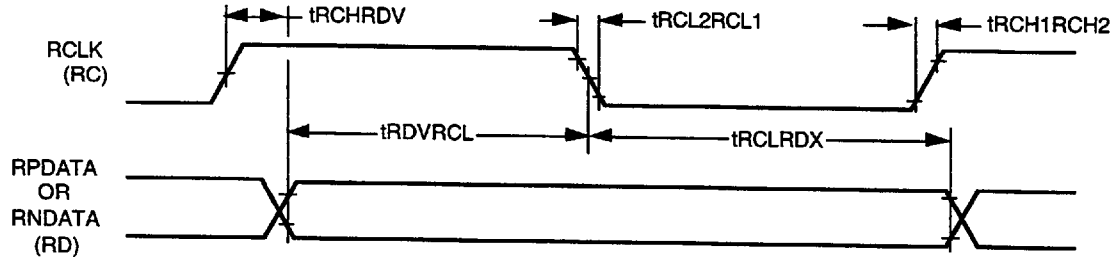

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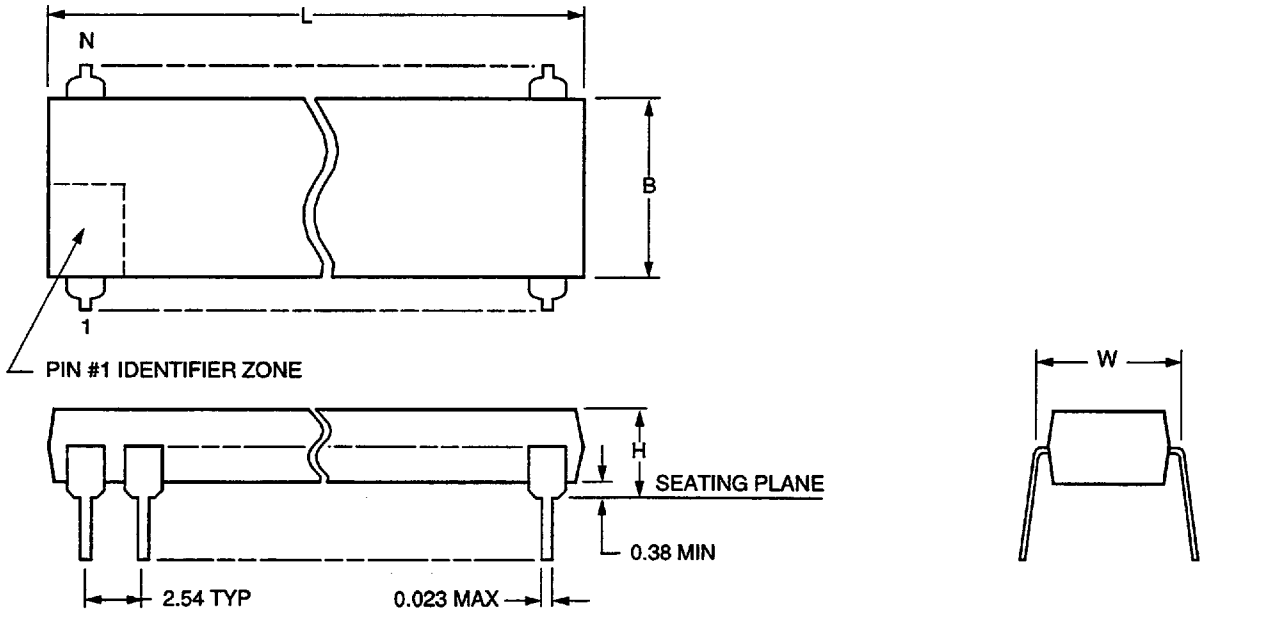
Figure 14. Timing Diagram for System Interface

Outline Diagrams

20-Pin, Plastic DIP

Dimensions are in millimeters.

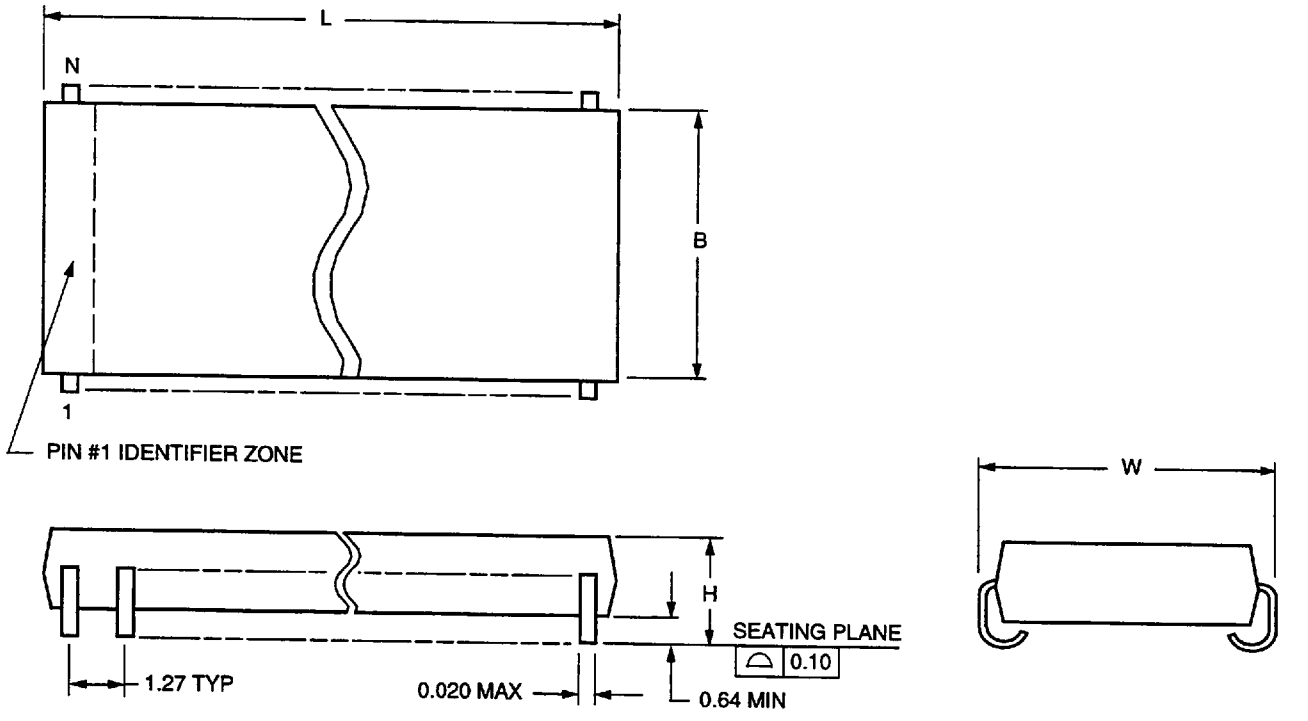


Number of Pins (N)	Package Dimensions (DIP)			
	Maximum Length (L)	Maximum Width Without Leads (B)	Maximum Width Including Leads (W)	Maximum Height Above Board (H)
20	26.42	6.48	7.87	5.08

Outline Diagrams (continued)

20-Pin, Plastic SOJ

Dimensions are in millimeters.



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Number of Pins (N)	Package Dimensions (SOJ)			
	Maximum Length (L)	Maximum Width Without Leads (B)	Maximum Width Including Leads (W)	Maximum Height Above Board (H)
20	12.95	7.62	8.81	3.18

Ordering Information

Device Code	Package	Temperature	Comcode (Ordering Number)
T - 7295 - - 6EL	20-Pin, Plastic SOJ	–40 °C to +85 °C	106601255
T - 7295 - - 6PL	20-Pin, Plastic DIP	–40 °C to +85 °C	106601248

Standards Documentation

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.)

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
FAX: 212-302-1286

AT&T Publications

AT&T Customer Information Center (CIC)

Tel: 800-432-6600
FAX: 800-566-9568 (in U.S.A.)
FAX: 317-322-6484 (outside U.S.A.)

Bellcore (U.S.A.)

Bellcore Customer Service
8 Corporate Plaza
Piscataway, New Jersey 08854

Tel: 800-521-CORE (in U.S.A.)
Tel: 908-699-5800
FAX: 212-302-1286

ITU-T

International Telecommunication Union-
Telecommunication Sector
Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285
FAX: 41-22-730-5991

ETSI

European Telecommunications Standards Institute
BP 152
F-06561 Valbonne Cedex, France

Tel: 33-92-94-42-00
FAX: 33-93-65-47-16

TTC (Japan)

TTC Standard Publishing Group of the
Telecommunications Technology Committee
2nd Floor, Hamamatsucho-Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
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