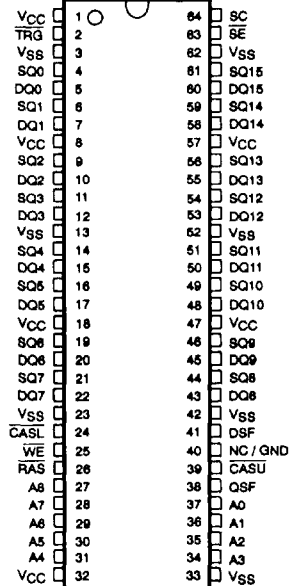


- **Organization:**
  - DRAM: 262 144 Words × 16 Bits
  - SAM: 256 Words × 16 Bits
- **Dual-Port Accessibility – Simultaneous and Asynchronous Access From the DRAM and SAM Ports**
- **Data-Transfer Function From the DRAM to the Serial-Data Register**
- **(4 × 4) × 4 Block-Write Feature for Fast Area-Fill Operations; as Many as Four Memory-Address Locations Written Per Cycle From the 16-Bit On-Chip Color Register**
- **Write-Per-Bit Feature for Selective Write to Each RAM I/O; Two Write-Per-Bit Modes to Simplify System Design**
- **Byte Write Control ( $\overline{\text{CASL}}$ ,  $\overline{\text{CASU}}$ ) Provides Flexibility**
- **Extended Data Output for Faster System Cycle Time**
- **Enhanced Page-Mode Operation for Faster Access**
- **$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$  (CBR) and Hidden-Refresh Modes**
- **Long Refresh Period Every 8 ms (Max)**
- **Up to 45-MHz Uninterrupted Serial-Data Streams**
- **256 Selectable Serial-Register Starting Locations**
- **$\overline{\text{SE}}$ -Controlled Register-Status QSF**
- **Split-Register-Transfer Read for Simplified Real-Time Register Load**
- **Programmable Split-Register Stop Point**
- **3-State Serial Outputs Allow Easy Multiplexing of Video-Data Streams**
- **All Inputs/Outputs and Clocks TTL Compatible**
- **Compatible With JEDEC Standards**
- **Performance Ranges:**

**HKC PACKAGE**  
(TOP VIEW)



PIN NOMENCLATURE	
A0–A8	Address Inputs
$\overline{\text{CASL}}$ , $\overline{\text{CASU}}$	Column-Address Strobe/Byte Selects
DQ0–DQ15	DRAM Data I/O, Write Mask Data
DSF	Special-Function Select
NC/GND	No Connect/Ground (Important: Not connected internally to VSS)
QSF	Special-Function Output
$\overline{\text{RAS}}$	Row-Address Strobe
SC	Serial Clock
$\overline{\text{SE}}$	Serial Enable
SQ0–SQ15	Serial-Data Output
TRG	Output Enable, Transfer Select
VCC	5-V Supply (TYP)
VSS	Ground
WE	DRAM Write-Enable Select

- **Texas Instruments EPIC™ Process**
- **Designed to Work With the Texas Instruments Graphics Family**

	ACCESS TIME ROW ENABLE	ACCESS TIME SERIAL DATA	DRAM CYCLE TIME	DRAM PAGE MODE	SERIAL CYCLE TIME	OPERATING CURRENT SERIAL PORT STANDBY	OPERATING CURRENT SERIAL PORT ACTIVE
	$t_{\text{a}}(\text{R})$ (MAX)	$t_{\text{a}}(\text{SQ})$ (MAX)	$t_{\text{c}}(\text{W})$ (MIN)	$t_{\text{c}}(\text{P})$ (MIN)	$t_{\text{c}}(\text{SC})$ (MIN)	$I_{\text{CC1}}$ (MAX)	$I_{\text{CC1A}}$ (MAX)
SMJ55161-70	70 ns	20 ns	130 ns	45 ns	22 ns	165 mA	210 mA
SMJ55161-80	80 ns	25 ns	150 ns	50 ns	30 ns	160 mA	195 mA

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



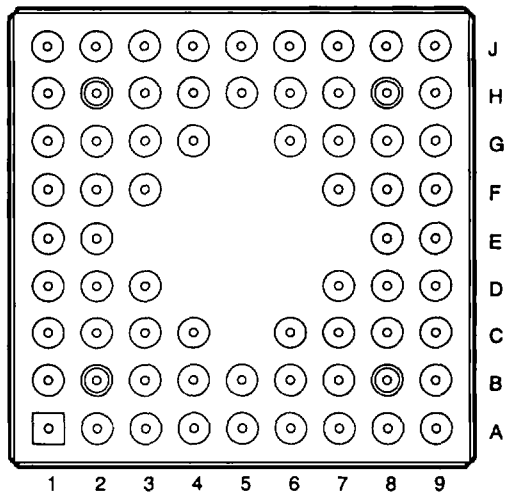
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**SMJ55161**  
**262144 BY 16-BIT**  
**MULTIPOINT VIDEO RAM**  
SGMS056A - MAY 1995 - REVISED JUNE 1995

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**GB PACKAGE**  
**(BOTTOM VIEW)**



**GB Package Pin Assignments - By Location**

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME						
J1	DQ1	J2	SQ3	J3	DQ3	J4	DQ4	J5	DQ5	J6	DQ6	J7	SQ7	J8	CASL	J9	A8
H1	DQ0	H2	SQ2	H3	DQ2	H4	SQ4	H5	SQ5	H6	SQ6	H7	DQ7	H8	WE	H9	A7
G1	SQ0	G2	SQ1	G3	VDD2	G4	VSS2			G6	VDD2	G7	VSS2	G8	RAS	G9	A6
F1	TRG	F2	VSS1	F3	VDD1					F7	VDD1	F8	VDD1	F9	A5		
E1	SC	E2	VDD1									E8	VSS1	E9	A4		
D1	SE	D2	VSS1	D3	VDD1					D7	VSS1	D8	A3	D9	A2		
C1	SQ15	C2	VSS1	C3	VDD2	C4	VSS2			C6	VDD2	C7	VSS2	C8	CASU	C9	A1
B1	DQ15	B2	DQ14	B3	DQ13	B4	DQ12	B5	DQ11	B6	DQ10	B7	SQ8	B8	DSF	B9	A0
A1	SQ14	A2	SQ13	A3	SQ12	A4	SQ11	A5	SQ10	A6	SQ9	A7	DQ9	A8	DQ8	A9	QSF

**GB Package Pin Assignments - By Signal**

PIN		PIN		PIN		PIN		PIN		PIN	
NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.
A0	B9	DQ1	J1	DQ12	B4	SQ2	H2	SQ13	A2	VDD2	G6
A1	C9	DQ2	H3	DQ13	B3	SQ3	J2	SQ14	A1	VDD2	C6
A2	D9	DQ3	J3	DQ14	B2	SQ4	H4	SQ15	C1	VSS1	F2
A3	D8	DQ4	J4	DQ15	B1	SQ5	H5	TRG	F1	VSS1	D2
A4	E9	DQ5	J5	DSF	B8	SQ6	H6	VDD1	E2	VSS1	C2
A5	F9	DQ6	J6	QSF	A9	SQ7	J7	VDD1	F3	VSS1	D7
A6	G9	DQ7	H7	RAS	G8	SQ8	B7	VDD1	D3	VSS1	E8
A7	H9	DQ8	A8	SC	E1	SQ9	A6	VDD1	F7	VSS2	G4
A8	J9	DQ9	A7	SE	D1	SQ10	A5	VDD1	F8	VSS2	C4
CASL	J8	DQ10	B8	SQ0	G1	SQ11	A4	VDD2	G3	VSS2	G7
CASU	C8	DQ11	B5	SQ1	G2	SQ12	A3	VDD2	C3	VSS2	C7
DQ0	H1									WE	H8



**SMJ55161**  
**262 144 BY 16-BIT**  
**MULTIPORT VIDEO RAM**  
SGMS056A – MAY 1995 – REVISED JUNE 1995

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**description**

The SMJ55161 multiport video RAM is a high-speed, dual-port memory device. It consists of a dynamic random-access memory (DRAM) organized as 262 144 words of 16 bits each interfaced to a serial-data register (serial-access memory (SAM)) organized as 256 words of 16 bits each. The SMJ55161 supports three basic types of operation: random access to and from the DRAM, serial access from the serial register, and transfer of data from any row in the DRAM to the serial register. Except during transfer operations, the SMJ55161 can be accessed simultaneously and asynchronously from the DRAM and SAM ports.

The SMJ55161 is equipped with several features designed to provide higher system-level bandwidth and to simplify design integration on both the DRAM and SAM ports. On the DRAM port, greater pixel draw rates are achieved by the device's  $(4 \times 4) \times 4$  block-write feature. The block-write mode allows 16 bits of data (present in an on-chip color-data register) to be written to any combination of four adjacent column-address locations. As many as 64 bits of data can be written to memory during each  $\overline{\text{CAS}}$  cycle time. Also on the DRAM port, a write mask or a write-per-bit feature allows masking of any combination of the 16 inputs/outputs on any write cycle. The persistent write-per-bit feature uses a mask register that, once loaded, can be used on subsequent write cycles without reloading. The SMJ55161 also offers byte control. Byte control can be applied in read cycles, write cycles, block-write cycles, load-write-mask-register cycles, and load-color-register cycles. The SMJ55161 also offers extended-data output mode. The extended-data output mode is effective in both the page-mode and standard DRAM cycles.

The SMJ55161 offers a split-register-transfer read (DRAM-to-SAM) feature for the serial register (SAM port). This feature enables real-time register load implementation for continuous serial-data streams without critical timing requirements. The register is divided into a high half and a low half. While one half is being read out of the SAM port, the other half can be loaded from the memory array. For applications not requiring real-time register load (for example, loads done during CRT-retrace periods), the full-register mode of operation is retained to simplify system design.

The SAM port is designed for maximum performance. Data can be accessed from the SAM at serial rates up to 45 MHz. During the split-register-transfer read operations, internal circuitry detects when the last bit position is accessed from the active half of the register and immediately transfers control to the opposite half. A separate output, QSF, is included to indicate which half of the serial register is active.

All inputs, outputs, and clock signals on the SMJ55161 are compatible with Series 74 TTL. All address lines and data-in lines are latched on-chip to simplify system design. All data-out lines are unlatched to allow greater system flexibility.

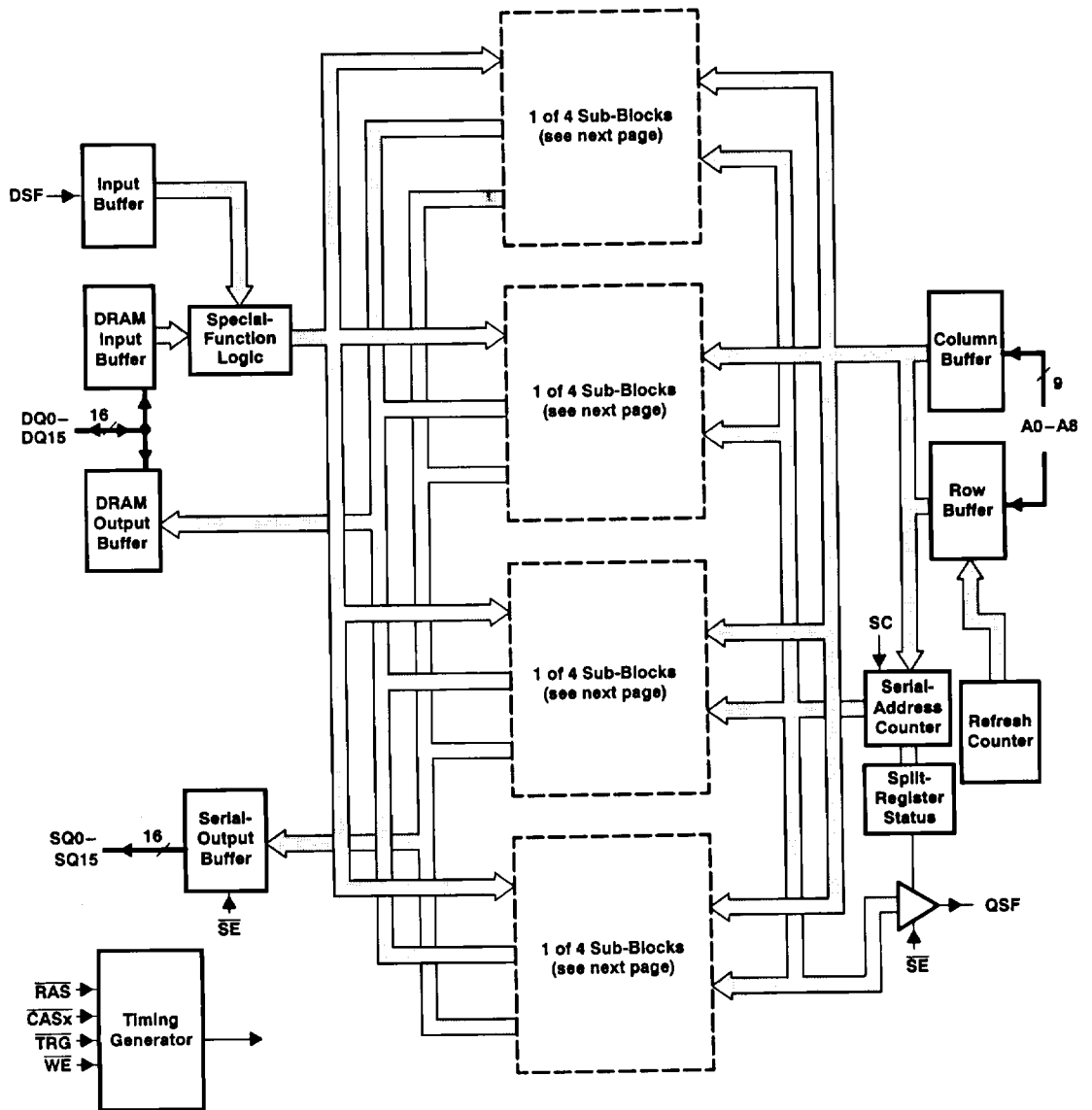
The SMJ55161 employs state-of-the-art Texas Instruments (TI) enhanced performance implanted CMOS (EPIC™) scaled-CMOS, double-level polysilicon/polycide gate technology combining very high performance with improved reliability.

The SMJ55161 is offered in a 68-pin ceramic pin-grid-array package (GB suffix) and a 64-pin ceramic flatpack (HKC suffix).

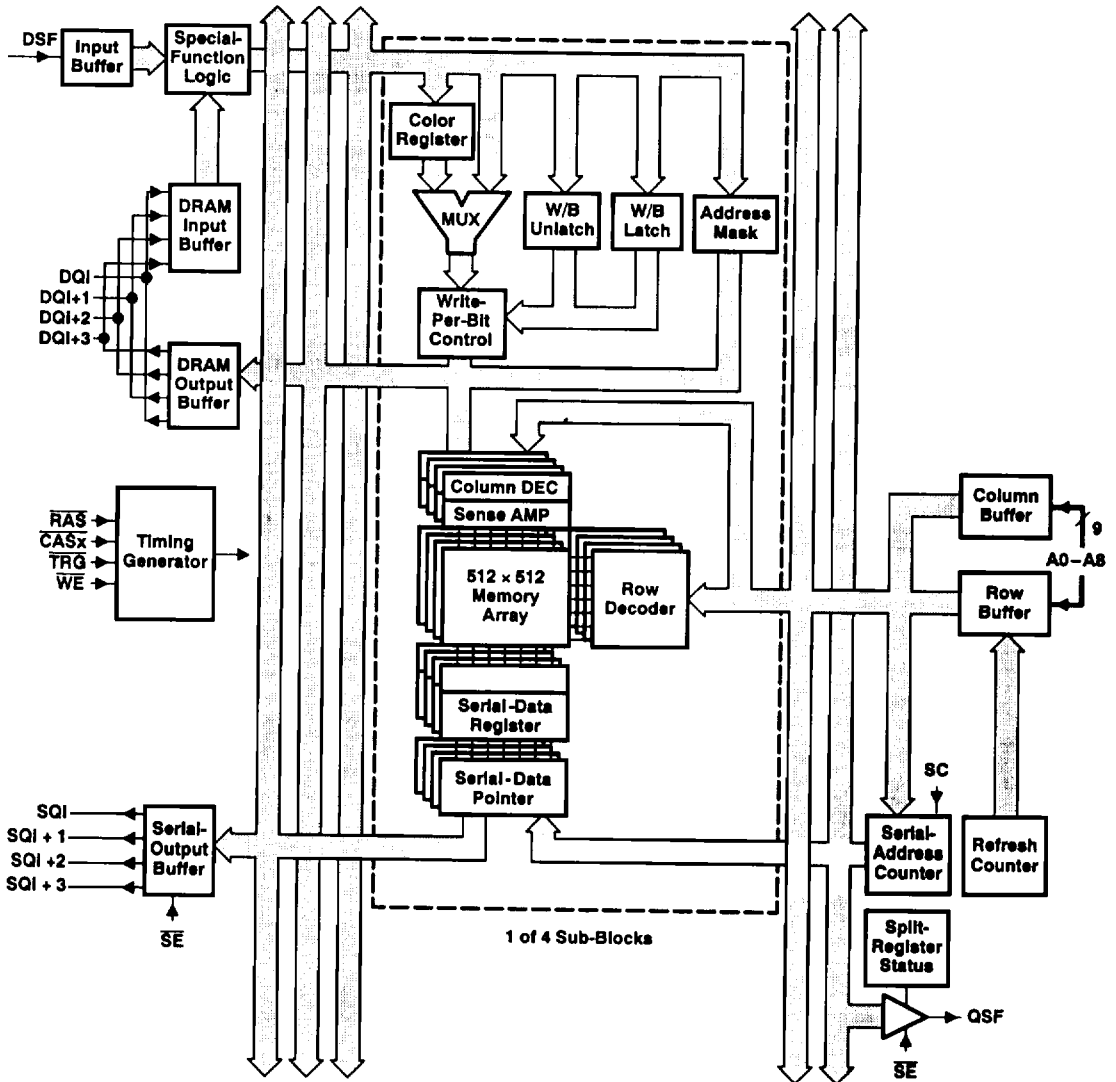
The SMJ55161 and other TI multiport video RAMs are supported by a broad line of graphic processors and control devices from TI. Refer to Tables 1 and 2 for additional function and description information.



functional block diagram



functional block diagram (continued)



**Function Table**

FUNCTION	RAS FALL				CASx FALL	ADDRESS		DQ0-DQ15†		MNE CODE
	CASx‡	TRG	WE	DSF	DSF	RAS	CASx§	RAS	CASL CASU WE	
Reserved (do not use)	L	L	L	L	X	X	X	X	X	—
CBR refresh (no reset) and stop-point set¶	L	X	L	H	X	Stop Point#	X	X	X	CBRS
CBR refresh (option reset)	L	X	H	L	X	X	X	X	X	CBR
CBR refresh (no reset)*	L	X	H	H	X	X	X	X	X	CBRN
Full-register-transfer read	H	L	H	L	X	Row Addr	Tap Point	X	X	RT
Split-register-transfer read	H	L	H	H	X	Row Addr	Tap Point	X	X	SRT
DRAM write (nonpersistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	Write Mask	Valid Data	RWM
DRAM block write (nonpersistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2-A8	Write Mask	Col Mask	BWM
DRAM write (persistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	X	Valid Data	RWM
DRAM block write (persistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2-A8	X	Col Mask	BWM
DRAM write (nonmasked)	H	H	H	L	L	Row Addr	Col Addr	X	Valid Data	RW
DRAM block write (nonmasked)	H	H	H	L	H	Row Addr	Block Addr A2-A8	X	Col Mask	BW
Load write-mask register□	H	H	H	H	L	Refresh Addr	X	X	Write Mask	LMR
Load color register	H	H	H	H	H	Refresh Addr	X	X	Color Data	LCR

**Legend:**

- Col Mask = H: Write to address/column enabled
- Write Mask = H: Write to I/O enabled
- X = Don't care

† DQ0-DQ15 are latched on either the first falling edge of CASx or the falling edge of WE, whichever occurs later.

‡ Logic L is selected when either or both CASL and CASU are low.

§ The column address and block address are latched on the first falling edge of CASx.

¶ CBRs cycle should be performed immediately after the powerup initialization cycle.

# A0-A3, A8: don't care; A4-A7: stop-point code

|| CBR refresh (option reset) mode ends persistent write-per-bit mode and stop-point mode.

\* CBR refresh (no reset) mode does not end persistent write-per-bit mode or stop-point mode.

□ Load-write-mask-register cycle sets the persistent write-per-bit mode. The persistent write-per-bit mode is reset only by the CBR (option reset) cycle.



Table 1. Pin Description Versus Operational Mode

PIN	DRAM	TRANSFER	SAM
A0 – A8	Row, column address	Row address, tap point	
$\overline{\text{CASL}}$ $\overline{\text{CASU}}$	Column-address strobe, DQ output enable	Tap-address strobe	
DQ	DRAM data I/O, write mask		
DSF	Block-write enable Write-mask-register load enable Color-register load enable CBR (option reset)	Split-register-transfer enable	
$\overline{\text{RAS}}$	Row-address strobe	Row-address strobe	
$\overline{\text{SE}}$			SQ output enable, QSF output enable
SC			Serial clock
SQ			Serial-data output
$\overline{\text{TRG}}$	DQ output enable	Transfer enable	
$\overline{\text{WE}}$	Write enable, write-per-bit enable		
QSF			Serial-register status
NC/GND	Either make no external connection or tie to system GND ( $V_{SS}$ )		
$V_{CC}^{\dagger}$	5-V supply		
$V_{SS}^{\dagger}$	Ground		

† For proper device operation, all  $V_{CC}$  pins must be connected to a 5-V supply, and all  $V_{SS}$  pins must be tied to ground.

## pin definitions

### address (A0–A8)

Eighteen address bits are required to decode one of 262 144 storage cell locations. Nine row-address bits are set up on pins A0–A8 and latched onto the chip on the falling edge of  $\overline{\text{RAS}}$ . Nine column-address bits are set up on pins A0–A8 and latched onto the chip on the first falling edge of  $\overline{\text{CASx}}$ . All addresses must be stable on or before the falling edge of  $\overline{\text{RAS}}$  and the first falling edge of  $\overline{\text{CASx}}$ .

During the full-register-transfer read operation, the states of A0–A8 are latched on the falling edge of  $\overline{\text{RAS}}$  to select one of the 512 rows where the transfer occurs. At the first falling edge of  $\overline{\text{CASx}}$ , the column-address bits A0–A8 are latched. The most significant column-address bit (A8) selects which half of the row is transferred to the SAM. The appropriate 8-bit column address (A0–A7) selects one of 256 tap points (starting positions) for the serial-data output.

During the split-register-transfer read operation, address bit A7 is ignored at the falling edge of  $\overline{\text{CASx}}$ . An internal counter selects which half of the register is used. If the high half of the SAM is currently in use, the low half of the SAM is loaded with the low half of the DRAM half row and vice versa. Column address (A8) selects the DRAM half row. The remaining seven address bits (A0–A6) are used to select one of 127 possible starting locations within the SAM. Locations 127 and 255 are not valid tap points.

### row-address strobe ( $\overline{\text{RAS}}$ )

$\overline{\text{RAS}}$  is similar to a chip enable so that all DRAM cycles and transfer cycles are initiated by the falling edge of  $\overline{\text{RAS}}$ .  $\overline{\text{RAS}}$  is a control input that latches the states of the row address,  $\overline{\text{WE}}$ ,  $\overline{\text{TRG}}$ ,  $\overline{\text{CASL}}$ ,  $\overline{\text{CASU}}$ , and DSF onto the chip to invoke DRAM and transfer-read functions of the SMJ55161.



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#### column-address strobe ( $\overline{\text{CASL}}$ , $\overline{\text{CASU}}$ )

$\overline{\text{CASL}}$  and  $\overline{\text{CASU}}$  are control inputs that latch the states of the column address and DSF to control DRAM and transfer functions of the SMJ55161.  $\overline{\text{CASx}}$  also act as output enables for the DRAM output pins DQ0–DQ15. In DRAM operation,  $\overline{\text{CASL}}$  enables data to be written to or read from the lower byte (DQ0–DQ7), and  $\overline{\text{CASU}}$  enables data to be written to or from the upper byte (DQ8–DQ15). In transfer operations, address bits A0–A8 are latched at the first falling edge of  $\overline{\text{CASx}}$  as the start position (tap) for the serial-data output (SQ0–SQ15).

#### output enable/transfer select ( $\overline{\text{TRG}}$ )

$\overline{\text{TRG}}$  selects either DRAM or transfer operation as  $\overline{\text{RAS}}$  falls. For DRAM operation,  $\overline{\text{TRG}}$  must be held high as  $\overline{\text{RAS}}$  falls. During DRAM operation,  $\overline{\text{TRG}}$  functions as an output enable for the DRAM output pins DQ0–DQ15. For transfer operation,  $\overline{\text{TRG}}$  must be brought low before  $\overline{\text{RAS}}$  falls.

#### write-mask select, write enable ( $\overline{\text{WE}}$ )

In DRAM operation,  $\overline{\text{WE}}$  enables data to be written to the DRAM.  $\overline{\text{WE}}$  is also used to select the DRAM write-per-bit mode. Holding  $\overline{\text{WE}}$  low on the falling edge of  $\overline{\text{RAS}}$  invokes the write-per-bit operation. The SMJ55161 supports both the nonpersistent write-per-bit mode and the persistent write-per-bit mode.

#### special-function select (DSF)

The DSF input is latched on the falling edge of  $\overline{\text{RAS}}$  or the first falling edge of  $\overline{\text{CASx}}$ , similar to an address. DSF determines which of the following functions are invoked on a particular cycle:

- CBR refresh with reset (CBR)
- CBR refresh with no reset (CBRN)
- CBR refresh with no reset and stop-point set (CBRS)
- Block write
- Loading write-mask register for the persistent write-per-bit mode (LMR)
- Loading color register for the block-write mode
- Split-register-transfer read

#### DRAM data I/O, write mask data (DQ0–DQ15)

DRAM data is written or read through the common I/O DQ pins. The 3-state DQ-output buffers provide direct TTL compatibility (no pullup resistors) with a fanout of one Series 54 TTL load. Data out is the same polarity as data in. During a normal access cycle, the outputs remain in the high-impedance state until  $\overline{\text{TRG}}$  is brought low. Data appears at the outputs until  $\overline{\text{TRG}}$  returns high,  $\overline{\text{CASx}}$  returns high following  $\overline{\text{RAS}}$  returning high, or  $\overline{\text{RAS}}$  returns high following  $\overline{\text{CASx}}$  returning high. The write mask is latched into the device via the random DQ pins by the falling edge of  $\overline{\text{RAS}}$  and is used on all write-per-bit cycles. In a transfer operation, the DQ outputs remain in the high-impedance state for the entire cycle.

#### serial-data outputs (SQ0–SQ15)

Serial data is read from the SQ pins. The SQ output buffers provide direct TTL compatibility (no pullup resistors) with a fanout of one Series 54 TTL load. The serial outputs are in the high-impedance (floating) state as long as the serial-enable pin,  $\overline{\text{SE}}$ , is high. The serial outputs are enabled when  $\overline{\text{SE}}$  is brought low.

#### serial clock (SC)

Serial data is accessed out of the data register from the rising edge of SC. The SMJ55161 is designed to work with a wide range of clock duty cycles to simplify system design. There is no refresh requirement because the data registers that comprise the SAM are static. There is also no minimum SC-clock operating frequency.

**serial enable ( $\overline{SE}$ )**

During serial-access operations,  $\overline{SE}$  is used as an enable/disable for the SQ outputs.  $\overline{SE}$  low enables the serial-data output.  $\overline{SE}$  high disables the serial-data output.  $\overline{SE}$  is also used as an enable/disable for output pin QSF.

**IMPORTANT:** While  $\overline{SE}$  is held high, the serial clock is not disabled. External SC pulses increment the internal serial-address counter regardless of the state of  $\overline{SE}$ . This ungated serial-clock scheme minimizes access time of serial output from  $\overline{SE}$  low because the serial-clock input buffer and the serial-address counter are not disabled by  $\overline{SE}$ .

**special-function output (QSF)**

QSF is an output pin that indicates which half of the SAM is being accessed. When QSF is low, the serial-address pointer is accessing the lower (least significant) 128 bits of the serial register (SAM). When QSF is high, the pointer is accessing the higher (most significant) 128 bits of the SAM.

During full-register-transfer operations, QSF can change state upon completing the cycle. This state is determined by the tap point loaded during the transfer cycle. QSF is enabled by  $\overline{SE}$ . If  $\overline{SE}$  is high, the QSF output is in the high-impedance state.

**no connect / ground (NC/GND)**

NC/GND should be tied to system ground or left floating for proper device operation.

functional operation description

random access operation

DRAM Function Table

FUNCTION	RAS FALL				CASx FALL	ADDRESS		DQ0–DQ15†		MNE CODE
	CASx‡	TRG	WE	DSF	DSF	RAS	CASx§	RAS	CASL CASU WE	
Reserved (do not use)	L	L	L	L	X	X	X	X	X	—
CBR refresh (no reset) and stop-point set¶	L	X	L	H	X	Stop Point#	X	X	X	CBRS
CBR refresh (option reset)	L	X	H	L	X	X	X	X	X	CBR
CBR refresh (no reset)*	L	X	H	H	X	X	X	X	X	CBRN
DRAM write (nonpersistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	Write Mask	Valid Data	RWM
DRAM block write (nonpersistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	Write Mask	Col Mask	BWM
DRAM write (persistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	X	Valid Data	RWM
DRAM block write (persistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BWM
DRAM write (nonmasked)	H	H	H	L	L	Row Addr	Col Addr	X	Valid Data	RW
DRAM block write (nonmasked)	H	H	H	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BW
Load write-mask register □	H	H	H	H	L	Refresh Addr	X	X	Write Mask	LMR
Load color register	H	H	H	H	H	Refresh Addr	X	X	Color Data	LCR

Legend:

- Col Mask = H: Write to address/column enabled
- Write Mask = H: Write to I/O enabled
- X = Don't care

† DQ0–DQ15 are latched on either the first falling edge of CASx or the falling edge of WE, whichever occurs later.

‡ Logic L is selected when either or both CASL and CASU are low.

§ The column address and block address are latched on the first falling edge of CASx.

¶ CBR cycle should be performed immediately after the power-up initialization cycle.

# A0–A3, A8: don't care; A4–A7: stop-point code

|| CBR refresh (option reset) mode ends persistent write-per-bit mode and stop-point mode.

\* CBR refresh (no reset) mode does not end persistent write-per-bit mode or stop-point mode.

□ Load-write-mask-register cycle sets the persistent write-per-bit mode. The persistent write-per-bit mode is reset only by the CBR (option reset) cycle.



#### enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. This mode eliminates the time required for row-address setup, row-address hold, and address multiplex. The maximum  $\overline{RAS}$  low time and  $\overline{CAS}$  page cycle time used determines the number of columns that can be accessed.

Unlike conventional page-mode operations, the enhanced page mode allows the SMJ55161 to operate at a higher data bandwidth. Data retrieval begins as soon as the column address is valid rather than when  $\overline{CASx}$  transitions low. A valid column address can be presented immediately after the row-address hold time has been satisfied, usually well in advance of the falling edge of  $\overline{CASx}$ . In this case, data is obtained after  $t_{a(C)} \max$  (access time from  $\overline{CASx}$  low) if  $t_{a(CA)} \max$  (access time from column address) has been satisfied.

#### refresh

##### $\overline{CAS}$ -before- $\overline{RAS}$ (CBR) refresh

CBR refreshes are accomplished by bringing either or both  $\overline{CASL}$  and  $\overline{CASU}$  low earlier than  $\overline{RAS}$ . The external row address is ignored, and the refresh row address is generated internally. Three types of CBR refresh cycles are available. The CBR refresh (option reset) ends the persistent write-per-bit mode and the stop-point mode. The CBRN and CBRs refreshes (no reset) do not end the persistent write-per-bit mode or the stop-point mode. The 512 rows of the DRAM do not necessarily need to be refreshed consecutively as long as the entire refresh is completed within the required time period,  $t_{r(MA)}$ . The output buffers remain in the high-impedance state during the CBR refresh cycles regardless of the state of  $\overline{TRG}$ .

##### hidden refresh

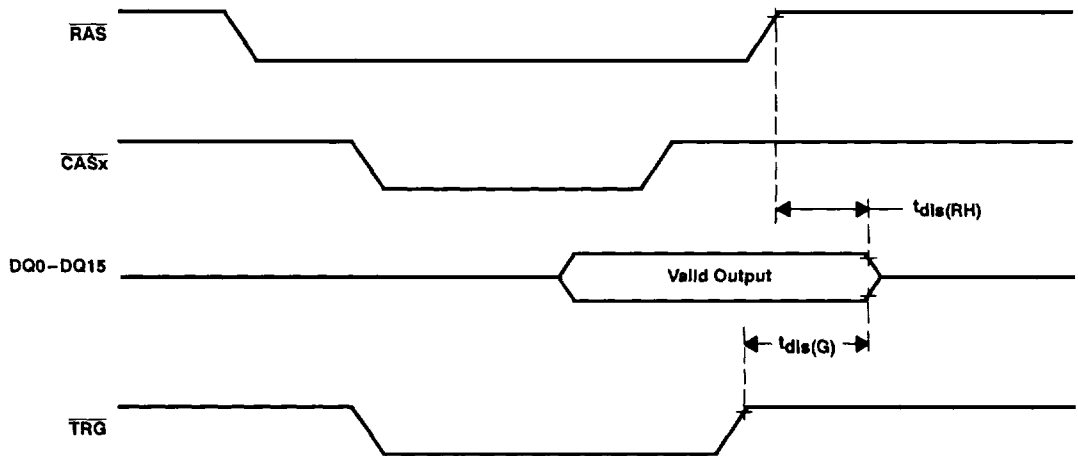
A hidden refresh is accomplished by holding both  $\overline{CASL}$  and  $\overline{CASU}$  low in the DRAM read cycle and cycling  $\overline{RAS}$ . The output data of the DRAM read cycle remains valid while the refresh is carried out. Like the CBR refresh, the refreshed row addresses are generated internally during the hidden refresh.

##### $\overline{RAS}$ -only refresh

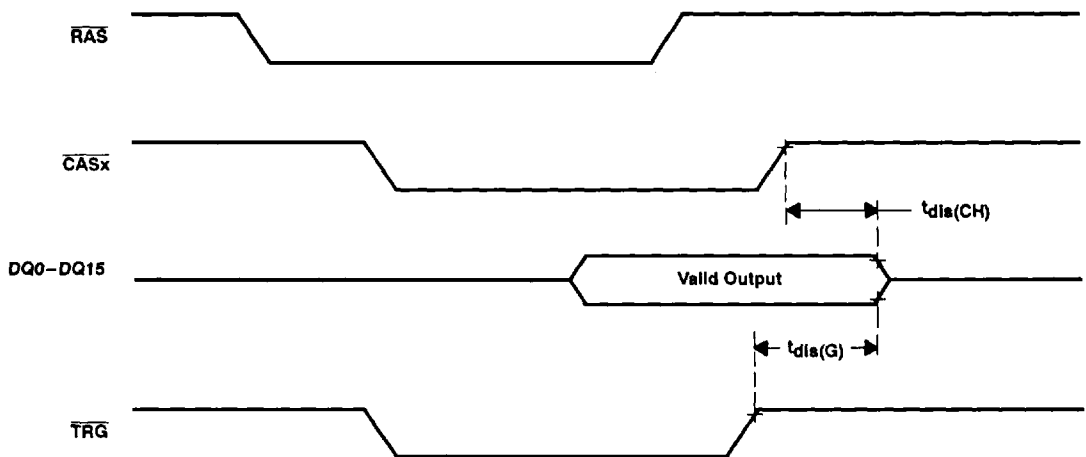
A  $\overline{RAS}$ -only refresh is accomplished by cycling  $\overline{RAS}$  at every row address. Unless  $\overline{CASx}$  and  $\overline{TRG}$  are low, the output buffers remain in the high-impedance state to conserve power. Externally-generated addresses must be supplied during  $\overline{RAS}$ -only refresh. Strobing each of the 512 row addresses with  $\overline{RAS}$  causes all bits in each row to be refreshed.

**extended data output**

The SMJ55161 features extended data output during DRAM accesses. While  $\overline{\text{RAS}}$  and  $\overline{\text{TRG}}$  are low, the DRAM output remains valid. The output remains valid even when  $\overline{\text{CASx}}$  returns high until  $\overline{\text{WE}}$  is low,  $\overline{\text{TRG}}$  is high, or both  $\overline{\text{CASx}}$  and  $\overline{\text{RAS}}$  are high (see Figures 1 and 2). The extended-data-output mode functions in all read cycles including DRAM read, page-mode read, and read-modify-write cycles (see Figure 3).



**Figure 1. DRAM Read Cycle With  $\overline{\text{RAS}}$ -Controlled Output**



**Figure 2. DRAM Read Cycle With  $\overline{\text{CASx}}$ -Controlled Output**

extended-data output (continued)

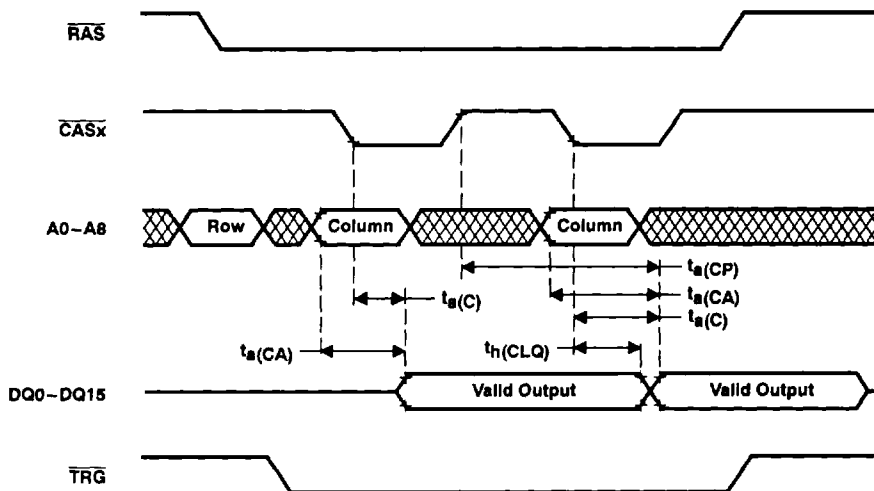


Figure 3. DRAM Page-Read Cycle With Extended Output

**byte operation**

Byte operation can be applied in DRAM-read cycles, write cycles, block-write cycles, load-write-mask-register cycles, and load-color-register cycles. In byte operation, the column address (A0-A8) is latched at the first falling edge of  $\overline{\text{CAS}}_x$ . In read cycles,  $\overline{\text{CAS}}_L$  enables the lower byte (DQ0-DQ7) and  $\overline{\text{CAS}}_U$  enables the upper byte (DQ8-DQ15) (see Figure 4).

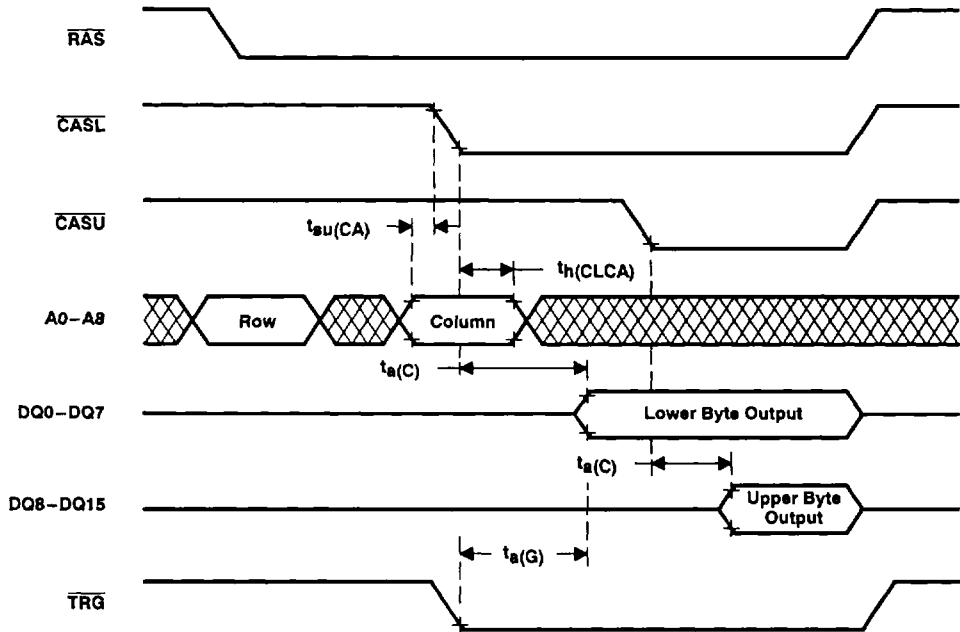


Figure 4. Example of a Byte-Read Cycle

**byte operation (continued)**

In byte-write operation,  $\overline{\text{CASL}}$  enables data to be written to the lower byte (DQ0–DQ7), and  $\overline{\text{CASU}}$  enables data to be written to the upper byte (DQ8–DQ15). In an early write cycle,  $\overline{\text{WE}}$  is brought low prior to both  $\overline{\text{CASx}}$  signals, and data setup and hold times for DQ0–DQ15 are referenced to the first falling edge of  $\overline{\text{CASx}}$  (see Figure 5).

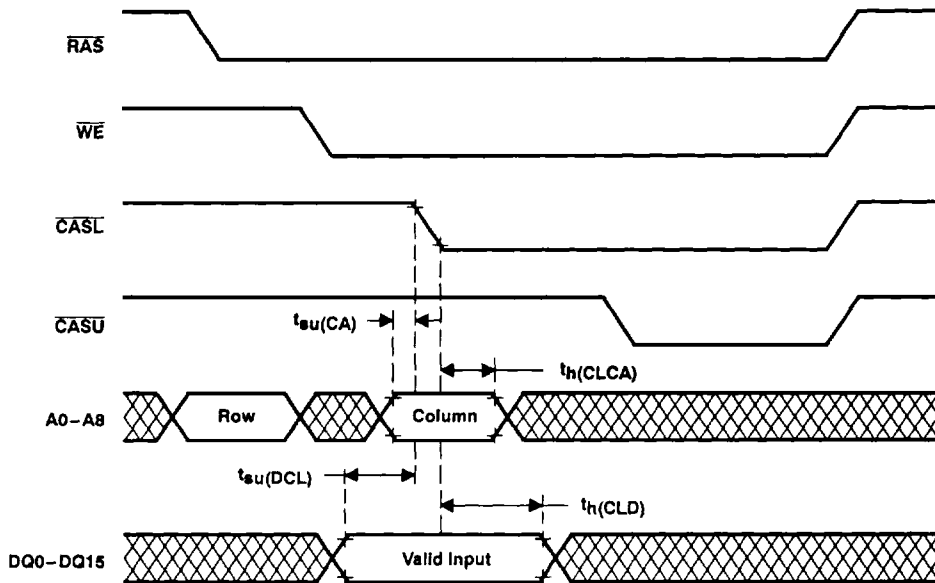
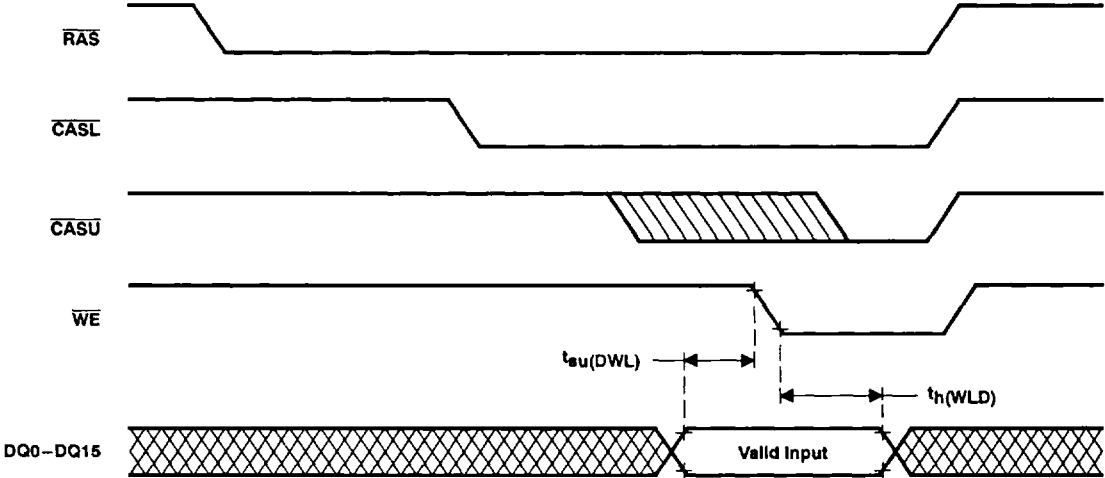


Figure 5. Example of an Early-Write Cycle

**byte operation (continued)**

For late-write or read-modify-write cycles,  $\overline{WE}$  is brought low after either or both  $\overline{CASL}$  and  $\overline{CASU}$  fall. The data is strobed in with data setup and hold times for  $DQ0-DQ15$  referenced to  $\overline{WE}$  (see Figure 6).



**Figure 6. Example of a Late-Write Cycle**

**write-per-bit**

The write-per-bit feature allows masking any combination of the 16 DQs on any write cycle. The write-per-bit operation is invoked when  $\overline{WE}$  is held low on the falling edge of  $\overline{RAS}$ . If  $\overline{WE}$  is held high on the falling edge of  $\overline{RAS}$ , the write operation is performed without any masking. The SMJ55161 offers two write-per-bit modes: nonpersistent write-per-bit and persistent write-per-bit.

**nonpersistent write-per-bit**

When  $\overline{WE}$  is low on the falling edge of  $\overline{RAS}$ , the write mask is reloaded. A 16-bit binary code (the write-per-bit mask) is input to the device via the DQ pins and latched on the falling edge of  $\overline{RAS}$ . The write-per-bit mask selects which of the 16 I/Os are to be written and which are not. After  $\overline{RAS}$  has latched the on-chip write-per-bit mask, input data is driven onto the DQ pins and is latched on either the first falling edge of  $\overline{CASx}$  or the falling edge of  $\overline{WE}$ , whichever occurs later.  $\overline{CASL}$  enables the lower byte (DQ0–DQ7) to be written through the mask and  $\overline{CASU}$  enables the upper byte (DQ8–DQ15) to be written through the mask. If a data low (write mask = 0) is strobed into a particular I/O pin on the falling edge of  $\overline{RAS}$ , data is not written to that I/O. If a data high (write mask = 1) is strobed into a particular I/O pin on the falling edge of  $\overline{RAS}$ , data is written to that I/O (see Figure 7).

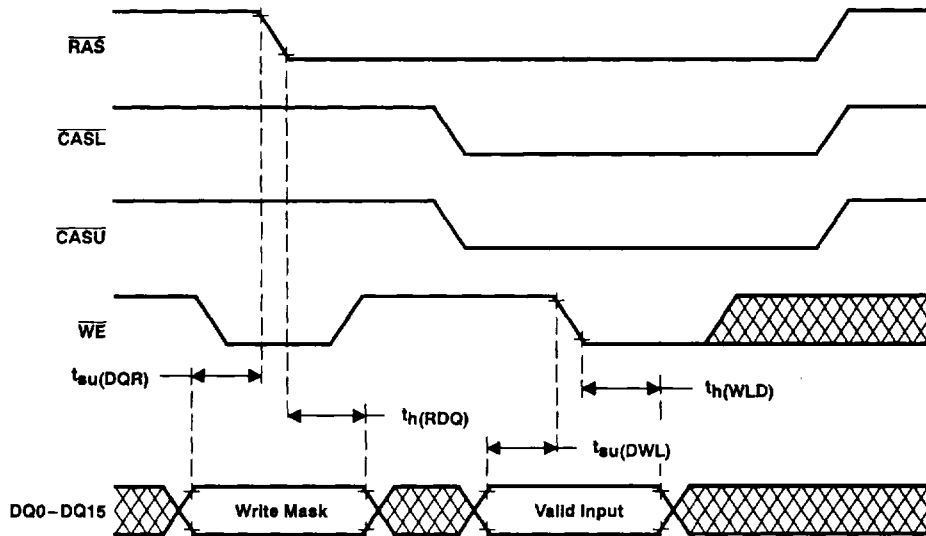
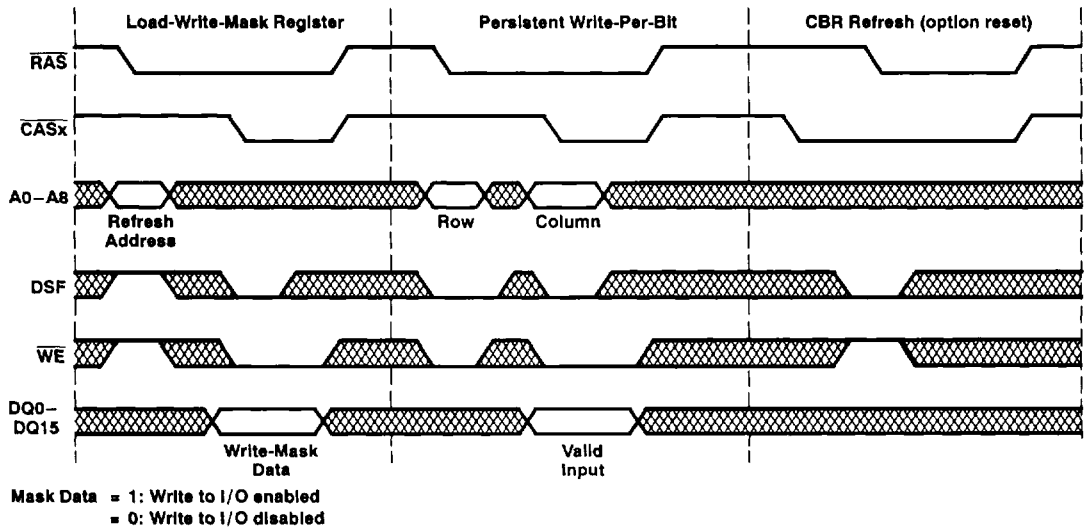


Figure 7. Example of a Nonpersistent Write-Per-Bit (Late-Write) Operation

***persistent write-per-bit***

The persistent write-per-bit mode is initiated by performing a load-write-mask register (LMR) cycle. In the persistent write-per-bit mode, the write-per-bit mask is overwritten but remains valid over an arbitrary number of write cycles until another LMR cycle is performed or power is removed.

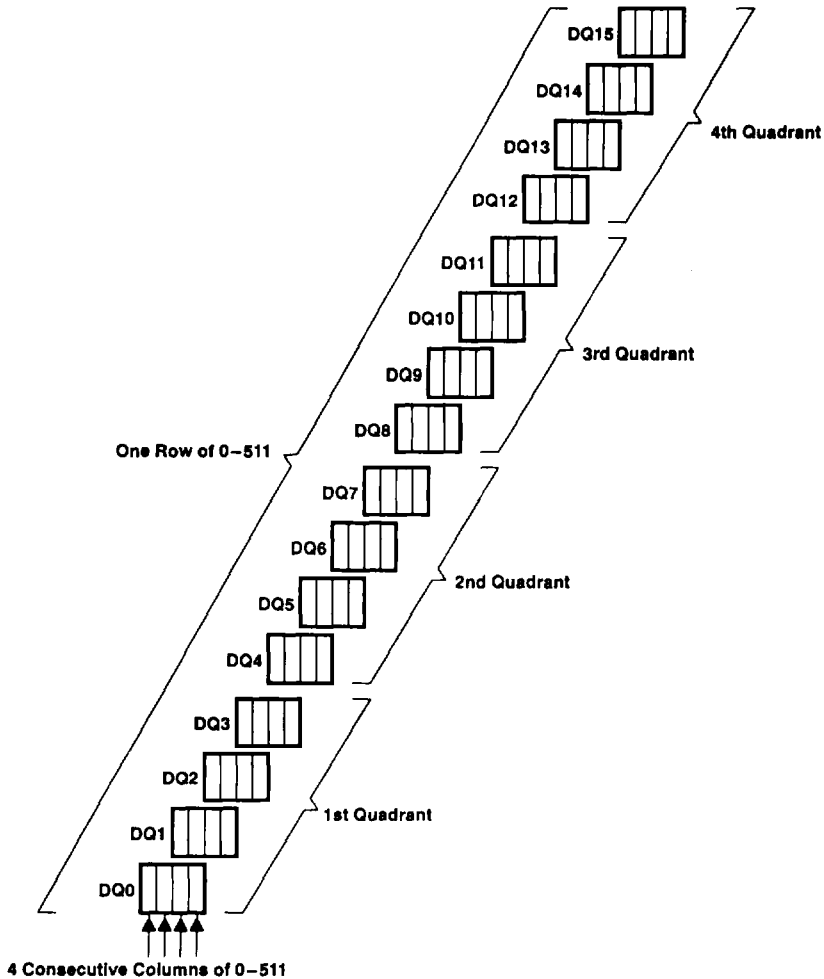
The LMR cycle is performed using DRAM write-cycle timing with DSF held high on the falling edge of  $\overline{\text{RAS}}$  and held low on the first falling edge of  $\overline{\text{CASx}}$ . A binary code is input to the write-mask register via the random I/O pins and latched on either the first falling edge of  $\overline{\text{CASx}}$  or the falling edge of  $\overline{\text{WE}}$ , whichever occurs later. Byte write control can be applied to the write mask during the LMR cycle. The persistent write-per-bit mode can then be used in exactly the same way as the nonpersistent write-per-bit mode except that the input data on the falling edge of  $\overline{\text{RAS}}$  is ignored. When the device is set to the persistent write-per-bit mode, it remains in this mode and is reset only by a CBR refresh (option-reset) cycle (see Figure 8).



**Figure 8. Example of a Persistent Write-Per-Bit Operation**

**block write**

The block-write feature allows up to 64 bits of data to be written simultaneously to one row of the memory array. This function is implemented as 4 columns x 4 DQs and repeated in four quadrants. In this manner, each of the four 1-megabit quadrants can have up to four consecutive columns written at a time with up to 4 DQs per column (see Figure 9).



**Figure 9. Block-Write Operation**

Each 1-megabit quadrant has a 4-bit column mask to mask off any or all of the four columns from being written with data. Nonpersistent write-per-bit or persistent write-per-bit functions can be applied to the block-write operation to provide write-masking options. The DQ data is provided by 4 bits from the on-chip color register. Bits 0-3 from the 16-bit write-mask register, bits 0-3 from the 16-bit column-mask register, and bits 0-3 from the 16-bit color-data register configure the block write for the first quadrant, while bits 4-7, 8-11, and 12-15 of the corresponding registers control the other quadrants in a similar fashion (see Figure 14).

block write (continued)

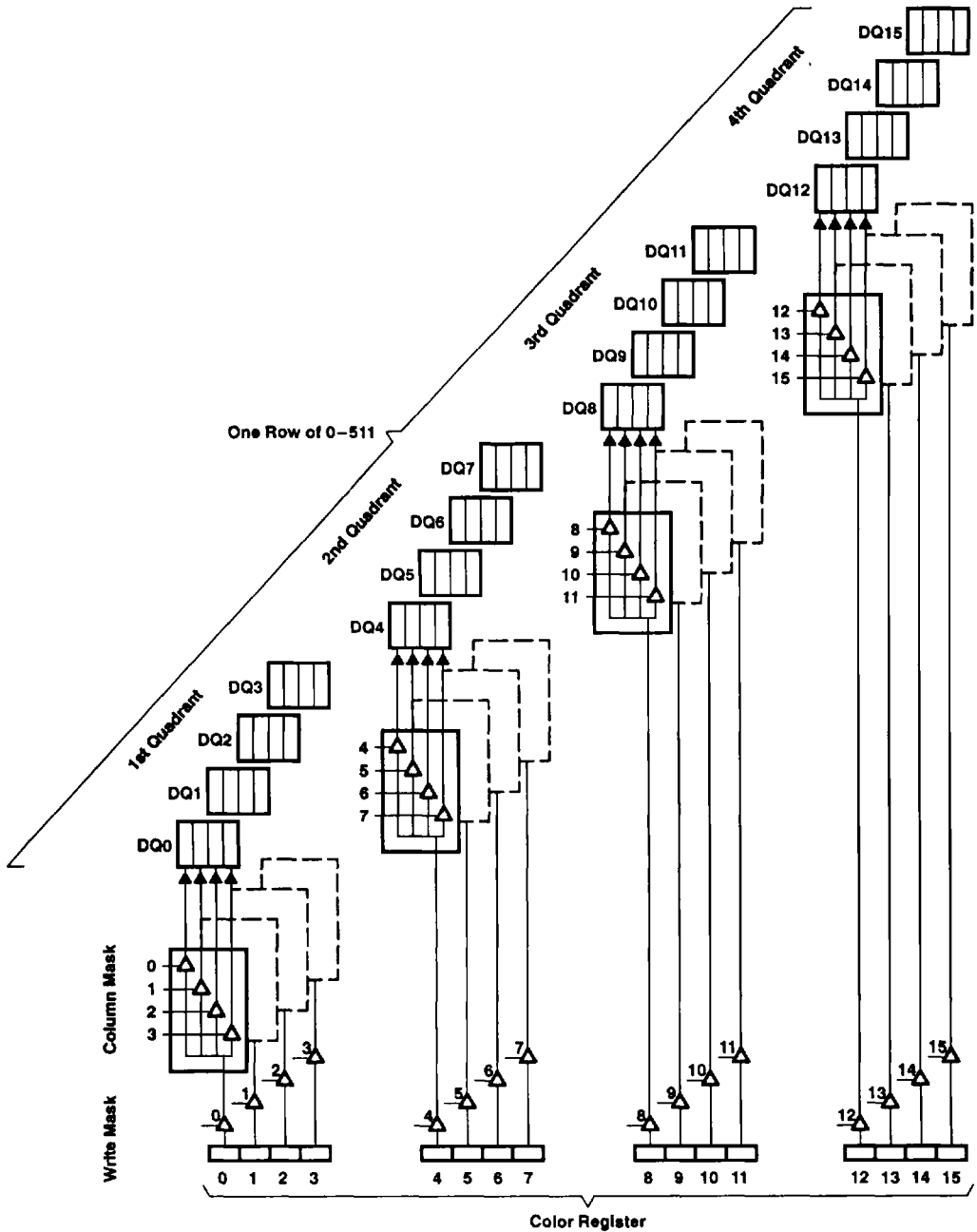
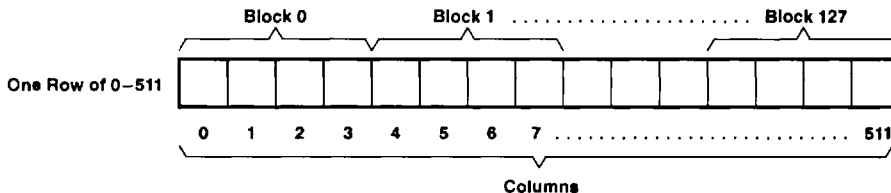


Figure 10. Block Write With Masks

**block write (continued)**

A set of four columns makes a block, resulting in 128 blocks along one row. Block 0 comprises columns 0–3, block 1 comprises columns 4–7, block 2 comprises columns 8–11, etc., as shown in Figure 11.



**Figure 11. Block Columns Organization**

During block-write cycles, only the seven most significant column addresses ( $A_2$ – $A_8$ ) are latched on the first falling edge of  $\overline{CAS}_x$  to decode one of the 128 blocks. Address bits  $A_0$ – $A_1$  are ignored. Each 1-megabit quadrant has the same block selected.

A block-write cycle is entered in a manner similar to a DRAM write cycle except  $\overline{DSF}$  is held high on the first falling edge of  $\overline{CAS}_x$ . As in a DRAM write operation,  $\overline{CAS}_L$  and  $\overline{CAS}_U$  enable the corresponding lower and upper DRAM DQ bytes to be written. The column-mask data is input via the DQs and is latched on either the first falling edge of  $\overline{CAS}_x$  or the falling edge of  $\overline{WE}$ , whichever occurs later. The 16-bit color-data register must be loaded prior to performing a block write as described below. Refer to the write-per-bit section for details on use of the write-mask capability, allowing additional performance options.

Example of block write:

block-write column address = 110000000 ( $A_0$ – $A_8$  from left to right)

	bit 0			bit 15
color-data register	= 1011	1011	1100	0111
write-mask register	= 1110	1111	1111	1011
column-mask register	= 1111	0000	0111	1010
	1st	2nd	3rd	4th
	Quad	Quad	Quad	Quad

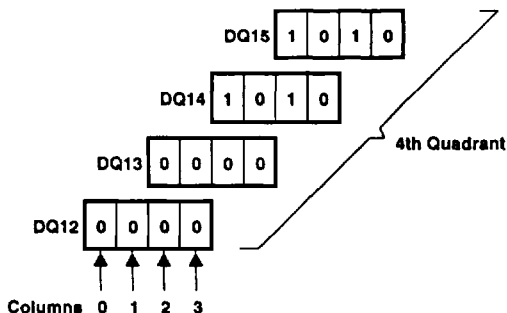
Column-address bits  $A_0$  and  $A_1$  are ignored. Block 0 (columns 0–3) is selected for each 1-megabit quadrant. The first quadrant has  $DQ_0$ – $DQ_2$  written with bits 0–2 from the color-data register (101) to all four columns of block 0.  $DQ_3$  is not written and retains its previous data due to write-mask-register-bit 3 being 0.

The second quadrant ( $DQ_4$ – $DQ_7$ ) has all four columns masked off due to column-mask bits 4–7 being 0, so that no data is written.

The third quadrant ( $DQ_8$ – $DQ_{11}$ ) has its four DQs written with bits 8–11 from the color-data register (1100) to columns 1–3 of its block 0. Column 0 is not written and retains its previous data on all four DQs due to column-mask-register-bit 8 being 0.

**block write (continued)**

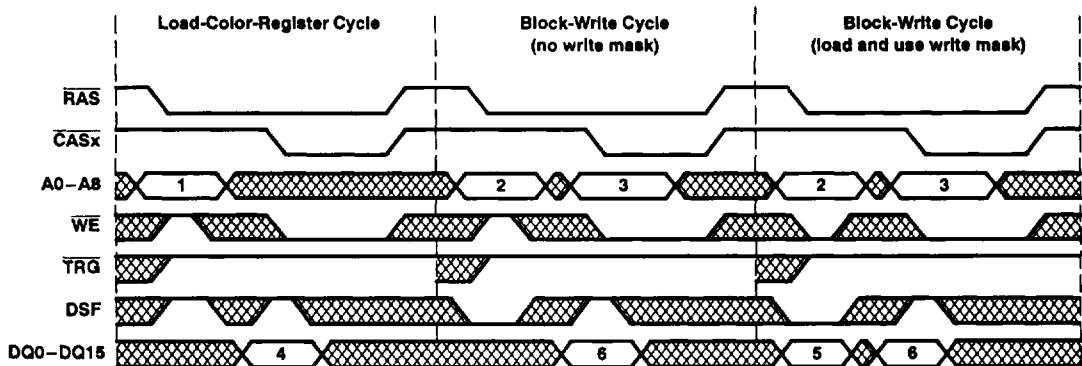
The fourth quadrant (DQ12–DQ15) has DQ12, DQ14, and DQ15 written with bits 12, 14, and 15 from the color-data register to column 0 and column 2 of its block 0. DQ13 retains its previous data on all columns due to the write mask. Columns 1 and 3 retain their previous data on all DQs due to the column mask. If the previous data for the quadrant was all 0s, the fourth quadrant would contain the data pattern shown in Figure 12 after the block-write operation shown in the previous example.



**Figure 12. Example of Fourth Quadrant After a Block-Write Operation**

**load color register**

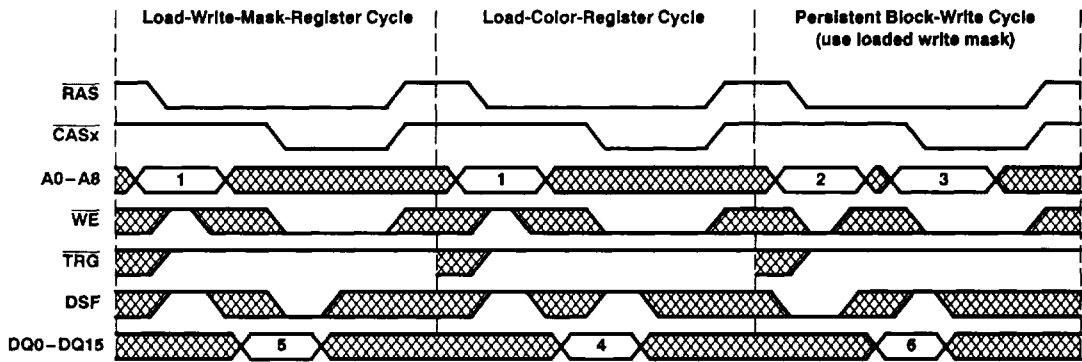
The load-color-register cycle is performed using normal DRAM write-cycle timing except that DSF is held high on the falling edges of  $\overline{RAS}$ ,  $\overline{CASL}$ , and  $\overline{CASU}$ . The color register is loaded from pins DQ0–DQ15, which are latched on either the first falling edge of  $\overline{CASx}$  or the falling edge of  $\overline{WE}$ , whichever occurs later. If only one  $\overline{CASx}$  is low, only the corresponding byte of the color register is loaded. When the color register is loaded, it retains data until power is lost or until another load-color-register cycle is performed (see Figures 13 and 14).



- Legend:
1. Refresh address
  2. Row address
  3. Block address (A2–A8) is latched on the first falling edge of  $\overline{CASx}$ .
  4. Color-register data
  5. Write-mask data: DQ0–DQ15 are latched on the falling edge of  $\overline{RAS}$ .
  6. Column-mask data: DQ1–DQ12 (l = 0, 4, 8, 12) are latched on either the first falling edge of  $\overline{CASx}$  or the falling edge of  $\overline{WE}$ , whichever occurs later.
- = don't care

**Figure 13. Example of Block Writes**

load color register (continued)



Legend:

1. Refresh address
2. Row address
3. Block address (A2-A8) is latched on the first falling edge of  $\overline{CASx}$ .
4. Color-register data
5. Write-mask data: DQ0-DQ15 are latched on the falling edge of  $\overline{CASx}$ .
6. Column-mask data: DQi-DQi+3 (i = 0, 4, 8, 12) are latched on either the first falling edge of  $\overline{CASx}$  or the falling edge of  $\overline{WE}$ , whichever occurs later.

= don't care

Figure 14. Example of a Persistent Block Write

DRAM-to-SAM transfer operation

During the DRAM-to-SAM transfer operation, one half of a row (256 columns) in the DRAM array is selected to be transferred to the 256-bit serial-data register. The transfer operation is invoked by  $\overline{TRG}$  being brought low and  $\overline{WE}$  being held high on the falling edge of  $\overline{RAS}$ . The state of DSF, which is latched on the falling edge of  $\overline{RAS}$ , determines whether the full-register-transfer read operation or the split-register-transfer read operation is performed.

Table 2. SAM Function Table

FUNCTION	$\overline{RAS}$ FALL				$\overline{CASx}$ FALL	ADDRESS		DQ0-DQ15		MNE CODE
	$\overline{CASx}^\dagger$	$\overline{TRG}$	$\overline{WE}$	DSF	DSF	$\overline{RAS}$	$\overline{CASx}$	$\overline{RAS}$	$\overline{CASx}$ $\overline{WE}$	
Full-register-transfer read	H	L	H	L	X	Row Addr	Tap Point	X	X	RT
Split-register-transfer read	H	L	H	H	X	Row Addr	Tap Point	X	X	SRT

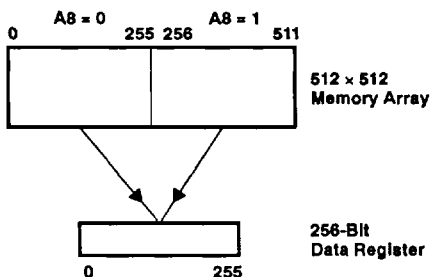
<sup>†</sup> Logic L is selected when either  $\overline{CASL}$  or  $\overline{CASU}$  are low.

X = don't care



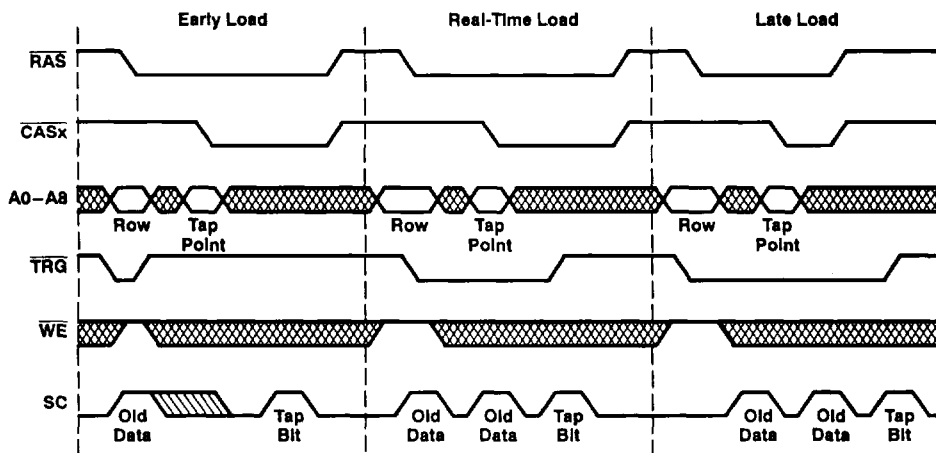
**full-register-transfer read**

A full-register-transfer read operation loads data from a selected half of a row in the DRAM into the SAM.  $\overline{TRG}$  is brought low and latched at the falling edge of  $\overline{RAS}$ . Nine row-address bits ( $A_0$ – $A_8$ ) are also latched at the falling edge of  $\overline{RAS}$  to select one of the 512 rows available for the transfer. The nine column-address bits ( $A_0$ – $A_8$ ) are latched at the first falling edge of  $\overline{CAS}_x$ , where address bit  $A_8$  selects which half of the row is transferred. Address bits  $A_0$ – $A_7$  select one of the SAM's 256 available tap points from which the serial data is read out (see Figure 15).



**Figure 15. Full-Register-Transfer Read**

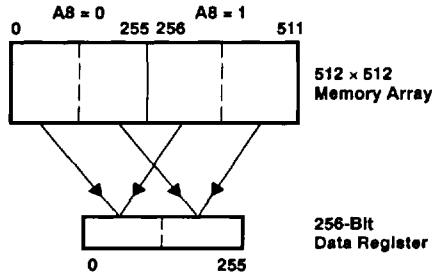
A full-register-transfer read can be performed in three ways: early load, real-time load (or midline load), or late load. Each of these offers the flexibility of controlling the  $\overline{TRG}$  trailing edge in the full-register-transfer read cycle (see Figure 16).



**Figure 16. Example of Full-Register-Transfer Read Operations**

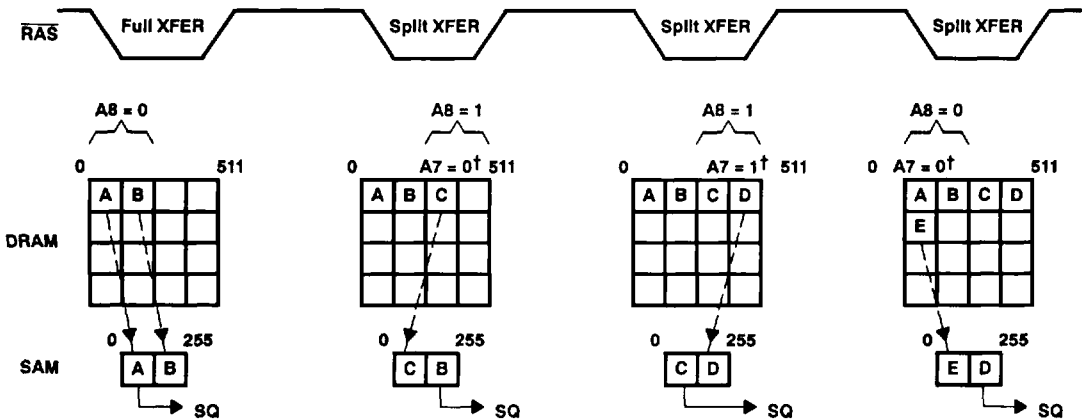
**split-register-transfer read**

In the split-register-transfer-read operation, the serial-data register is split into halves. The low half contains bits 0–127, and the high half contains bits 128–255. While one half is being read out of the SAM port, the other half can be loaded from the memory array.



**Figure 17. Split-Register-Transfer Read**

To invoke a split-register-transfer-read cycle, DSF is brought high,  $\overline{TRG}$  is brought low, and both are latched at the falling edge of  $\overline{RAS}$ . Nine row-address bits (A0–A8) are also latched at the falling edge of  $\overline{RAS}$  to select one of the 512 rows available for the transfer. Eight of the nine column-address bits (A0–A6 and A8) are latched at the first falling edge of  $\overline{CASx}$ . Column-address bit A8 selects which half of the row is to be transferred. Column-address bits A0–A6 selects one of the 127 tap points in the specified half of the SAM. Column-address bit A7 is ignored, and the split-register transfer is internally controlled to select the inactive register half.



† A7 shown is internally controlled.

**Figure 18. Example of a Split-Register-Transfer Read Operation**

A full-register-transfer read must precede the first split-register-transfer read to ensure proper operation. After the full-register-transfer read cycle, the first split-register-transfer read can follow immediately without any minimum SC clock requirement.

*split-register-transfer read (continued)*

QSF indicates which half of the register is being accessed during serial-access operation. When QSF is low, the serial-address pointer is accessing the lower (least significant) 128 bits of the SAM. When QSF is high, the pointer is accessing the higher (most significant) 128 bits of the SAM. QSF changes state upon completing a full-register-transfer read cycle. The tap point loaded during the current transfer cycle determines the state of QSF. QSF also changes state when a boundary between two register halves is reached.

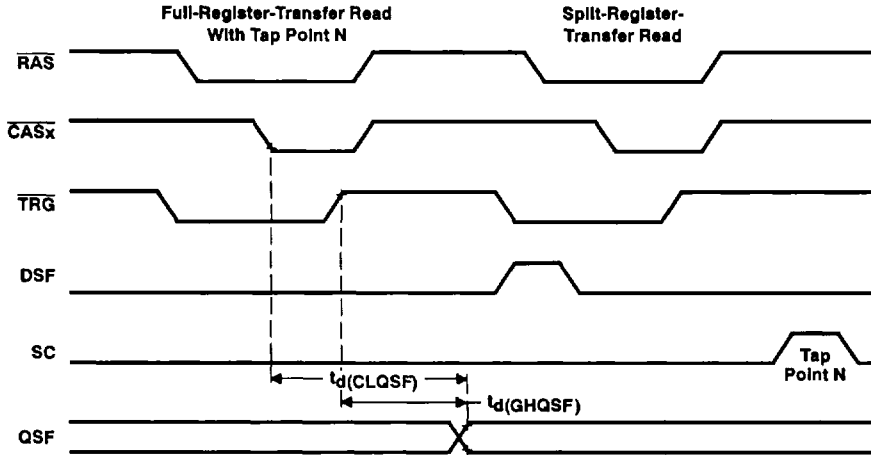


Figure 19. Example of a Split-Register-Transfer Read After a Full-Register-Transfer Read

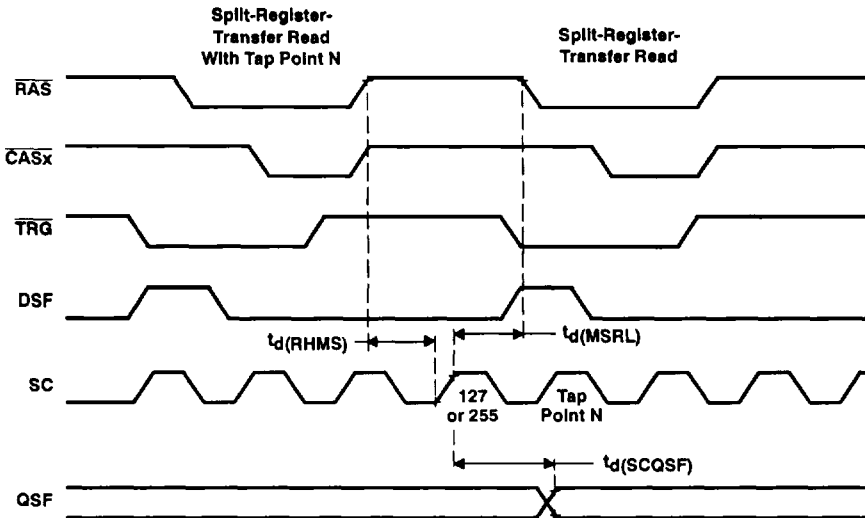
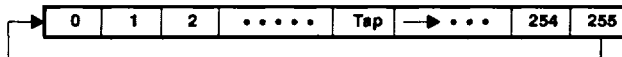


Figure 20. Example of Successive Split-Register-Transfer Read Operations

**serial-read operation**

The serial-read operation can be performed through the SAM port simultaneously and asynchronously with DRAM operations except during transfer operations. Serial data can be read from the SAM by clocking SC starting at the tap point loaded by the preceding transfer cycle, proceeding sequentially to the most significant bit (bit 255), and then wrapping around to the least significant bit (bit 0), as shown in Figure 21.



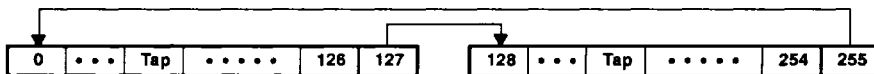
**Figure 21. Serial-Pointer Direction for Serial Read**

For split-register-transfer read operation, serial data can be read out from the active half of the SAM by clocking SC starting at the tap point loaded by the preceding split-register-transfer cycle. The serial pointer then proceeds sequentially to the most significant bit of the half, bit 127 or bit 255. If there is a split-register-transfer read to the inactive half during this period, the serial pointer points next to the tap point location loaded by that split-register transfer (see Figure 22).



**Figure 22. Serial Pointer for Split-Register Read – Case I**

If there is no split-register-transfer read to the inactive half during this period, the serial pointer points next to bit 128 or bit 0, respectively (see Figure 23).

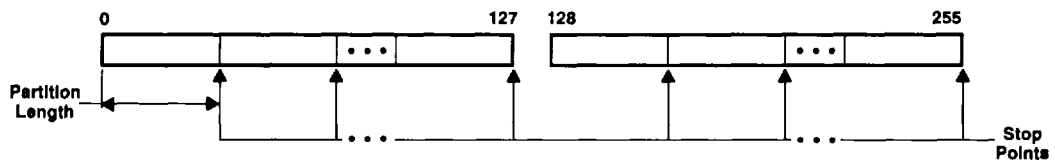


**Figure 23. Serial Pointer for Split-Register Read – Case II**

**split-register programmable stop point**

The SMJ55161 offers programmable stop-point mode for split-register-transfer read operation. This mode can be used to improve two-dimensional drawing performance in a nonscanline data format.

In split-register-transfer read operation, the stop point is defined as a register location at which the serial output stops coming from one half of the SAM and switches to the opposite half of the SAM. While in stop-point mode, the SAM is divided into partitions whose length is programmed via row addresses A4–A7 in a CBR set (CBRS) cycle. The last serial-address location of each partition is the stop point (see Figure 24).



**Figure 24. Example of the SAM With Partitions**

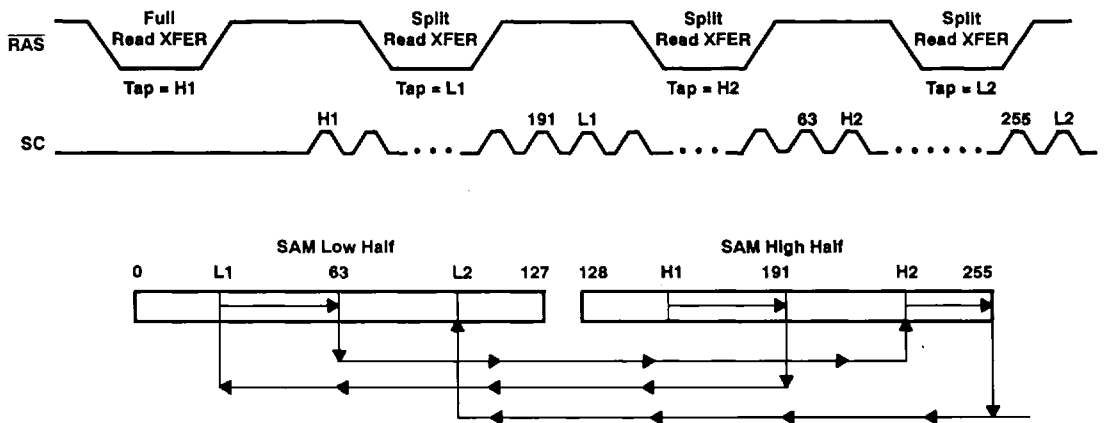
**split-register programmable stop point (continued)**

Stop-point mode is not active until the CBRS cycle is initiated. The CBRS operation is performed by holding CASx and WE low and DSF high on the falling edge of RAS. The falling edge of RAS also latches row addresses A4-A7 which are used to define the SAM's partition length. The other row-address inputs are don't cares. Stop-point mode should be initiated after the initialization cycles are performed (see Table 3).

**Table 3. Programming Code for Stop-Point Mode**

MAXIMUM PARTITION LENGTH	ADDRESS AT RAS IN CBRS CYCLE						NUMBER OF PARTITIONS	STOP-POINT LOCATIONS
	A8	A7	A6	A5	A4	A0-A3		
16	X	L	L	L	L	X	16	15, 31, 47, 63, 79, 95, 111, 127, 143, 159, 175, 191, 207, 223, 239, 255
32	X	L	L	L	H	X	8	31, 63, 95, 127, 159, 191, 223, 255
64	X	L	L	H	H	X	4	63, 127, 191, 255
128 (default)	X	L	H	H	H	X	2	127, 255

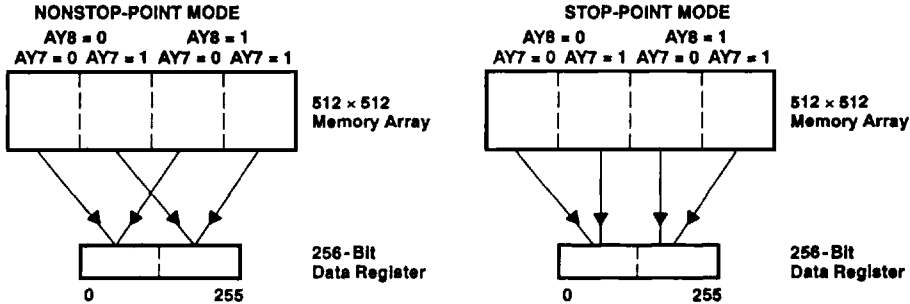
In stop-point mode, the tap point loaded during the split-register-transfer read cycle determines the SAM partition in which the serial output begins and at which stop point the serial output stops coming from one half of the SAM and switches to the opposite half of the SAM (see Figure 25).



**Figure 25. Example of Split-Register Operation With Programmable Stop Points**

**256-/512-bit compatibility of split-register programmable stop point**

The stop-point mode is designed to be compatible with both 256-bit SAM and 512-bit SAM devices. After the CBRS cycle is initiated, the stop-point mode becomes active. In the stop-point mode, and only in the stop-point mode, the column-address bits AY7 and AY8 are internally swapped to assure compatibility (see Figure 26). This address-bit swap applies to the column address, and it is effective for all DRAM and transfer cycles. For example, during the split-register-transfer cycle with stop point, column-address bit AY8 is a don't care and AY7 decodes the DRAM row half for the split-register transfer. During stop-point mode, a CBR (option reset) cycle is not recommended, because this ends the stop-point mode and restores address bits AY7 and AY8 to their normal functions. Consistent use of CBR cycles ensures that the SMJ55161 remains in normal mode.



**Figure 26. DRAM-to-SAM Mapping, Nonstop-Point Versus Stop Point**

**IMPORTANT:** For proper device operation, a stop-point-mode (CBRS) cycle should be initiated immediately after the power-up initialization cycles are performed.

**power up**

To achieve proper device operation, an initial pause of 200 μs is required after power up followed by a minimum of eight  $\overline{\text{RAS}}$  cycles or eight CBR cycles to initialize the DRAM port. A full-register-transfer read cycle and two SC cycles are required to initialize the SAM port.

After initialization, the internal state of the SMJ55161 is as follows:

	STATE AFTER INITIALIZATION
QSF	Defined by the transfer cycle during initialization
Write mode	Nonpersistent mode
Write-mask register	Undefined
Color register	Undefined
Serial-register tap point	Defined by the transfer cycle during initialization
SAM port	Output mode

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ (see Note 1)	-1 V to 7 V
Voltage range on any pin	-1 V to 7 V
Short-circuit output current	50 mA
Power dissipation	1.1 W
Operating free-air temperature range, $T_A$	-55°C to 125°C
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to  $V_{SS}$ .

**recommended operating conditions**

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5	5.5	V
$V_{SS}$ Supply voltage		0		V
$V_{IH}$ High-level input voltage	2.4		6.5	V
$V_{IL}$ Low-level input voltage (see Note 2)	-1		0.8	V
$T_A$ Operating free-air temperature	-55		125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

PARAMETER	TEST CONDITIONS ‡	SAM PORT	'55161-70		'55161-80		UNIT
			MIN	MAX	MIN	MAX	
$V_{OH}$ High-level output voltage	$I_{OH} = -1$ mA		2.4		2.4		V
$V_{OL}$ Low-level output voltage	$I_{OL} = 2$ mA		0.4		0.4		V
$I_I$ Input current (leakage)	$V_{CC} = 5.5$ V, $V_I = 0$ V to 5.8 V, All other pins at 0 V to $V_{CC}$		±10		±10		µA
$I_O$ Output current (leakage) (see Note 3)	$V_{CC} = 5.5$ V, $V_O = 0$ V to $V_{CC}$		±10		±10		µA
$I_{CC1}$ Operating current §	See Note 4	Standby	165		160		mA
$I_{CC1A}$ Operating current §	$t_c(SC) = \text{MIN}$	Active	210		195		mA
$I_{CC2}$ Standby current	All clocks = $V_{CC}$	Standby	12		12		mA
$I_{CC2A}$ Standby current	$t_c(SC) = \text{MIN}$	Active	70		65		mA
$I_{CC3}$ $\overline{\text{RAS}}$ -only refresh current	See Note 4	Standby	165		160		mA
$I_{CC3A}$ $\overline{\text{RAS}}$ -only refresh current	$t_c(SC) = \text{MIN}$ , See Note 4	Active	215		195		mA
$I_{CC4}$ Page-mode current §	$t_c(P) = \text{MIN}$ , See Note 5	Standby	100		95		mA
$I_{CC4A}$ Page-mode current §	$t_c(SC) = \text{MIN}$ , See Note 5	Active	145		130		mA
$I_{CC5}$ CBR current	See Note 4	Standby	165		160		mA
$I_{CC5A}$ CBR current	$t_c(SC) = \text{MIN}$ , See Note 4	Active	210		195		mA
$I_{CC6}$ Data-transfer current	See Note 4	Standby	180		170		mA
$I_{CC6A}$ Data-transfer current	$t_c(SC) = \text{MIN}$	Active	225		200		mA

‡ For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

§ Measured with outputs open

NOTES: 3.  $\overline{\text{SE}}$  is disabled for SQ output leakage tests.

4. Measured with one address change while  $\overline{\text{RAS}} = V_{IL}$ ;  $t_c(rd)$ ,  $t_c(W)$ ,  $t_c(TRD) = \text{MIN}$

5. Measured with one address change while  $\overline{\text{CAS}} = V_{IH}$



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capacitance over recommended ranges of supply voltage and operating free-air temperature,  $f = 1$  MHz (see Note 6)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		5	10	pF
$C_{i(RC)}$	Input capacitance, address-strobe inputs		8	10	pF
$C_{i(W)}$	Input capacitance, write-enable input		7	10	pF
$C_{i(SC)}$	Input capacitance, serial clock		6	10	pF
$C_{i(SE)}$	Input capacitance, serial enable		7	10	pF
$C_{i(OSF)}$	Input capacitance, special function		7	10	pF
$C_{i(TRG)}$	Input capacitance, transfer-register input		7	10	pF
$C_{o(O)}$	Output capacitance, SQ and DQ		12	15	pF
$C_{o(QSF)}$	Output capacitance, QSF		10	12	pF

NOTE 8:  $V_{CC} = 5 V \pm 0.5 V$ , and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 7)

PARAMETER	TEST CONDITIONS†	ALT. SYMBOL	'55161-70		'55161-80		UNIT	
			MIN	MAX	MIN	MAX		
$t_{a(C)}$	Access time from $\overline{CASx}$	$t_d(RLCL) = \text{MAX}$	$t_{CAC}$	20		20	ns	
$t_{a(CA)}$	Access time from column address	$t_d(RLCL) = \text{MAX}$	$t_{AA}$	35		40	ns	
$t_{a(CP)}$	Access time from $\overline{CASx}$ high	$t_d(RLCL) = \text{MAX}$	$t_{CPA}$	40		45	ns	
$t_{a(R)}$	Access time from $\overline{RAS}$	$t_d(RLCL) = \text{MAX}$	$t_{RAC}$	70		80	ns	
$t_{a(G)}$	Access time of DQ from $\overline{TRG}$ low		$t_{OEA}$	20		20	ns	
$t_{a(SQ)}$	Access time of SQ from SC high	$C_L = 30$ pF	$t_{SCA}$	20		25	ns	
$t_{a(SE)}$	Access time of SQ from $\overline{SE}$ low	$C_L = 30$ pF	$t_{SEA}$	15		20	ns	
$t_{dis(CH)}$	Disable time, random output from $\overline{CASx}$ high (see Note 8)	$C_L = 50$ pF	$t_{OFF}$	0	20	0	20	ns
$t_{dis(RH)}$	Disable time, random output from $\overline{RAS}$ high (see Note 8)	$C_L = 50$ pF		0	20	0	20	ns
$t_{dis(G)}$	Disable time, random output from $\overline{TRG}$ high (see Note 8)	$C_L = 50$ pF	$t_{OEZ}$	0	20	0	20	ns
$t_{dis(WL)}$	Disable time, random output from $\overline{WE}$ low (see Note 8)	$C_L = 50$ pF	$t_{WEZ}$	0	20	0	20	ns
$t_{dis(SE)}$	Disable time, serial output from $\overline{SE}$ high (see Note 8)	$C_L = 30$ pF	$t_{SEZ}$	0	15	0	20	ns

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

NOTES: 7. Switching times for RAM-port output are measured with a load equivalent to 1 TTL load and 50 pF. Data-out reference level:  $V_{OH}/V_{OL} = 2 V/0.8 V$ . Switching times for SAM-port output are measured with a load equivalent to 1 TTL load and 30 pF. Serial-data out reference level:  $V_{OH}/V_{OL} = 2 V/0.8 V$ .

8.  $t_{dis(CH)}$ ,  $t_{dis(RH)}$ ,  $t_{dis(G)}$ ,  $t_{dis(WL)}$ , and  $t_{dis(SE)}$  are specified when the output is no longer driven.



**Timing requirements over recommended ranges of supply voltage and operating free-air temperature†**

	ALT. SYMBOL	'55161-70		'55161-80		UNIT
		MIN	MAX	MIN	MAX	
t <sub>c</sub> (rd) Cycle time, read	t <sub>RC</sub>	130		150		ns
t <sub>c</sub> (W) Cycle time, write	t <sub>WC</sub>	130		150		ns
t <sub>c</sub> (rdW) Cycle time, read-modify-write	t <sub>RMW</sub>	175		200		ns
t <sub>c</sub> (P) Cycle time, page-mode read, write	t <sub>PC</sub>	45		50		ns
t <sub>c</sub> (RDWP) Cycle time, page-mode read-modify-write	t <sub>PRMW</sub>	85		90		ns
t <sub>c</sub> (TRD) Cycle time, transfer read	t <sub>RC</sub>	130		150		ns
t <sub>c</sub> (SC) Cycle time, serial clock (see Note 9)	t <sub>SCC</sub>	22		30		ns
t <sub>w</sub> (CH) Pulse duration, $\overline{CASx}$ high	t <sub>CPN</sub>	10		10		ns
t <sub>w</sub> (CL) Pulse duration, $\overline{CASx}$ low (see Note 10)	t <sub>CAS</sub>	20	10 000	20	10 000	ns
t <sub>w</sub> (RH) Pulse duration, $\overline{RAS}$ high	t <sub>RP</sub>	50		60		ns
t <sub>w</sub> (RL) Pulse duration, $\overline{RAS}$ low (see Note 11)	t <sub>RAS</sub>	70	10 000	80	10 000	ns
t <sub>w</sub> (WL) Pulse duration, $\overline{WE}$ low	t <sub>WP</sub>	10		15		ns
t <sub>w</sub> (TRG) Pulse duration, $\overline{TRG}$ low		20		20		ns
t <sub>w</sub> (SCH) Pulse duration, SC high	t <sub>SC</sub>	8		10		ns
t <sub>w</sub> (SCL) Pulse duration, SC low	t <sub>SCP</sub>	8		10		ns
t <sub>w</sub> (GH) Pulse duration, $\overline{TRG}$ high	t <sub>TP</sub>	20		20		ns
t <sub>w</sub> (RLP) Pulse duration, $\overline{RAS}$ low (page mode)	t <sub>RASP</sub>	70	100 000	80	100 000	ns
t <sub>su</sub> (CA) Setup time, column address before $\overline{CASx}$ low	t <sub>ASC</sub>	0		0		ns
t <sub>su</sub> (SFC) Setup time, DSF before $\overline{CASx}$ low	t <sub>FSC</sub>	0		0		ns
t <sub>su</sub> (RA) Setup time, row address before $\overline{RAS}$ low	t <sub>ASR</sub>	0		0		ns
t <sub>su</sub> (WMB) Setup time, $\overline{WE}$ before $\overline{RAS}$ low	t <sub>WSR</sub>	0		0		ns
t <sub>su</sub> (DQR) Setup time, DQ before $\overline{RAS}$ low	t <sub>MS</sub>	0		0		ns
t <sub>su</sub> (TRG) Setup time, $\overline{TRG}$ high before $\overline{RAS}$ low	t <sub>THS</sub>	0		0		ns
t <sub>su</sub> (SFR) Setup time, DSF low before $\overline{RAS}$ low	t <sub>FSR</sub>	0		0		ns
t <sub>su</sub> (DCL) Setup time, data valid before $\overline{CASx}$ low	t <sub>DSC</sub>	0		0		ns
t <sub>su</sub> (DWL) Setup time, data valid before $\overline{WE}$ low	t <sub>DSW</sub>	0		0		ns
t <sub>su</sub> (rd) Setup time, read command, $\overline{WE}$ high before $\overline{CASx}$ low	t <sub>RCS</sub>	0		0		ns
t <sub>su</sub> (WCL) Setup time, early-write command, $\overline{WE}$ low before $\overline{CASx}$ low	t <sub>WCS</sub>	0		0		ns
t <sub>su</sub> (WCH) Setup time, $\overline{WE}$ low before $\overline{CASx}$ high, write	t <sub>CWL</sub>	15		20		ns
t <sub>su</sub> (WRH) Setup time, $\overline{WE}$ low before $\overline{RAS}$ high, write	t <sub>RWL</sub>	20		20		ns
t <sub>h</sub> (CLCA) Hold time, column address after $\overline{CASx}$ low	t <sub>CAH</sub>	10		15		ns
t <sub>h</sub> (SFC) Hold time, DSF after $\overline{CASx}$ low	t <sub>CFH</sub>	15		15		ns
t <sub>h</sub> (RA) Hold time, row address after $\overline{RAS}$ low	t <sub>RAH</sub>	10		10		ns

† Timing measurements are referenced to V<sub>IL</sub> max and V<sub>IH</sub> min.

NOTES: 9. Cycle time assumes t<sub>t</sub> = 3 ns.

10. In a read-modify-write cycle, t<sub>d</sub>(CLWL) and t<sub>su</sub>(WCH) must be observed. Depending on the user's transition times, this can require additional  $\overline{CASx}$  low time [t<sub>w</sub>(CL)].

11. In a read-modify-write cycle, t<sub>d</sub>(RLWL) and t<sub>su</sub>(WRH) must be observed. Depending on the user's transition times, this can require additional  $\overline{RAS}$  low time [t<sub>w</sub>(RL)].

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued) †

	ALT. SYMBOL	'55161-70		'55161-80		UNIT
		MIN	MAX	MIN	MAX	
t <sub>h</sub> (TRG) Hold time, TRG after RAS low	t <sub>THH</sub>	15		15		ns
t <sub>h</sub> (RWM) Hold time, write mask after RAS low	t <sub>RWH</sub>	15		15		ns
t <sub>h</sub> (RDQ) Hold time, DQ after RAS low (write-mask operation)	t <sub>MH</sub>	15		15		ns
t <sub>h</sub> (SFR) Hold time, DSF after RAS low	t <sub>RFH</sub>	10		10		ns
t <sub>h</sub> (RLCA) Hold time, column address valid after RAS low (see Note 12)	t <sub>AR</sub>	30		35		ns
t <sub>h</sub> (CLD) Hold time, data valid after CASx low	t <sub>DH</sub>	15		15		ns
t <sub>h</sub> (RLD) Hold time, data valid after RAS low (see Note 12)	t <sub>DHR</sub>	35		35		ns
t <sub>h</sub> (WLD) Hold time, data valid after WE low	t <sub>DH</sub>	15		15		ns
t <sub>h</sub> (CHrd) Hold time, read, WE high after CASx high (see Note 13)	t <sub>RCH</sub>	0		0		ns
t <sub>h</sub> (RHrd) Hold time, read, WE high after RAS high (see Note 13)	t <sub>RRH</sub>	0		0		ns
t <sub>h</sub> (CLW) Hold time, write, WE low after CASx low	t <sub>WCH</sub>	15		15		ns
t <sub>h</sub> (RLW) Hold time, write, WE low after RAS low (see Note 12)	t <sub>WCR</sub>	35		35		ns
t <sub>h</sub> (WLG) Hold time, TRG high after WE low (see Note 14)	t <sub>OEH</sub>	10		10		ns
t <sub>h</sub> (SHSQ) Hold time, SQ valid after SC high	t <sub>SOH</sub>	2		2		ns
t <sub>h</sub> (RSF) Hold time, DSF after RAS low	t <sub>FHR</sub>	35		35		ns
t <sub>h</sub> (CLO) Hold time, output valid after CASx low	t <sub>DHC</sub>	0		0		ns
t <sub>d</sub> (RLCH) Delay time, RAS low to CASx high	t <sub>CSH</sub>	70		80		ns
	See Note 15 t <sub>CHR</sub>	10		15		
t <sub>d</sub> (CHRL) Delay time, CASx high to RAS low	t <sub>CRP</sub>	0		0		ns
t <sub>d</sub> (CLRH) Delay time, CASx low to RAS high	t <sub>RSH</sub>	20		20		ns
t <sub>d</sub> (CLWL) Delay time, CASx low to WE low (see Notes 16 and 17)	t <sub>CWD</sub>	45		50		ns
t <sub>d</sub> (RLCL) Delay time, RAS low to CASx low (see Note 18)	t <sub>RCD</sub>	20	50	20	60	ns
t <sub>d</sub> (CARH) Delay time, column address valid to RAS high	t <sub>RAL</sub>	35		40		ns
t <sub>d</sub> (CACH) Delay time, column address valid to CASx high	t <sub>CAL</sub>	35		40		ns
t <sub>d</sub> (RLWL) Delay time, RAS low to WE low (see Note 16)	t <sub>RWD</sub>	95		105		ns
t <sub>d</sub> (CAWL) Delay time, column address valid to WE low (see Note 16)	t <sub>AWD</sub>	60		65		ns
t <sub>d</sub> (CLRL) Delay time, CASx low to RAS low (see Note 15)	t <sub>CSR</sub>	0		0		ns
t <sub>d</sub> (RHCL) Delay time, RAS high to CASx low (see Note 15)	t <sub>RPC</sub>	0		0		ns
t <sub>d</sub> (CLGH) Delay time, CASx low to TRG high for DRAM read cycles		20		20		ns
t <sub>d</sub> (GHD) Delay time, TRG high before data applied at DQ	t <sub>OED</sub>	15		15		ns

† Timing measurements are referenced to V<sub>IL</sub> max and V<sub>IH</sub> min.

NOTES: 12. The minimum value is measured when t<sub>d</sub>(RLCL) is set to t<sub>d</sub>(RLCL) min as a reference.

13. Either t<sub>h</sub>(RHrd) or t<sub>d</sub>(CHrd) must be satisfied for a read cycle.

14. Output-enable-controlled write. Output remains in the high-impedance state for the entire cycle.

15. CBR refresh operation only

16. Read-modify-write operation only

17. TRG must disable the output buffers prior to applying data to the DQ pins.

18. The maximum value is specified only to assure RAS access time.



timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)<sup>†</sup>

	ALT. SYMBOL	'55161-70		'55161-80		UNIT	
		MIN	MAX	MIN	MAX		
t <sub>d</sub> (RLTH)	Delay time, $\overline{RAS}$ low to $\overline{TRG}$ high (see Note 19)	t <sub>RTH</sub>	55	60		ns	
t <sub>d</sub> (RLSH)	Delay time, $\overline{RAS}$ low to first SC high after $\overline{TRG}$ high (see Note 20)	t <sub>RS</sub>	70	80		ns	
t <sub>d</sub> (RLCA)	Delay time, $\overline{RAS}$ low to column address valid	t <sub>RAD</sub>	15	35	15	40	ns
t <sub>d</sub> (GLRH)	Delay time, $\overline{TRG}$ low to $\overline{RAS}$ high	t <sub>ROH</sub>	20	20		ns	
t <sub>d</sub> (CLSH)	Delay time, $\overline{CASx}$ low to first SC high after $\overline{TRG}$ high (see Note 20)	t <sub>CS</sub>	20	25		ns	
t <sub>d</sub> (SCTR)	Delay time, SC high to $\overline{TRG}$ high (see Notes 19 and 20)	t <sub>TS</sub>	5	5		ns	
t <sub>d</sub> (THRH)	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ high (see 19)	t <sub>TRD</sub>	-10	-10		ns	
t <sub>d</sub> (THRL)	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ low (see Note 21)	t <sub>TRP</sub>	50	60		ns	
t <sub>d</sub> (THSC)	Delay time, $\overline{TRG}$ high to SC high (see Note 19)	t <sub>TS</sub>	15	20		ns	
t <sub>d</sub> (RHMS)	Delay time, $\overline{RAS}$ high to last (most significant) rising edge of SC before boundary switch during split-register-transfer read cycles		20	20		ns	
t <sub>d</sub> (CLTH)	Delay time, $\overline{CASx}$ low to $\overline{TRG}$ high in real-time-transfer read cycles	t <sub>CTH</sub>	15	15		ns	
t <sub>d</sub> (CASH)	Delay time, column address to first SC in early-load-transfer read cycles	t <sub>AS</sub>	25	30		ns	
t <sub>d</sub> (CAGH)	Delay time, column address to $\overline{TRG}$ high in real-time-transfer read cycles	t <sub>ATH</sub>	20	20		ns	
t <sub>d</sub> (DCL)	Delay time, data to $\overline{CASx}$ low	t <sub>DZC</sub>	0	0		ns	
t <sub>d</sub> (DGL)	Delay time, data to $\overline{TRG}$ low	t <sub>DZO</sub>	0	0		ns	
t <sub>d</sub> (MSRL)	Delay time, last (most significant) rising edge of SC to $\overline{RAS}$ low before boundary switch during split-register-transfer read cycles		20	20		ns	
t <sub>d</sub> (SCQSF)	Delay time, last (127 or 255) rising edge of SC to QSF switching at the boundary during split-register-transfer read cycles (see Note 22)	t <sub>SQD</sub>		25	30	ns	
t <sub>d</sub> (CLQSF)	Delay time, $\overline{CASx}$ low to QSF switching in transfer-read cycles (see Note 22)	t <sub>CQD</sub>		30	35	ns	
t <sub>d</sub> (GHQSF)	Delay time, $\overline{TRG}$ high to QSF switching in transfer-read cycles (see Note 22)	t <sub>TQD</sub>		25	30	ns	
t <sub>d</sub> (RLQSF)	Delay time, $\overline{RAS}$ low to QSF switching in transfer-read cycles (see Note 22)	t <sub>RQD</sub>		70	75	ns	
t <sub>r</sub> (MA)	Refresh time interval, memory	t <sub>REF</sub>		8	8	ms	
t <sub>t</sub>	Transition time	t <sub>T</sub>	3	50	3	50	ns

<sup>†</sup> Timing measurements are referenced to V<sub>IL</sub> max and V<sub>IH</sub> min.

NOTES: 19. Real-time-load transfer read or late-load-transfer read cycle only

20. Early-load-transfer read cycle only

21. Full-register-(read) transfer cycles only

22. Switching times for QSF output are measured with a load equivalent to 1 TTL load and 30 pF, and output reference level is V<sub>OH</sub> / V<sub>OL</sub> = 2 V / 0.8 V.

PARAMETER MEASUREMENT INFORMATION

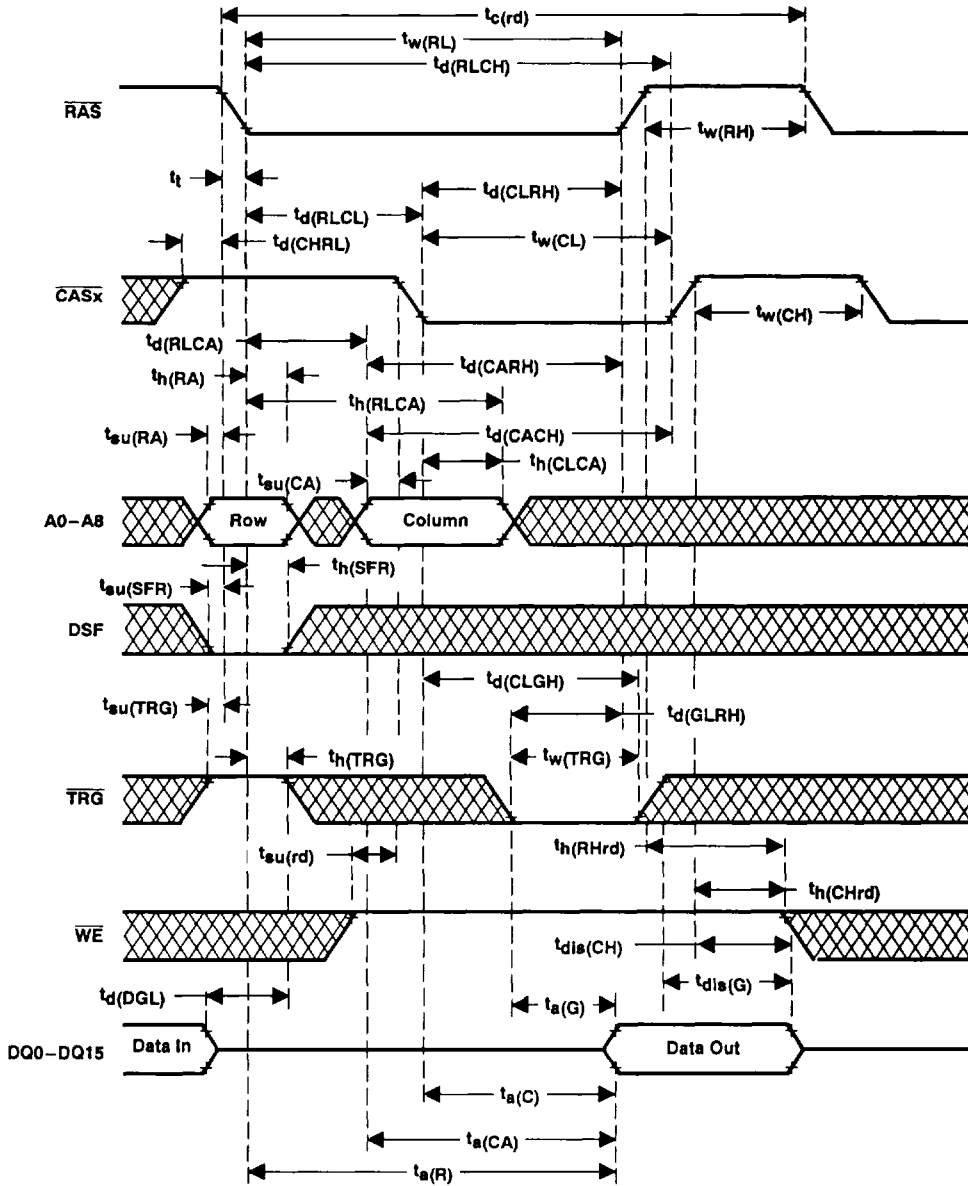


Figure 27. Read-Cycle Timing With  $\overline{\text{CASx}}$ -Controlled Output

PARAMETER MEASUREMENT INFORMATION

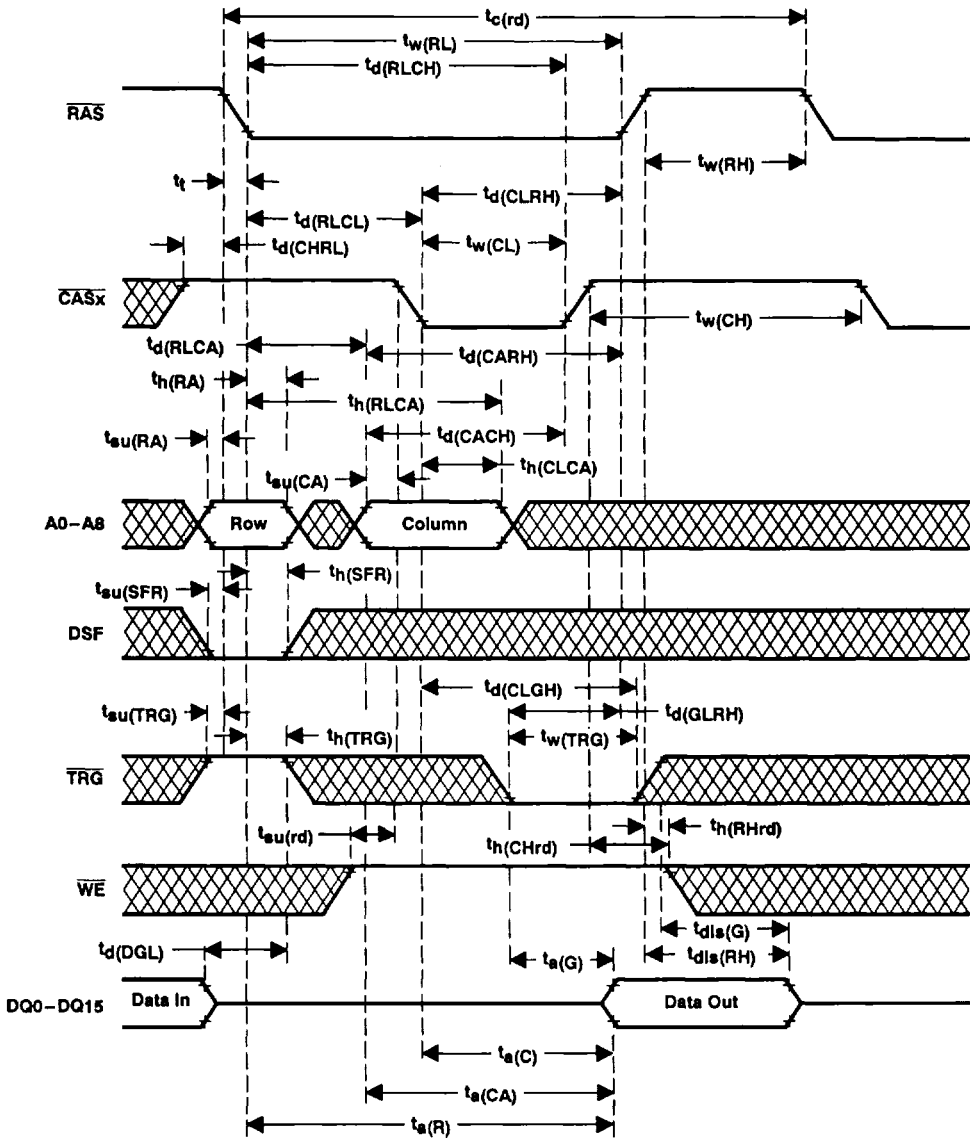


Figure 28. Read-Cycle Timing With  $\overline{RAS}$ -Controlled Output

PARAMETER MEASUREMENT INFORMATION

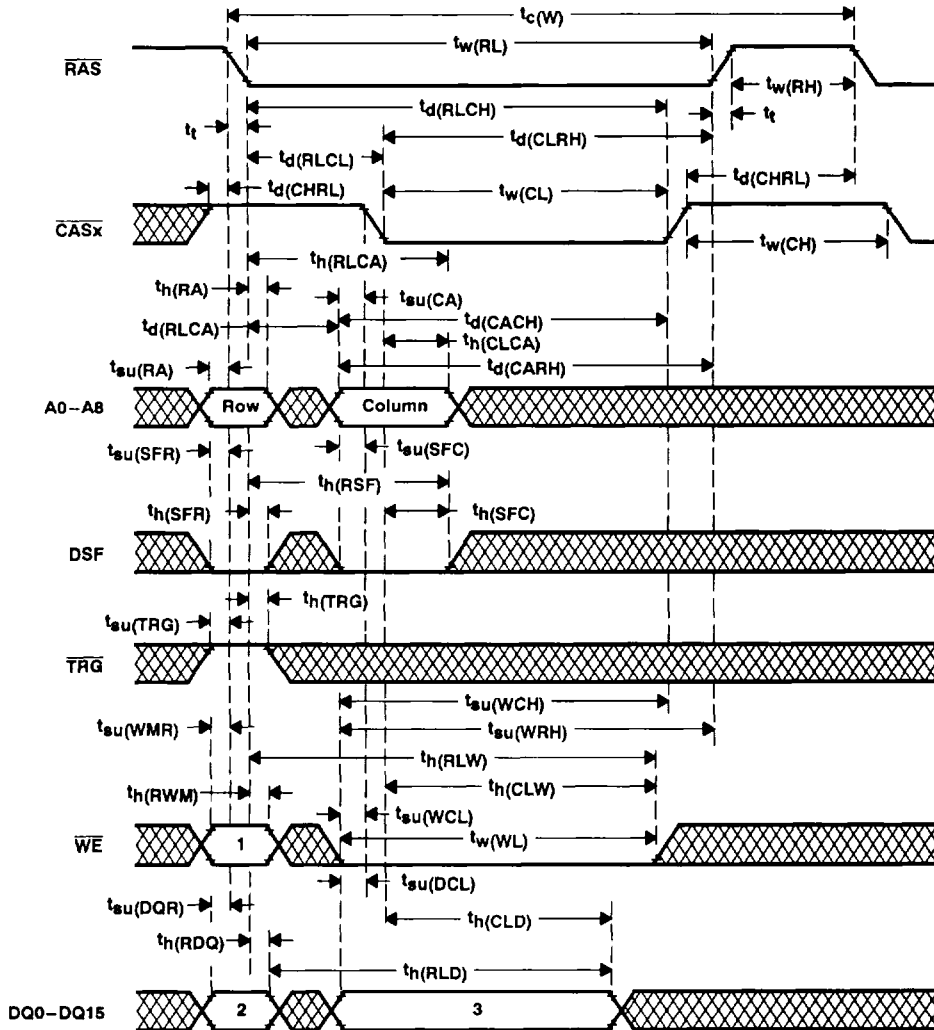


Figure 29. Early-Write-Cycle Timing

Table 4. Early-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data



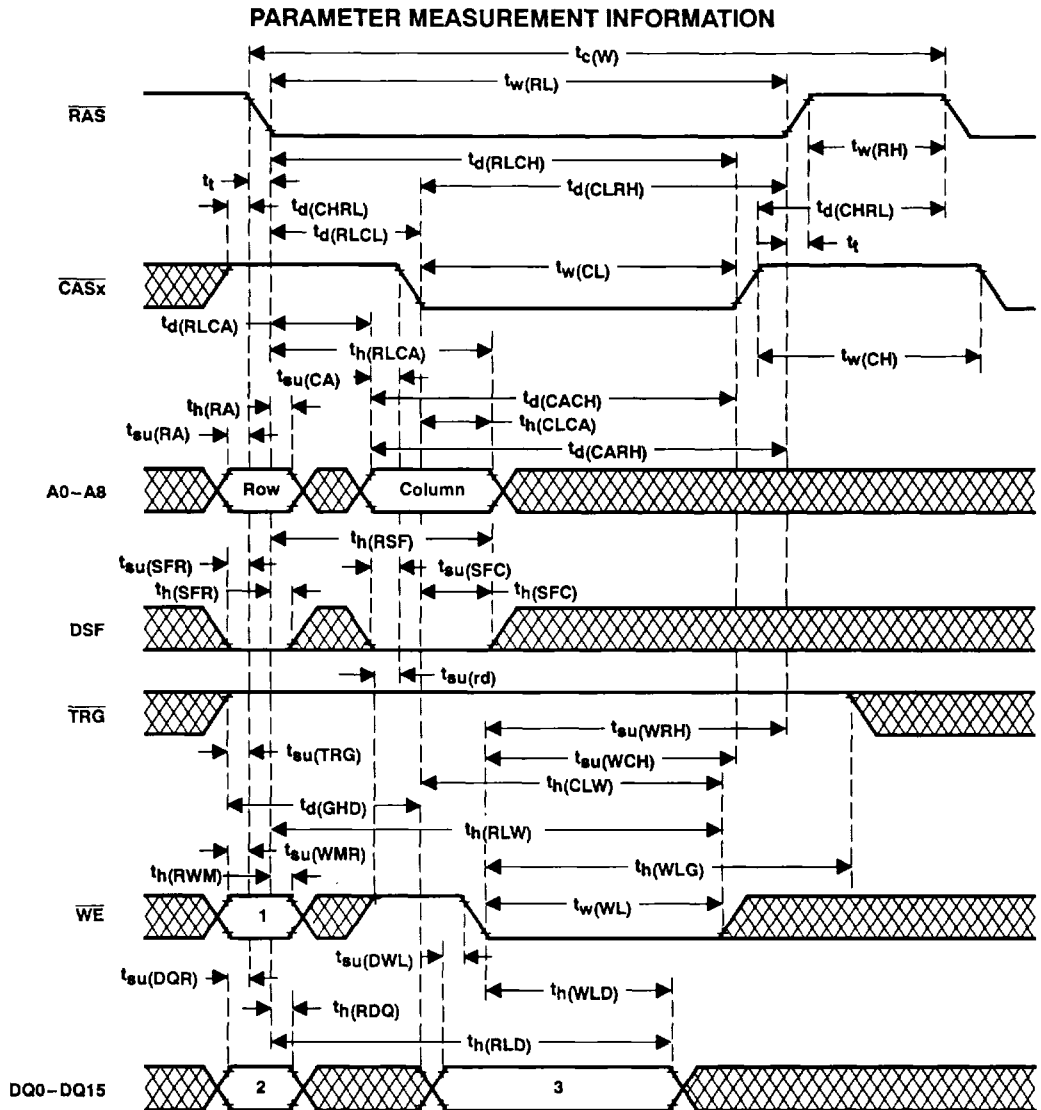


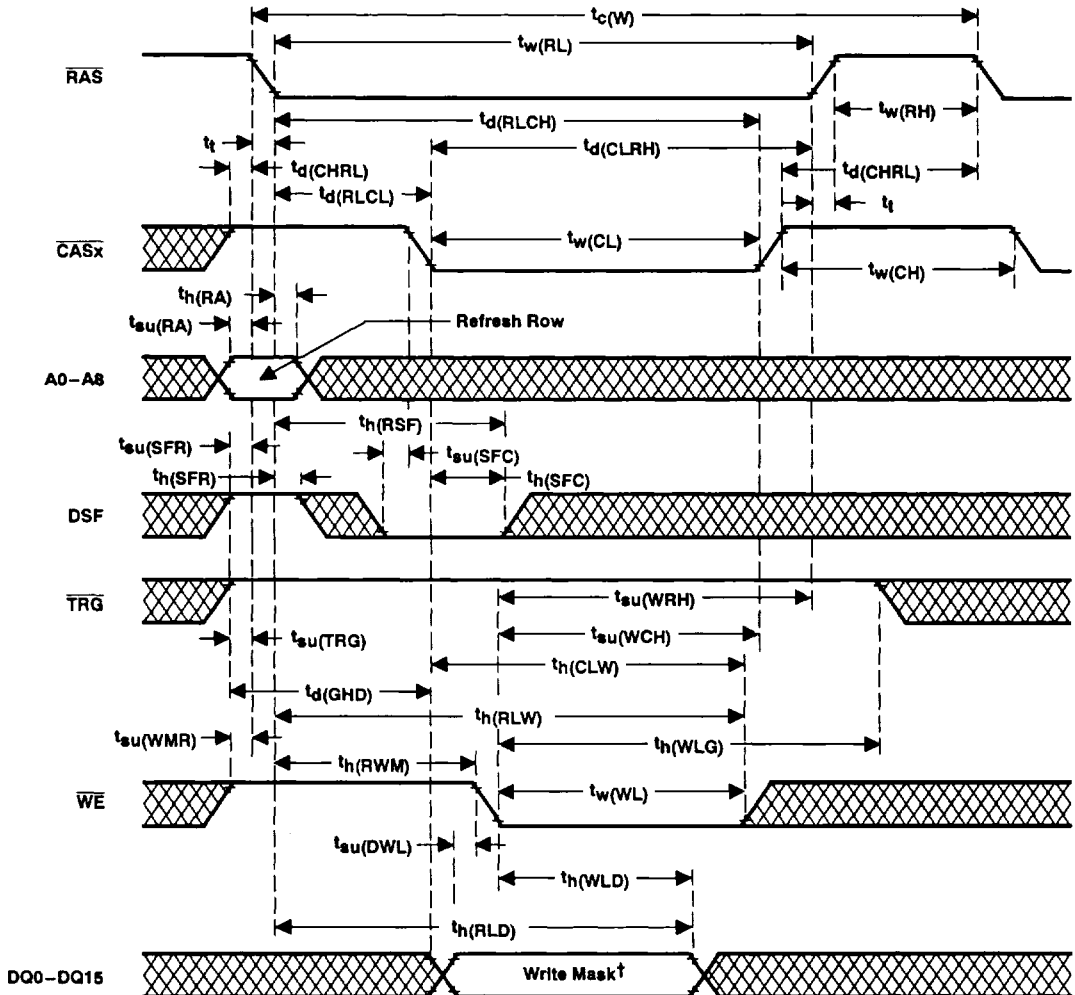
Figure 30. Late-Write-Cycle Timing (Output-Enable-Controlled Write)

Table 5. Late-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data



PARAMETER MEASUREMENT INFORMATION

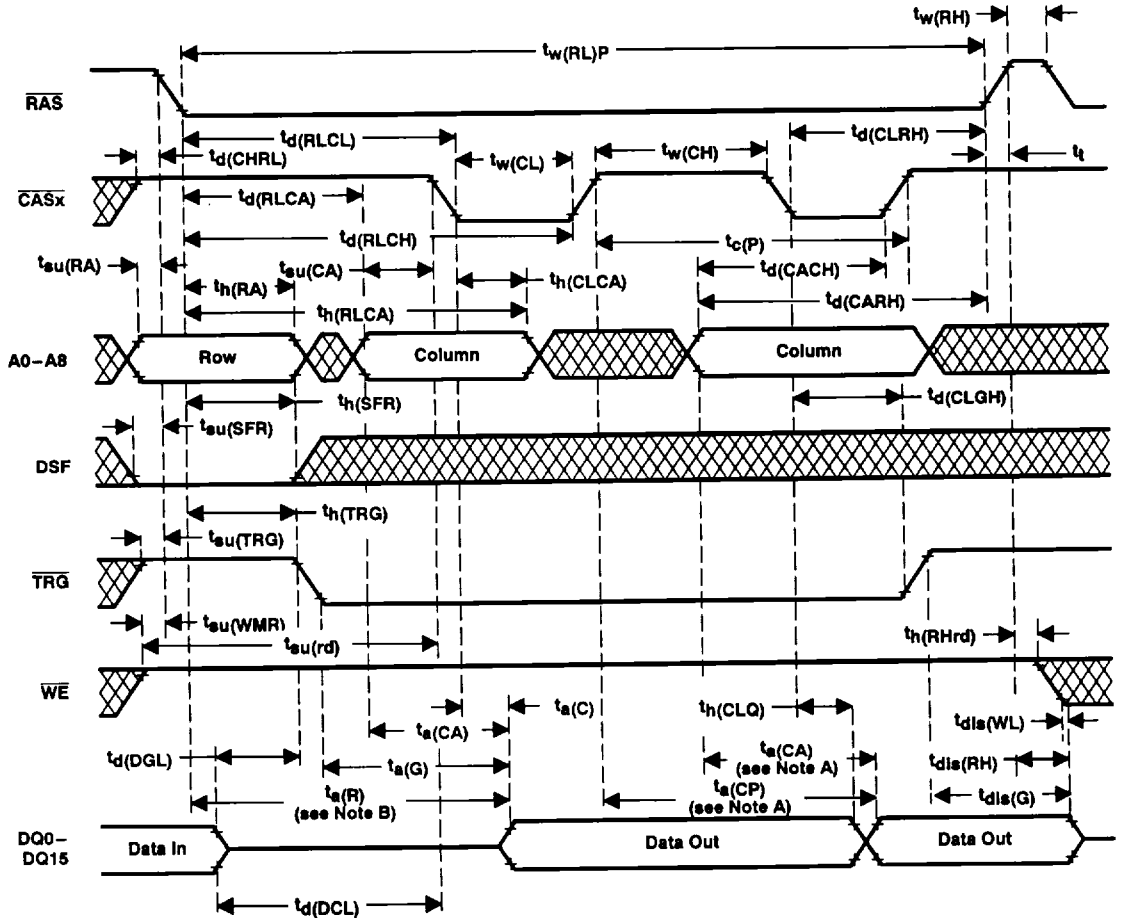


† Load-write-mask-register cycle puts the device into the persistent write-per-bit mode.

Figure 32. Load-Write-Mask-Register-Cycle Timing (Late-Write Load)



PARAMETER MEASUREMENT INFORMATION

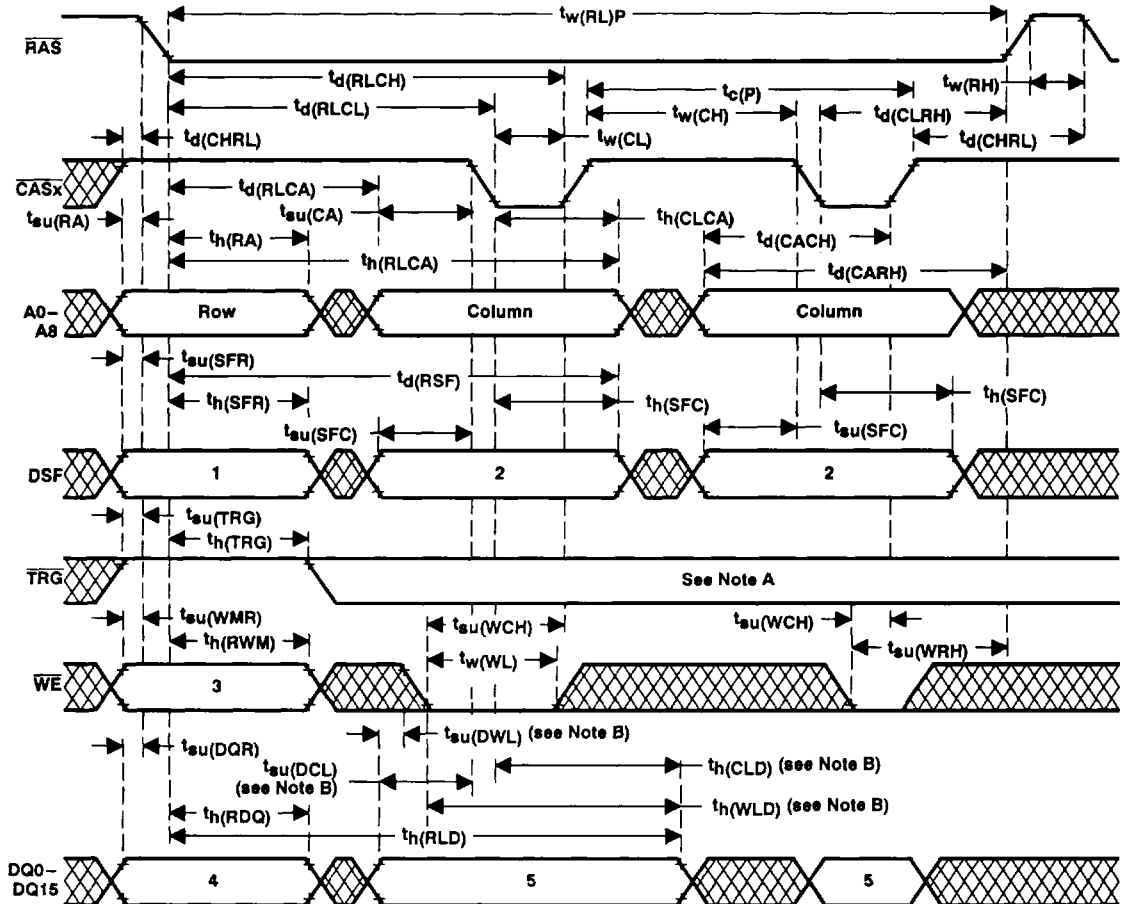


- NOTES:
- Access time is  $t_a(CP)$  or  $t_a(CA)$  dependent.
  - Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
  - A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated and the proper polarity of DSF is selected on the falling edge of RAS and CASx to select the desired write mode (normal, block write, etc.).

Figure 34. Enhanced-Page-Mode Read-Cycle Timing



PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to the first falling edge of  $\overline{\text{CASx}}$  or the falling edge of  $\overline{\text{WE}}$ , whichever occurs later  
 B. A read cycle or a read-modify-write cycle can be intermixed with write cycles, observing read and read-modify-write timing specifications. To assure page-mode cycle time, TRG must remain high throughout the entire page-mode operation if the late write feature is used. If the early write-cycle timing is used, the state of TRG is a don't care after the minimum period  $t_h(\text{TRG})$  from the falling edge of  $\overline{\text{RAS}}$ .

Figure 35. Enhanced-Page-Mode Write-Cycle Timing  
 Table 7. Enhanced-Page-Mode Write-Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation (nonmasked)	L	L	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	L	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	L	L	Don't care	Valid data
Load-write mask on either the first falling edge of $\overline{\text{CASx}}$ or the falling edge of $\overline{\text{WE}}$ , whichever occurs later. <sup>†</sup>	H	L	H	Don't care	Write mask

<sup>†</sup> Load-write-mask-register cycle puts the device in the persistent write-per-bit mode. Column address at the falling edge of  $\overline{\text{CASx}}$  is a don't care during this cycle.











PARAMETER MEASUREMENT INFORMATION

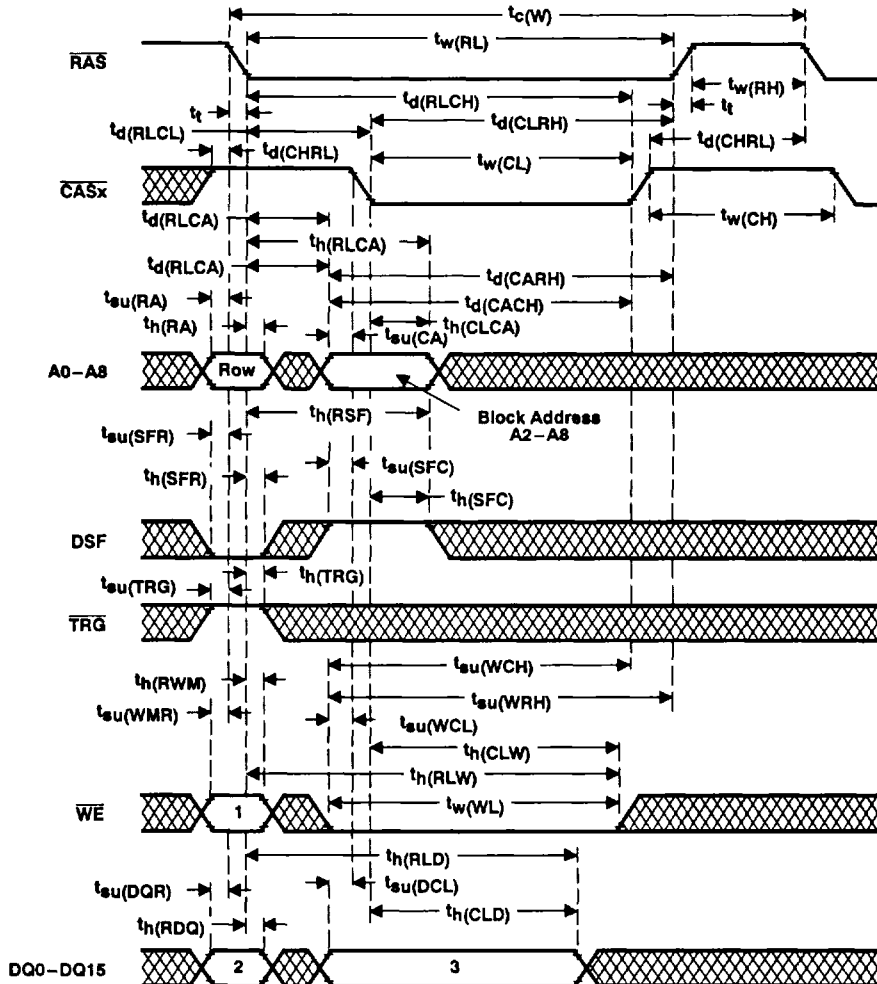


Figure 40. Block-Write-Cycle Timing (Early Write)

Table 9. Block-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent write-per-bit	L	Write mask	Column mask
Block-write operation with persistent write-per-bit	L	Don't care	Column mask

Write-mask data 0: I/O write disable

1: I/O write enable

Column-mask data  $DQ_i - DQ_i + 3$  0: column-write disable

( $i = 0, 4, 8, 12$ ) 1: column-write enable

Example:

$DQ_0$  — column 0 (address  $A_1 = 0, A_0 = 0$ )

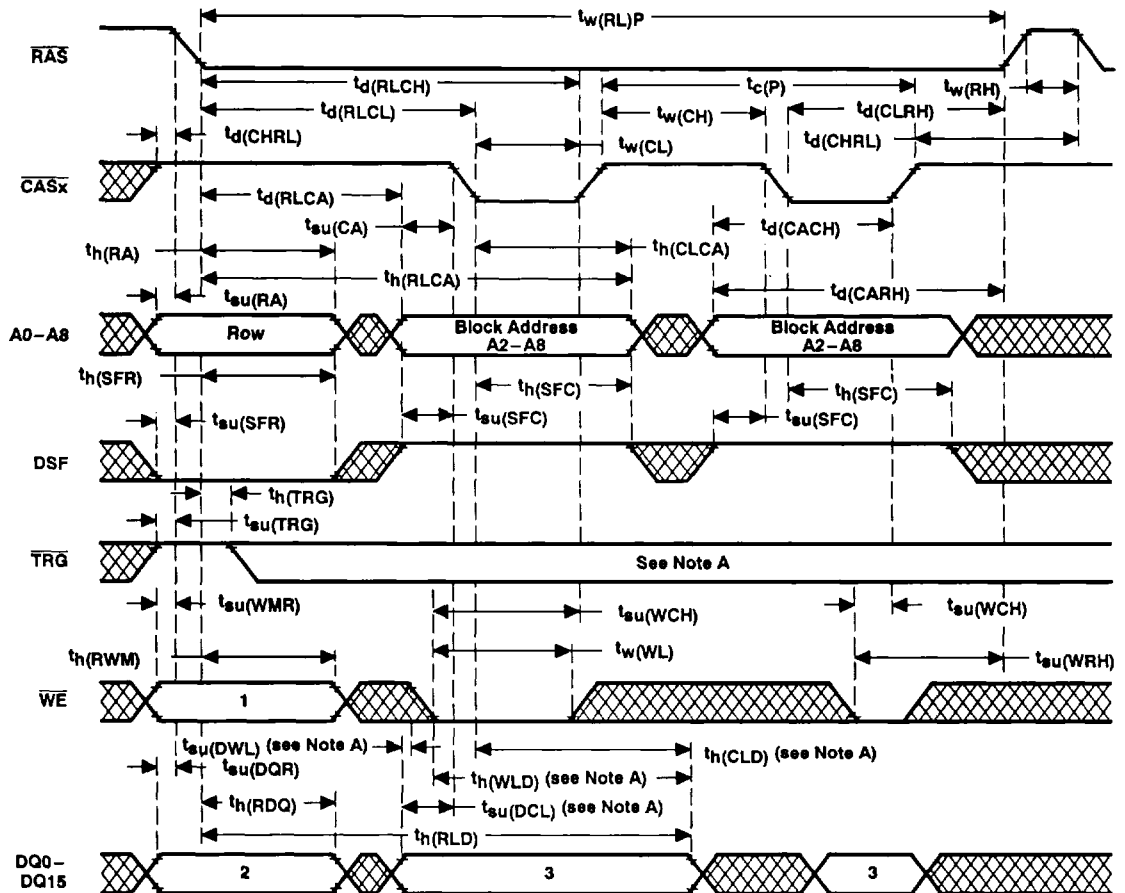
$DQ_1$  — column 1 (address  $A_1 = 0, A_0 = 1$ )

$DQ_2$  — column 2 (address  $A_1 = 1, A_0 = 0$ )

$DQ_3$  — column 3 (address  $A_1 = 1, A_0 = 1$ )



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Referenced to the first falling edge of  $\overline{\text{CASx}}$  or the falling edge of  $\overline{\text{WE}}$ , whichever occurs later  
 B. To assure page-mode cycle time,  $\overline{\text{TRG}}$  must remain high throughout the entire page-mode operation. If the late-write feature is used, if the early-write cycle timing is used, the state of  $\overline{\text{TRG}}$  is a don't care after the minimum period  $t_h(\text{TRG})$  from the falling edge of  $\overline{\text{RAS}}$ .

Figure 42. Enhanced-Page-Mode Block-Write-Cycle Timing

Table 11. Enhanced-Page-Mode Block-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent write-per-bit	L	Write mask	Column mask
Block-write operation with persistent write-per-bit	L	Don't care	Column mask

Write-mask data 0: I/O write disable  
 1: I/O write enable  
 Column-mask data  $\text{DQi} - \text{DQi} + 3$  0: column-write disable  
 ( $i = 0, 4, 8, 12$ ) 1: column-write enable

Example:  
 DQ0 — column 0 (address  $\text{A1} = 0, \text{A0} = 0$ )  
 DQ1 — column 1 (address  $\text{A1} = 0, \text{A0} = 1$ )  
 DQ2 — column 2 (address  $\text{A1} = 1, \text{A0} = 0$ )  
 DQ3 — column 3 (address  $\text{A1} = 1, \text{A0} = 1$ )



PARAMETER MEASUREMENT INFORMATION

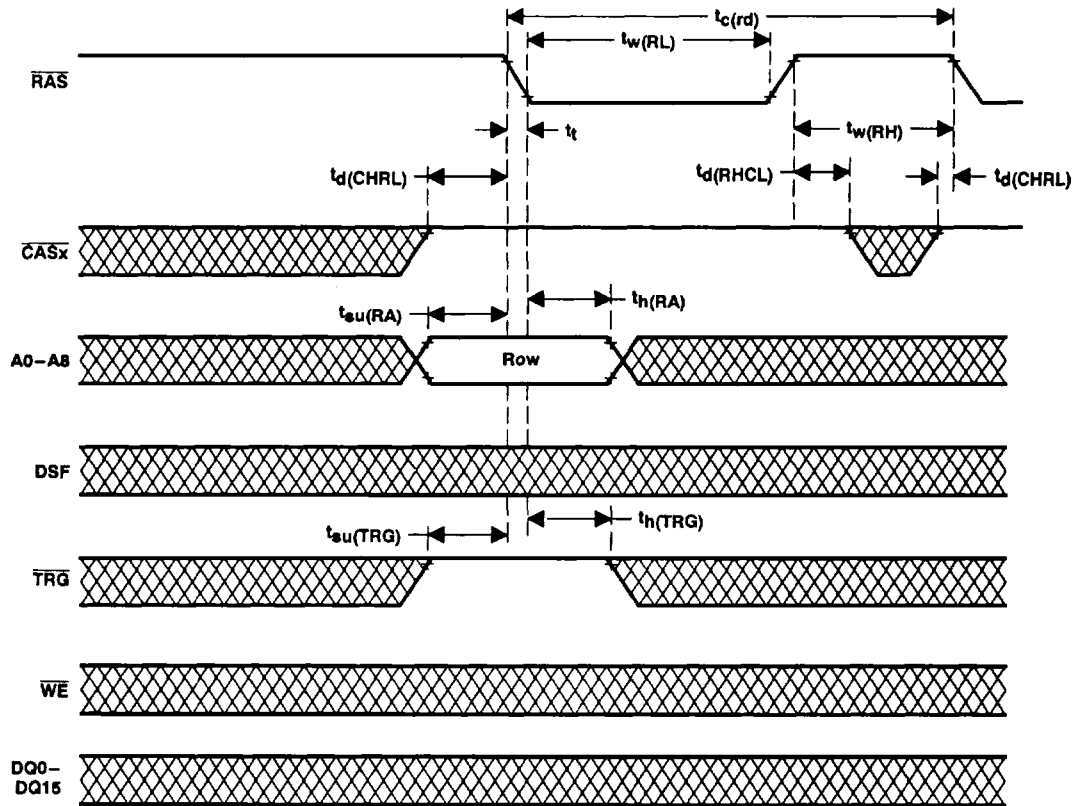


Figure 43. RAS-Only Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

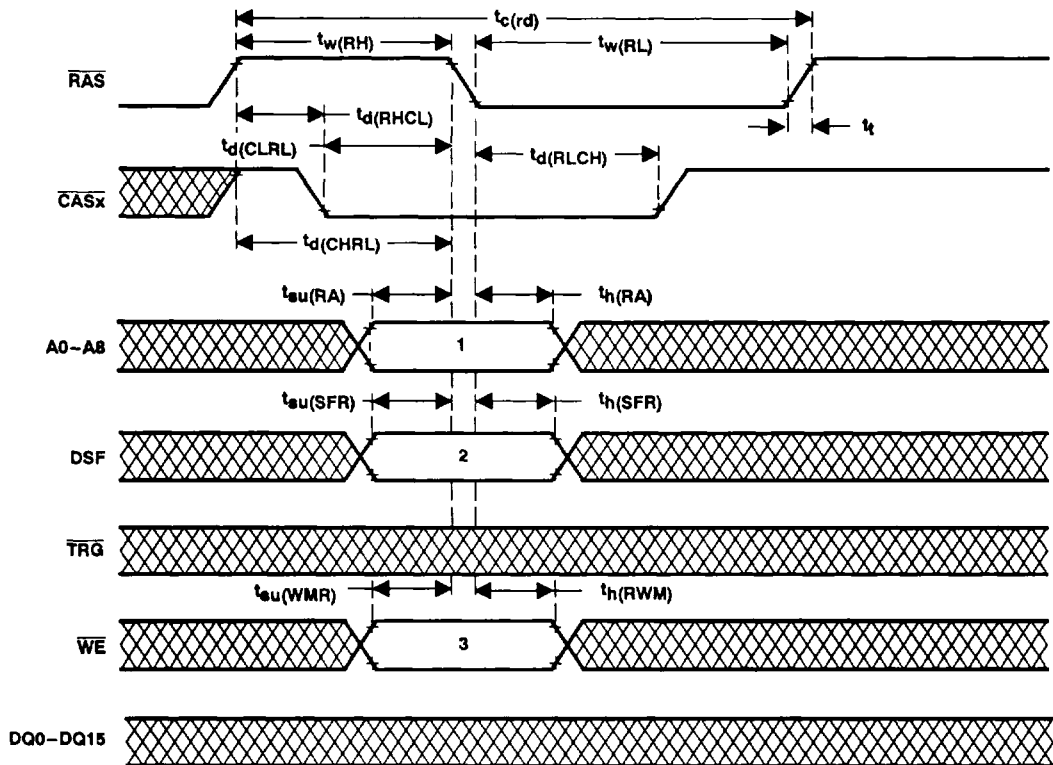


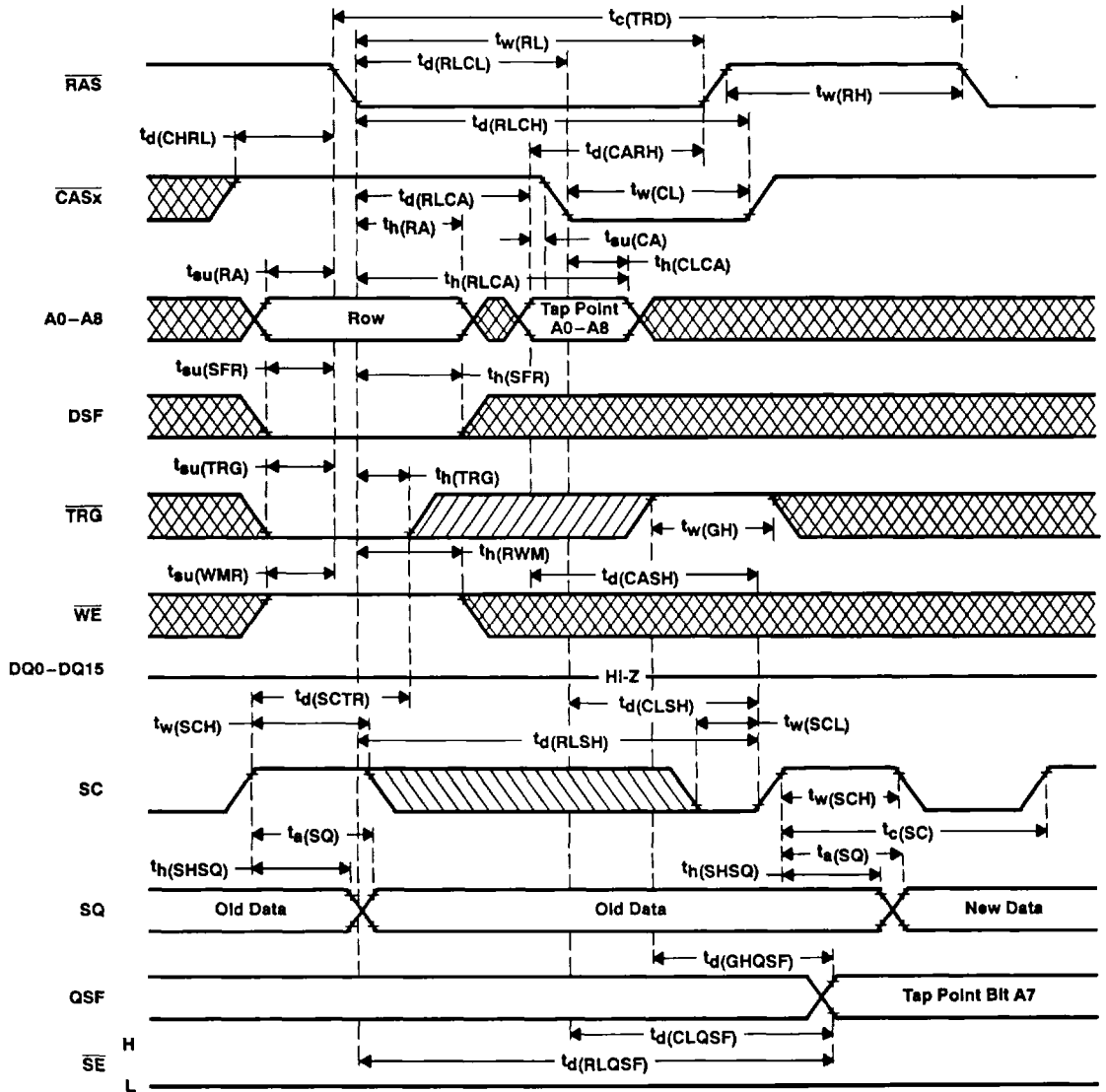
Figure 44. CBR-Refresh-Cycle Timing

Table 12. CBR-Cycle State Table

CYCLE	STATE		
	1	2	3
CBR refresh with option reset	Don't care	L	H
CBR refresh with no reset	Don't care	H	H
CBR refresh with stop-point set and no reset	Stop address	H	L



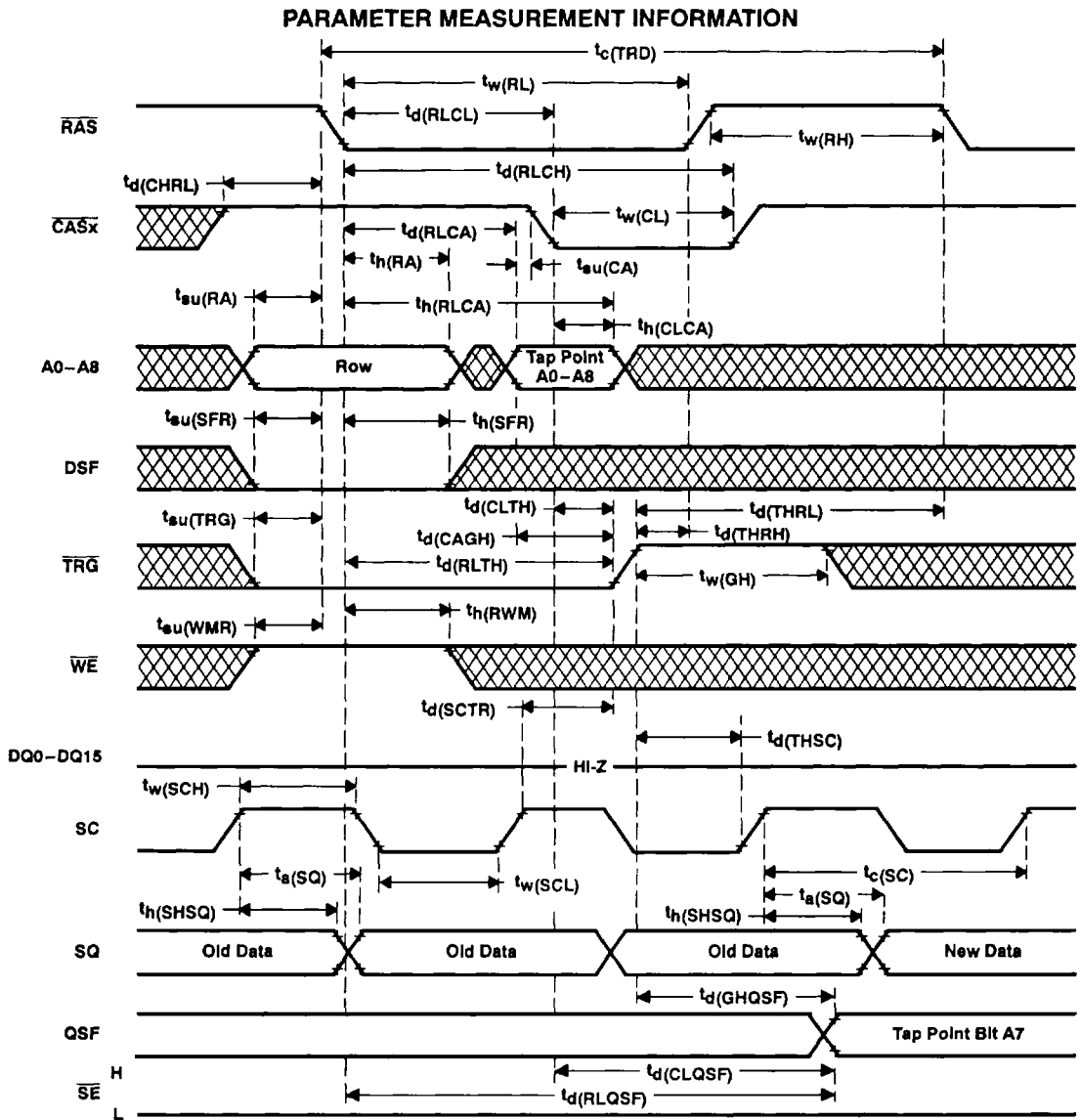
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. DQ outputs remain in the high-impedance state for the entire memory-to-data-register transfer cycle. The memory-to-data-register transfer cycle is used to load the data registers in parallel from the memory array. The 256 locations in each data register are written into from the 256 corresponding columns of the selected row.
- B. Once data is transferred into the data registers, the SAM is in the serial-read mode (i.e., the SQ is enabled), allowing data to be shifted out of the registers. Also, the first bit to read from the data register after  $\overline{\text{TRG}}$  has gone high must be activated by a positive transition of SC.
- C. A0 - A7: register tap point; A8: identifies the DRAM row half
- D. Early-load operation is defined as  $t_h(\text{TRG})_{\text{min}} < t_h(\text{TRG}) < t_d(\text{RLTH})_{\text{min}}$ .

Figure 46. Full-Register Transfer-Read Timing, Early-Load Operations



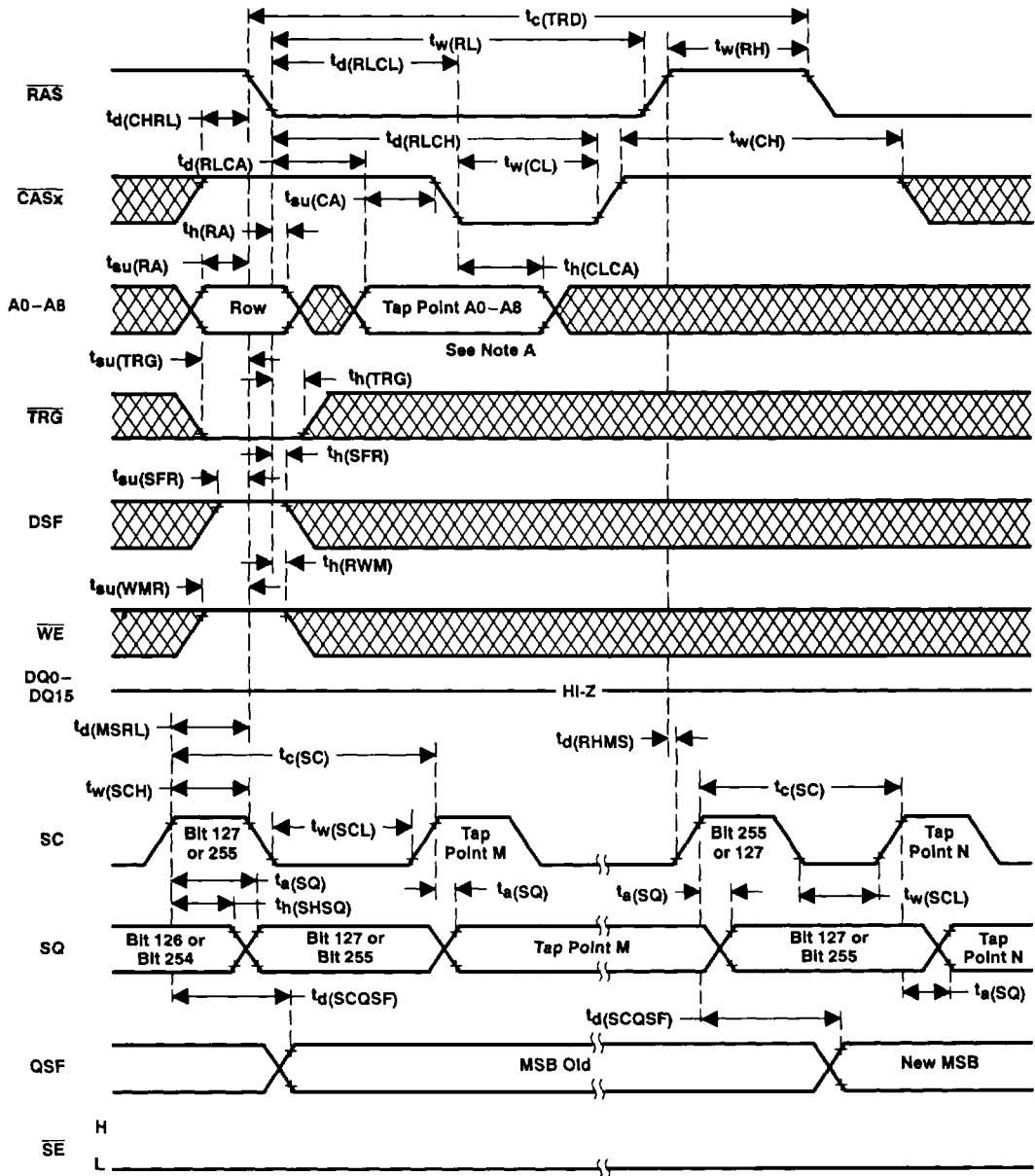


- NOTES: A. DQ outputs remain in the high-impedance state for the entire memory-to-data-register transfer cycle. The memory-to-data-register transfer cycle is used to load the data registers in parallel from the memory array. The 256 locations in each data register are written into from the 256 corresponding columns of the selected row.
- B. Once data is transferred into the data registers, the SAM is in the serial-read mode (i.e., the SQ is enabled), allowing data to be shifted out of the registers. Also, the first bit to read from the data register after TRG has gone high must be activated by a positive transition of SC.
- C. A0-A7: register tap point; A8: Identifies the DRAM row half
- D. Late load operation is defined as  $t_d(\text{THRH}) < 0$  ns.

**Figure 47. Full-Register Transfer Read-Timing, Real-Time Load Operation/Late-Load Operation**



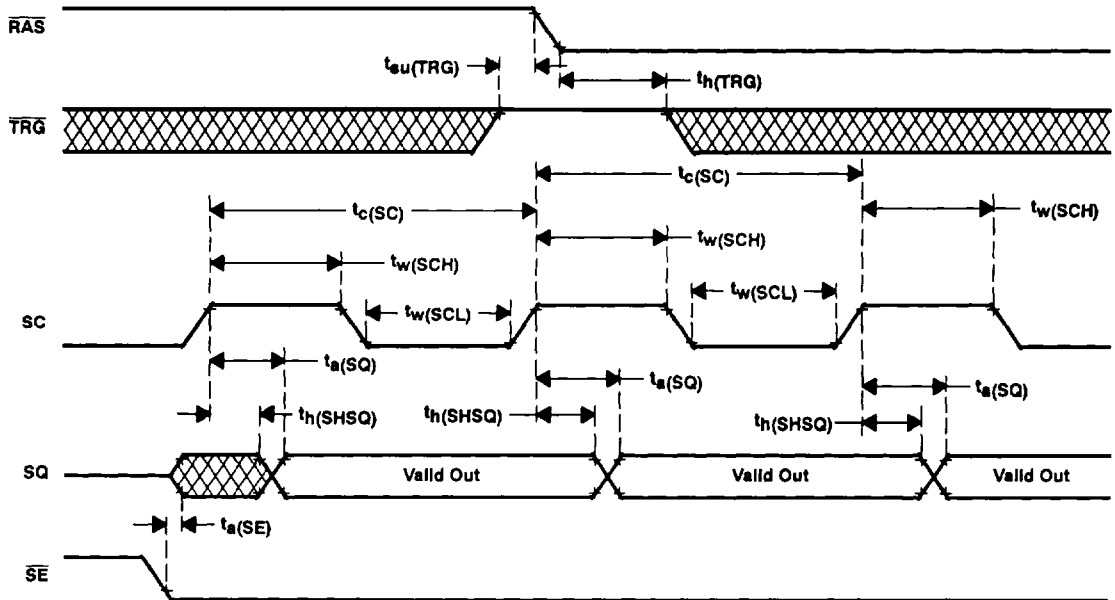
PARAMETER MEASUREMENT INFORMATION



NOTE A: A0-A6: tap point of the given half; A7: don't care; A8: identifies the DRAM row half

Figure 48. Split-Register-Transfer-Read Timing

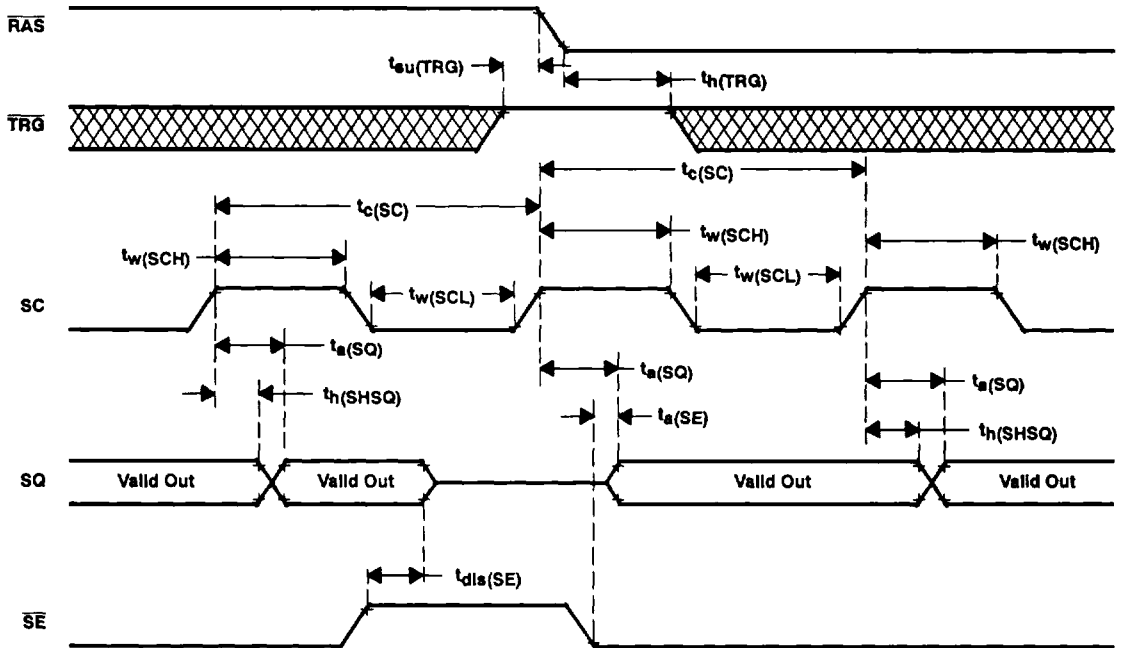
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. While the data is being read through the serial-data register,  $\overline{TRG}$  is a don't care; however  $\overline{TRG}$  must be held high when  $\overline{RAS}$  goes low. This is to avoid the initiation of a register-data transfer operation.  
 B. The serial data-out cycle is used to read data out of the data registers. Before data can be read via SQ, the device must be put into the read mode by performing a transfer-read cycle.

Figure 49. Serial-Read-Cycle Timing ( $\overline{SE} = V_{IL}$ )

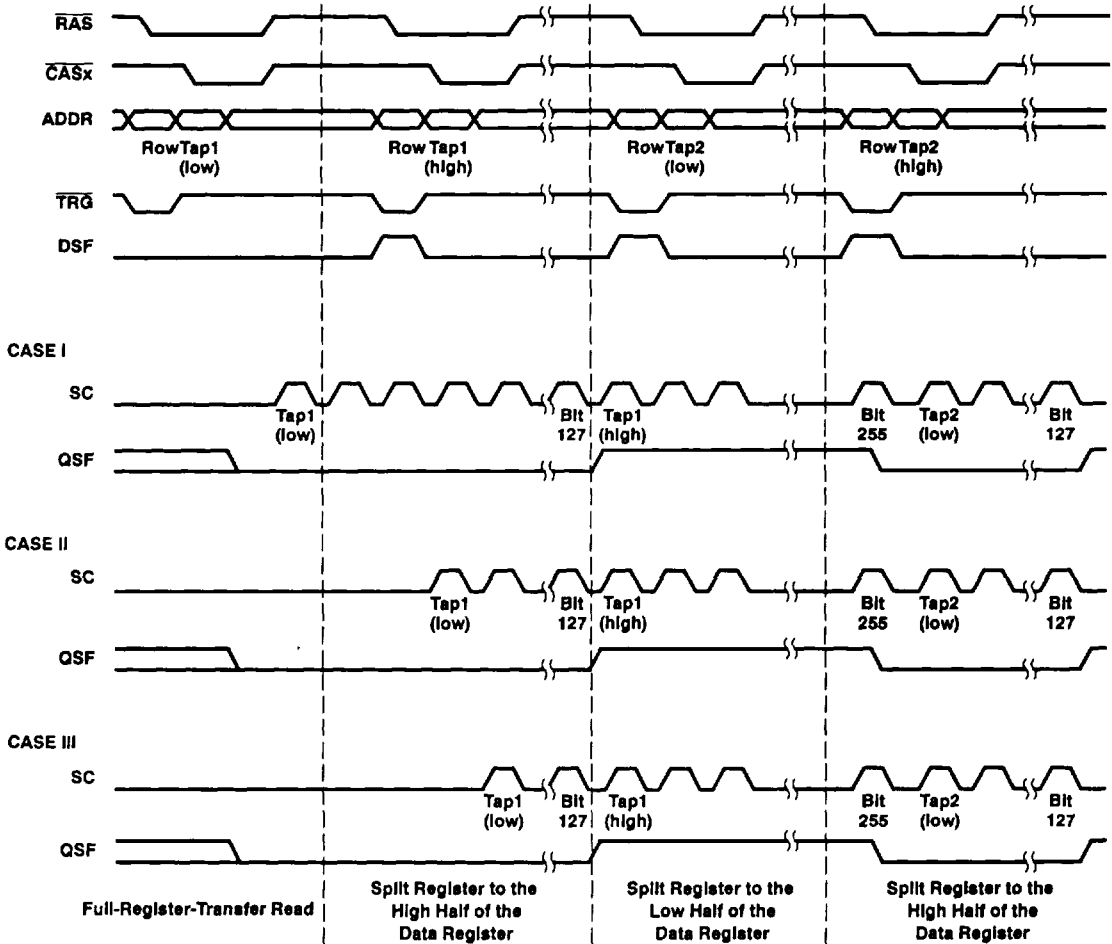
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. While the data is being read through the serial-data register,  $\overline{TRG}$  is a don't care; however  $\overline{TRG}$  must be held high when  $\overline{RAS}$  goes low. This is to avoid the initiation of a register-data transfer operation.  
 B. The serial data-out cycle is used to read data out of the data registers. Before data can be read via  $SQ$ , the device must be put into the read mode by performing a transfer-read cycle.

Figure 50. Serial-Read Timing ( $\overline{SE}$ -Controlled Read)

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. To achieve proper split-register operation, a full-register-transfer read must be performed before the first split-register-transfer cycle. This is necessary to initialize the data register and the starting tap location. First serial access can begin either after the full-register-transfer read cycle (CASE I), during the first split-register-transfer cycle (CASE II), or even after the first split-register-transfer cycle (CASE III). There is no minimum requirement of SC clock between the full-register-transfer-read cycle and the first split-register cycle.
- B. A split-register transfer into the inactive half is not allowed until  $t_d(\text{MSRL})$  is met.  $t_d(\text{MSRL})$  is the minimum delay time between the rising edge of the serial clock of the last bit (bit 127 or 255) and the falling edge of RAS of the split-register-transfer cycle into the inactive half. After the  $t_d(\text{MSRL})$  requirement is met, the split-register transfer into the inactive half must also satisfy the minimum  $t_d(\text{RHMS})$  requirement.  $t_d(\text{RHMS})$  is the minimum delay time between the rising edge of RAS of the split-register-transfer cycle into the inactive half and the rising edge of the serial clock of the last bit (bit 127 or 255).

Figure 51. Split-Register Operating Sequence

device symbolization

