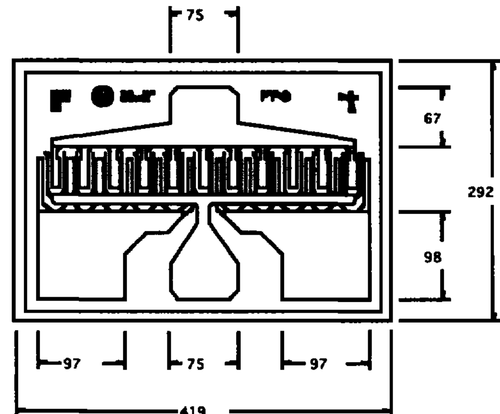
MICROWAVE TECHNOLOGY

MwT-9

18 GHz High Power GaAs FET



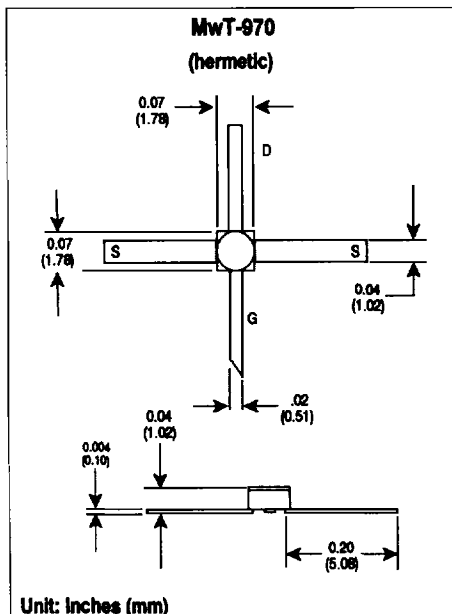
- **+26 dBm OUTPUT POWER AT 12 GHz**
- **8.5 dB SMALL SIGNAL GAIN AT 12 GHz**
- **0.3 MICRON REFRACTORY METAL/GOLD GATE**
- **750 MICRON GATE WIDTH**
- **CHOICE OF CHIP AND THREE PACKAGE TYPES**

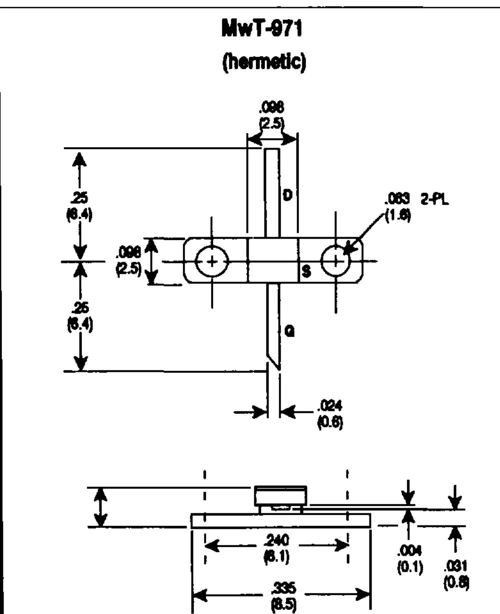
DESCRIPTION

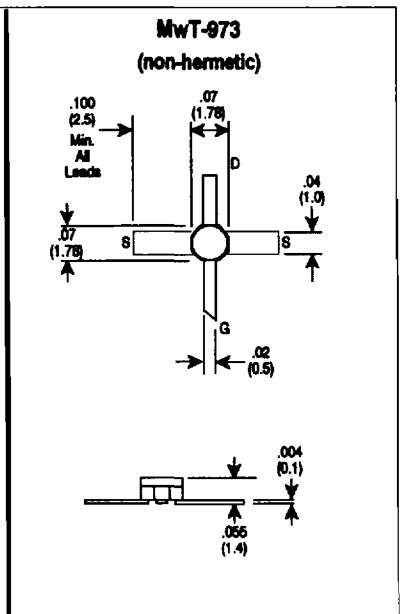
The MwT-9 is a GaAs MESFET device whose nominal quarter-micron gate length and 750 micron gate width make it ideally suited to applications requiring high-gain in the 500 MHz to 18 GHz frequency range with power outputs ranging from +24 to +26 dBm. It can be easily matched as the driver stage in high power communications amplifiers or in broad-band military amplifiers and operated at reduced bias in battery powered wireless communications devices. The chip is produced using MwT's reliable metal system and all devices are screened to insure reliability. All chips are passivated using MwT's patented "Diamond-Like Carbon" process for durability with no degradation in performance. Designers can use MwT's unique BIN selection feature to choose devices from narrow Idss ranges, insuring consistent circuit operation.

RF SPECIFICATIONS AT Ta = 25°C

				MwT-9 SP MwT-970 SP MwT-971 SP MwT-973 SP		MwT-9 HP MwT-970 HP MwT-971 HP MwT-973 HP	
SYMBOL	**PARAMETERS AND CONDITIONS**	**FREQ**	**UNITS**	**MIN**	**TYP**	**MIN**	**TYP**
P1dB	Output Power at 1dB Compression VDS=6.0 V IDS=0.6 IDSS=120mA	12 GHz	dBm	24.5	25.5	25.0	26.0
SSG	Small Signal Gain VDS=6.0 V IDS=0.6 IDSS=120mA	12 GHz	dB	7.5	8.0	8.0	8.5
PAE	Power Added Efficiency VDS=6.0 V IDS=0.6 IDSS=120mA	12 GHz	%	25	30	30	35
IDSS	Recommended IDSS Range for Optimum P1dB		mA		150-234		198-270







DC SPECIFICATIONS AT Ta = 25 °C

SYMBOL	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
Idss	Saturated Drain Current Vds=4.0 V VGS=0.0 V	mA	78		282
Gm	Transconductance Vds=2.0 V VGS=0.0 V	mS	95	120	
Vp	Pinch-off Voltage Vds=3.0 V IDS=5.0 mA	V		-2.0	-5.0
BVGSO	Gate-to-Source Breakdown Voltage Igs=-0.5 mA	V	-6.0	-12.0	
BVGDO	Gate-to-Drain Breakdown Voltage Igd=-0.5 mA	V	-8.0	-12.0	
Rth	Thermal Resistance* MwT-9 Chip,971 MwT-970,973	°C/W		70 175**	

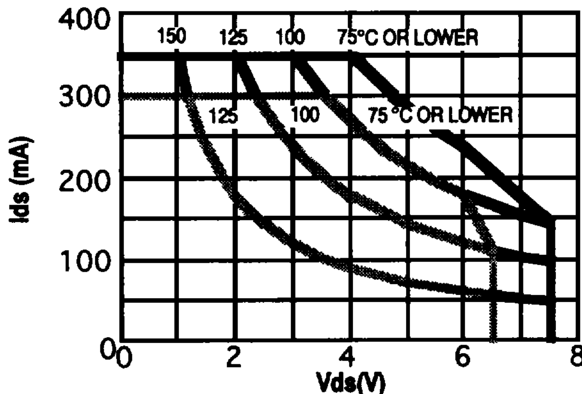
* Overall Rth depends on case mounting

MAXIMUM RATINGS AT Ta = 25 ° C

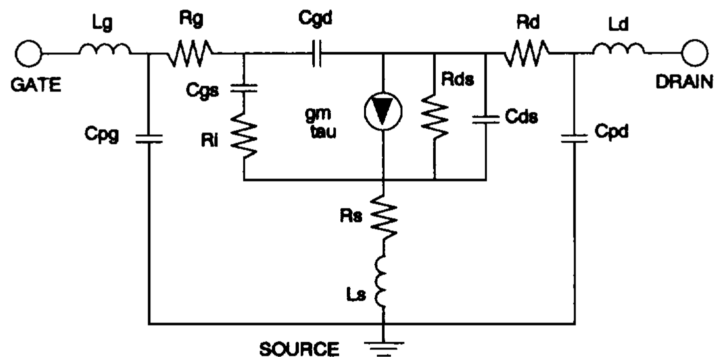
SYMBOL	PARAMETER	UNITS	CONT MAX[1]	ABSOLUTE MAX[2]
VDS	Drain to Source Voltage	V	See Safe Operating Limits	
Tch	Channel Temperature	°C	+150	+175
Tst	Storage Temperature	°C	-65 to +150	+175
Pin	RF Input Power	mW	300	450

NOTES: 1. Exceeding any one of these limits in continuous operation may reduce the mean-time-to-failure below the design goals.
2. Exceeding any one of these limits may cause permanent damage.

SAFE OPERATING LIMITS vs. Case Temperature



DEVICE EQUIVALENT CIRCUIT MODEL

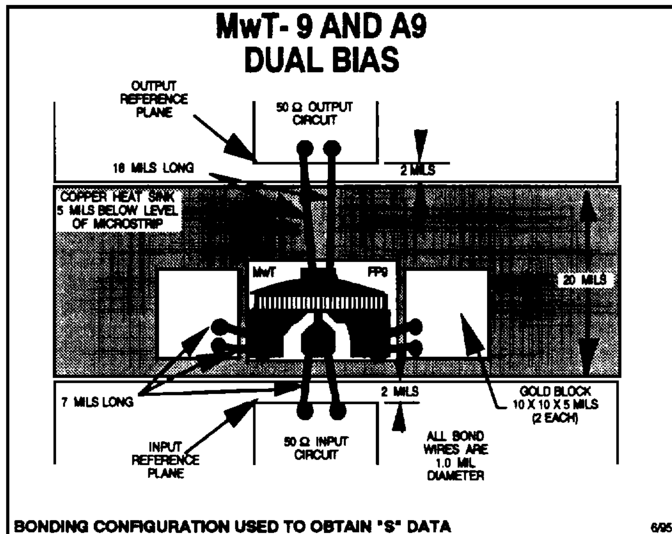


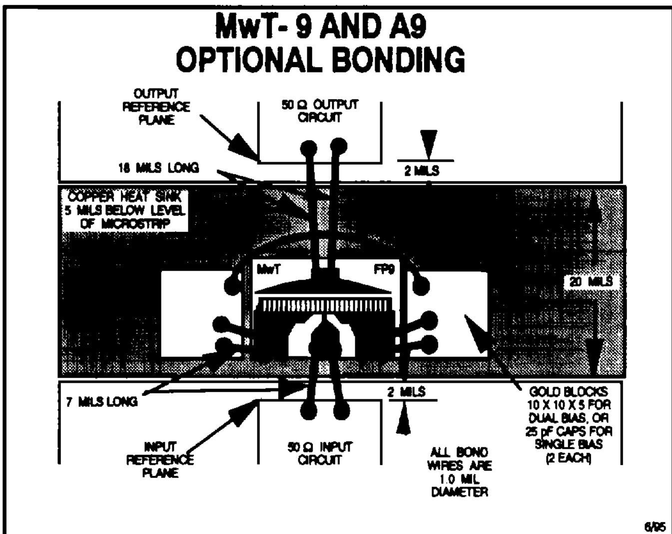
PARAMETER		VALUE
Gate Bond Wire Inductance	Lg	.15 nH
Gate Pad Capacitance	Cpg	.07 pF
Gate Resistance	Rg	.5 Ω
Gate-Source Capacitance	Cgs	.85 pF
Channel Resistance	Ri	1.0 Ω
Gate-Drain Capacitance	Cgd	.08 pF
Transconductance	gm	95 mS
Transit time	tau	2.6 psec

PARAMETER		VALUE
Source Resistance	Rs	0.20 Ω
Source Inductance	Ls	.055 nH
Drain-Source Resistance	Rds	300 Ω
Drain-Source Capacitance	Cds	.05 pF
Drain Resistance	Rd	1.02 Ω
Drain Pad Capacitance	Cpd	.05 pF
Drain Inductance	Ld	.23 nH

RECOMMENDED ASSEMBLY CONFIGURATION

Shown below is the assembly and bonding configuration used for S-Parameter measurements of the MwT-9 chip. This configuration is recommended for optimum performance. For single-bias applications the gold blocks may be replaced by capacitors. An additional interconnecting bond would then be required. Contact MwT for additional applications information.





BIN SELECTION

Every MwT-9 wafer has been probed for Idss and the data stored on computer disk. Customers may select from Idss values in any of 18 current bins, as shown below, to insure consistent performance in their circuit. The shaded bins are typically available in smaller quantity and caution is advised before designing these bins into high production applications. MwT's "Smart Wafer Picker" reads the stored Idss Data from the disk and devices from customer selected bins are quickly and automatically picked from the wafer and loaded into shipping containers.

BIN#	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
IDSS (mA)	78-90	90-102	102-114	114-126	126-138	138-150	150-162	162-174	174-186	186-198	198-210	210-222	222-234	234-246	246-258	258-270	270-282	282-294

BIN ACCURACY

Due to the effects of temperature, dc loading and probe tip varnishing, the IDSS from the "on wafer" probing of any MwT device may differ after it has been attached to a proper heat sink and tested in an RF or DC circuit.

Because of the aforementioned effects, the IDSS distribution may deviate as much as +/- 1 bin within the range identified on the label of each die shipping container, and +/- 2 bins within the selected range.

TYPICAL COMMON SOURCE SCATTERING PARAMETERS

MwT-9 CHIP: VDS = 6.0 V, IDS = 0.6 IDSS =120 mA

FREQUENCY (GHz)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
1.00	.95	-45.5	7.38	150.4	.03	66.7	.53	-17.4
2.00	.88	-79.9	6.01	128.4	.05	50.8	.47	-30.0
3.00	.86	-107.0	4.96	110.3	.06	40.3	.42	-39.6
4.00	.82	-126.3	4.01	96.9	.06	32.9	.38	-47.2
5.00	.81	-140.8	3.41	86.3	.06	30.8	.36	-53.5
6.00	.80	-152.2	2.94	76.8	.06	29.2	.35	-58.3
7.00	.80	-162.0	2.57	67.8	.06	28.2	.35	-64.9
8.00	.80	-169.9	2.28	60.2	.06	27.5	.34	-72.2
9.00	.81	-176.4	2.05	53.0	.06	27.2	.33	-80.7
10.00	.82	177.5	1.86	46.0	.06	27.8	.33	-90.2
12.00	.84	167.4	1.57	32.8	.06	38.8	.36	-108.8
14.00	.83	159.0	1.32	20.4	.07	45.6	.43	-120.9
16.00	.86	154.1	1.14	10.2	.08	45.2	.48	-129.7
18.00	.90	148.6	1.00	0.5	.08	49.3	.50	-137.0
20.00	.89	142.5	.88	-9.3	.10	55.3	.55	-147.0
22.00	.90	138.5	.80	-18.6	.12	47.9	.64	-159.8
24.00	.89	133.3	.72	-30.3	.13	42.3	.69	-169.1
26.00	.91	128.5	.64	-39.3	.14	36.6	.71	178.9

MwT-970: VDS = 6.0 V, IDS = 0.6 IDSS = 120 mA

FREQUENCY (GHz)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
1.00	.917	-59.612	5.997	135.785	.029	55.286	.610	-26.668
2.00	.822	-96.672	4.332	107.952	.041	40.139	.592	-40.676
3.00	.762	-120.650	3.366	89.518	.046	34.784	.589	-46.575
4.00	.713	-143.567	2.870	74.399	.045	27.349	.555	-50.289
5.00	.691	-166.699	2.640	60.172	.047	41.167	.507	-52.476
6.00	.746	169.631	2.490	42.833	.060	42.864	.446	-67.100
8.00	.815	133.435	1.968	8.164	.054	37.249	.352	-119.483
10.00	.797	122.609	1.378	-19.500	.079	25.024	.546	-153.160
12.00	.761	103.242	1.257	-42.305	.082	11.895	.631	-162.741
14.00	.631	58.192	1.293	-78.395	.157	-9.475	.657	-179.048
16.00	.534	-10.668	1.096	-120.137	.241	-44.921	.646	149.661
18.00	.524	-71.177	.880	-146.257	.317	-59.621	.631	128.319

MwT-971: VDS = 6.0 V, IDS = 0.6 IDSS = 120 mA

FREQUENCY (GHz)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
1.00	.933	-56.110	6.177	138.633	.027	57.843	.589	-31.268
2.00	.854	-87.839	4.463	113.413	.039	39.700	.580	-49.202
3.00	.790	-105.659	3.473	97.531	.044	35.542	.591	-57.611
4.00	.730	-123.098	2.981	83.850	.045	27.578	.582	-63.044
5.00	.689	-142.549	2.745	71.501	.038	34.447	.564	-65.201
6.00	.743	-166.627	2.585	54.618	.056	23.245	.543	-76.751
8.00	.791	158.158	2.068	23.103	.062	-5.699	.435	-106.259
10.00	.752	144.719	1.549	-10.721	.052	-57.087	.594	-139.353
12.00	.819	119.468	1.318	-30.241	.019	-23.297	.628	-157.466
14.00	.752	84.512	1.387	-61.787	.074	-35.804	.610	-164.786
16.00	.372	40.556	1.215	-106.741	.151	-61.791	.604	177.407
18.00	.311	-40.751	1.105	-140.525	.289	-87.861	.550	158.421

MwT-973: VDS = 6.0 V, IDS = 0.6 IDSS =120 mA

FREQUENCY (GHz)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
1.00	.92	-50.6	6.40	142.0	.03	68.6	.52	-24.0
2.00	.80	-88.4	4.96	114.5	.05	48.2	.47	-41.0
3.00	.72	-116.4	4.08	94.1	.06	41.1	.43	-52.0
4.00	.66	-143.4	3.47	76.2	.07	34.4	.40	-60.7
5.00	.63	-168.1	3.06	61.0	.07	33.6	.38	-66.0
6.00	.66	168.0	2.81	45.2	.08	32.0	.37	-77.1
8.00	.77	124.5	2.32	11.7	.10	14.9	.25	-111.8
10.00	.86	93.0	1.83	-23.3	.10	-5.9	.28	-169.4
12.00	.97	69.1	1.40	-50.3	.10	-3.8	.41	157.6
14.00	.94	55.4	1.21	-74.9	.14	-14.6	.50	134.4
16.00	.77	34.2	.97	-106.1	.16	-40.7	.53	104.5
18.00	.70	6.9	.72	-119.5	.21	-36.7	.57	84.2

DEVICE HANDLING PROCEDURE

1) Open package in clean room environment only.
2) GaAs FETs are sensitive to electrostatic discharge. Precautions should be taken in handling, die attachment, and bonding to assure that Maximum Ratings are not exceeded as a result of electrical discharge.
3) Chips have been cleaned and are ready for die attachment. DO NOT attempt to re-clean.
4) Assembly should be performed with parts no hotter than 300° C. All circuit components (such as resistors and capacitors) should be assembled completely before the FET is die attached. Assembly should be performed as quickly as possible. In general, no chip should be left at 300°C for over 2 minutes.
5) Die attach with clean AuSn alloy under forming gas at 280 to 300° C. Scrub chip down with tweezers. Thermal resistance is critically dependent on this operation.
6) Thermasonic wedge bonding is recommended. A .0015 in. bond flat wedge at 125 to 150° C should be used with a heater stage temperature of 200 to 225° C. Apply 15 to 20 grams of bond force to .001 in. diameter gold wire with an elongation of 2 to 5%.
7) Store in a clean, dry, inert environment such as nitrogen at room temperature.
8) CAUTION: Handling of chips other than as specified above may cause permanent damage.