HA13539FP/549FP

Voice Coil Motor Driver IC

Description

The HA13539FP and the HA13549FP are IC that was developed for use as a voice coil motor driver in 12 V HDD applications. It provides the following functions and features.

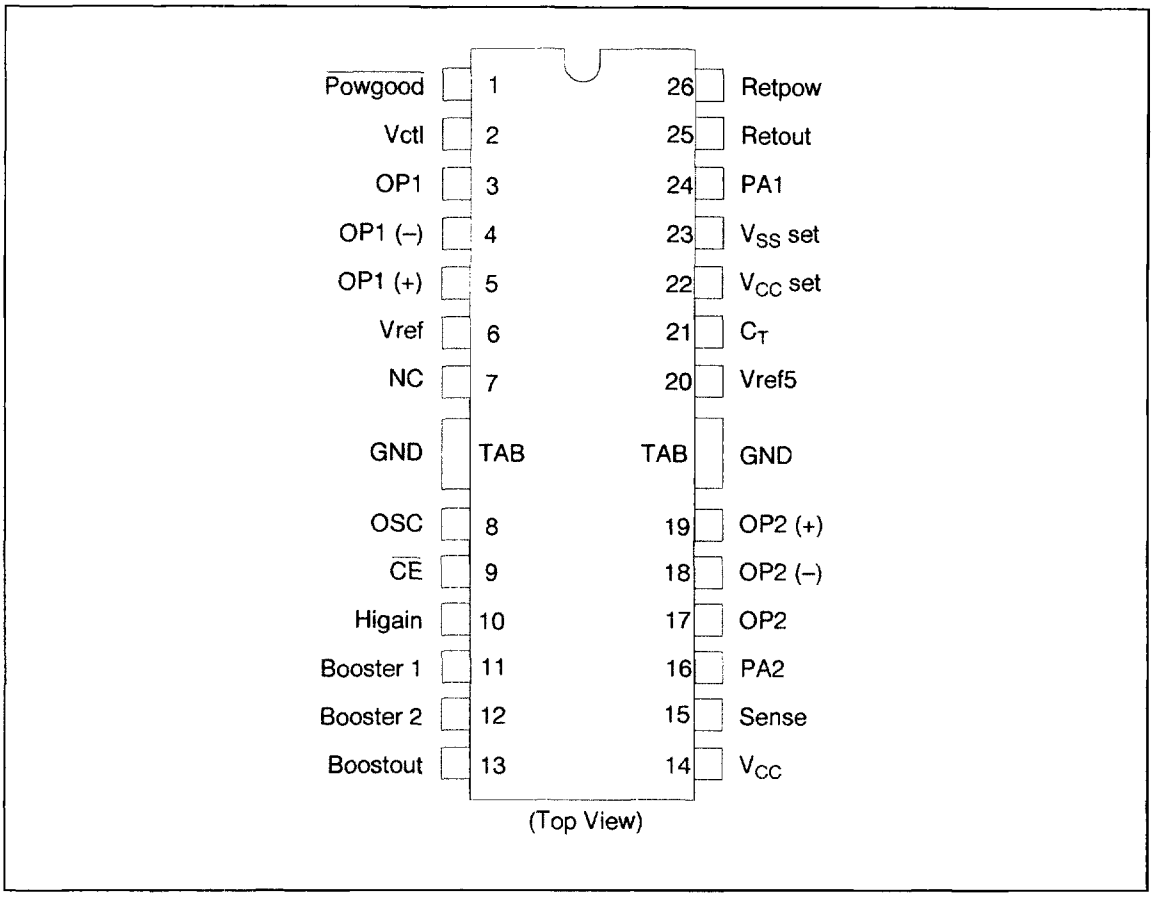
Features

- Low saturation voltage
- Low crossover distortion
- Less external components

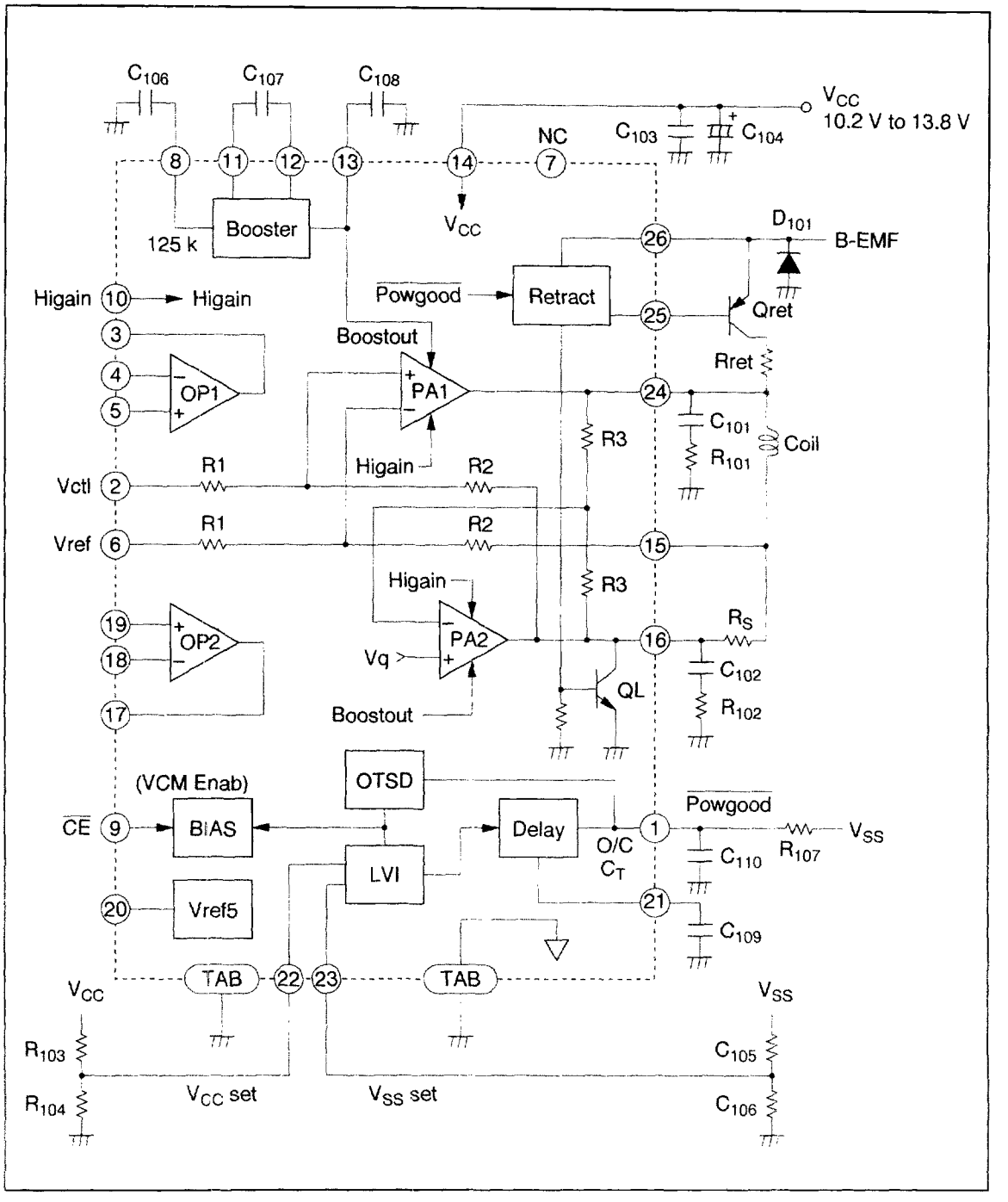
Functions

- 1.5 A BTL output amplifier (Dual gain)
- Auto-retraction circuit
- Two independent operational amplifiers
- 5 V reference voltage
- Thermal protection circuit OTSD
- Two under-voltage protection circuits LVI

Pin Arrangement



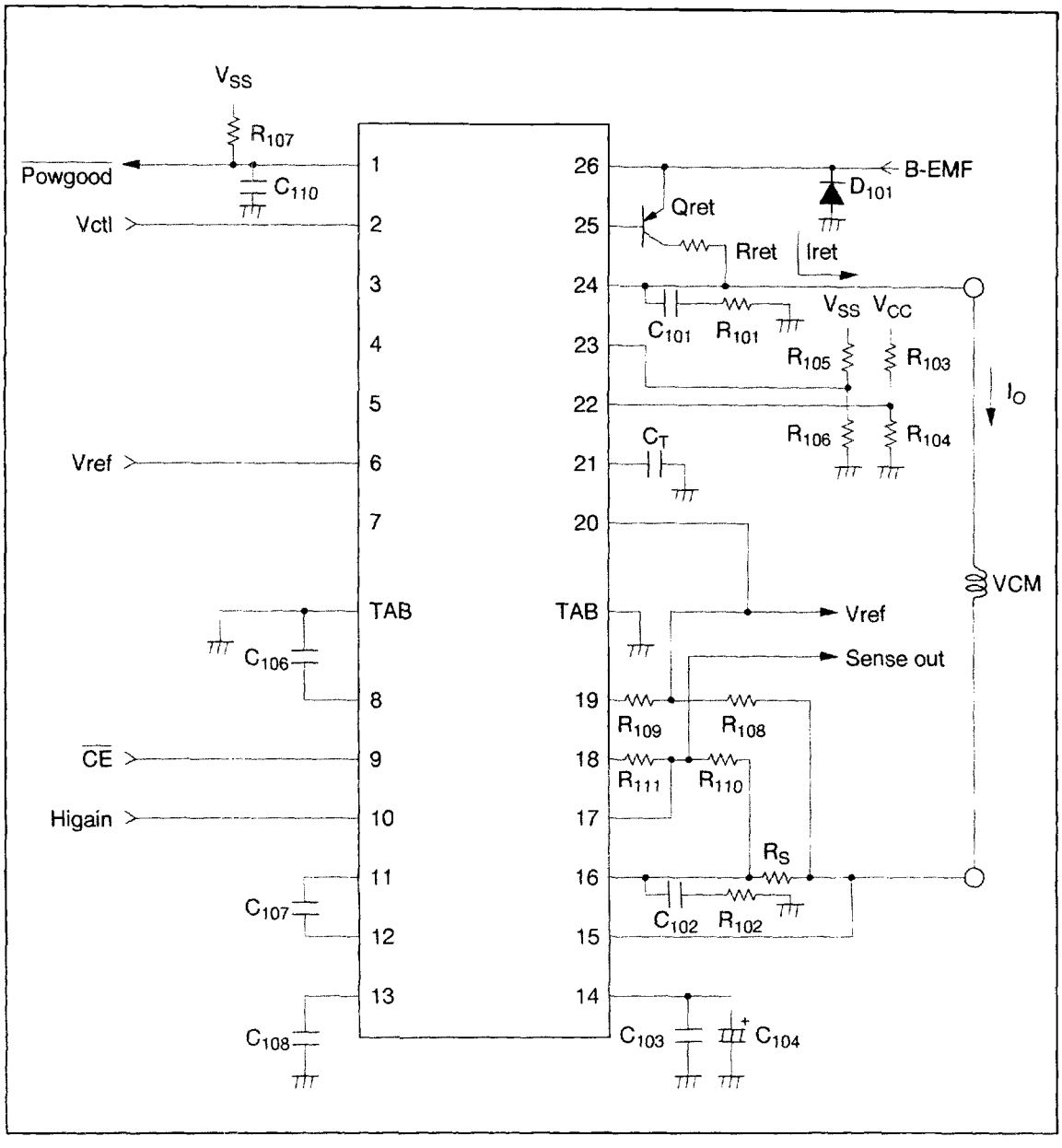
Block Diagram



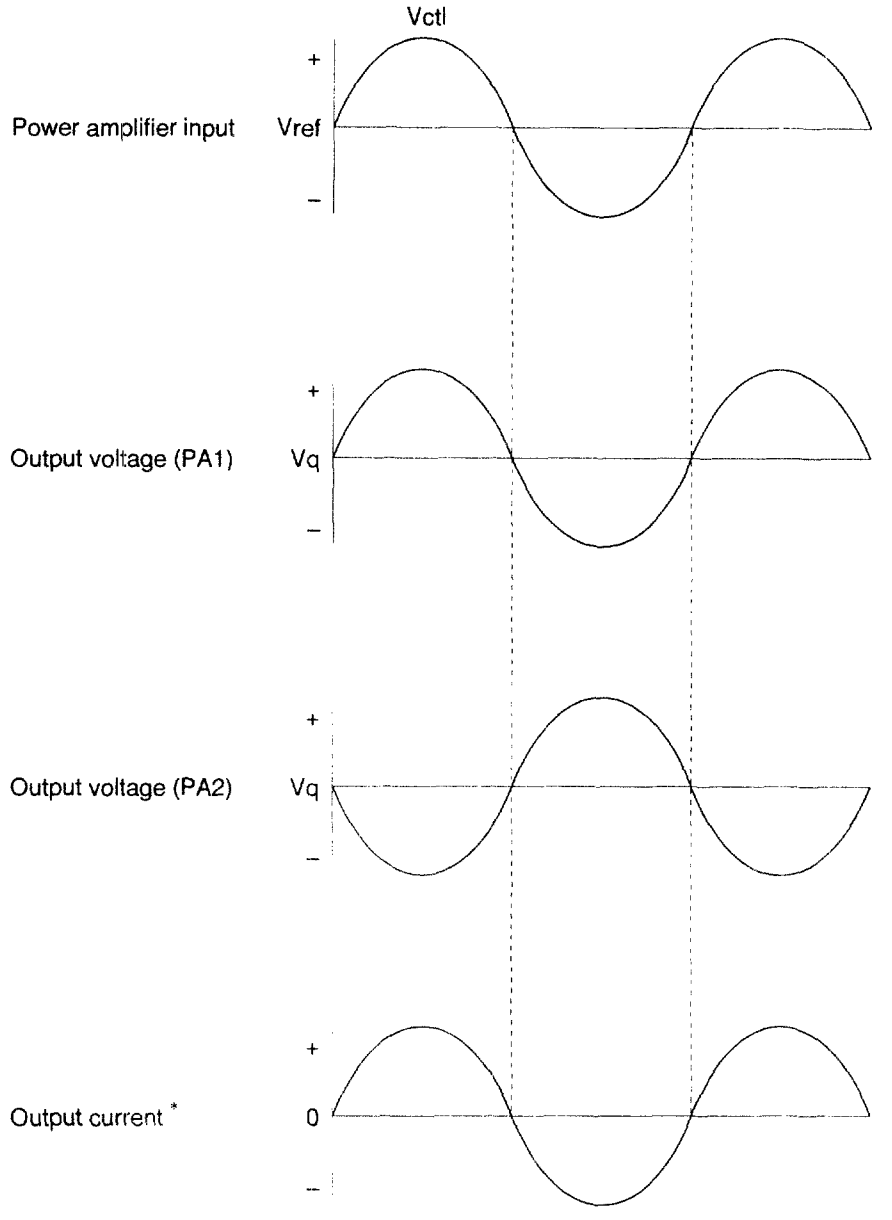
Pin Assignment

Pin No.	Symbol	Function
1	$\overline{\text{Powgood}}$	Abnormal state monitor. Low: Normal state, High impedance: Abnormal state. Open collector output
2	V_{ctl}	Power amplifier (+) input. PA1 output reference.
3	OP1	Operational amplifier that operates when Vcc > 10 V independent of the $\overline{\text{CE}}$ pin. Can be used for input filter.
4	OP1 (–)	OP1 (–) input Must be shorted to ground when unused.
5	OP1 (+)	OP1 (+) input
6	V_{ref}	Power amplifier (–) input. PA1 output reference.
8	OSC	Used with the booster (charge pump) and as an oscillator frequency adjustment.
9	$\overline{\text{CE}}$	Chip enable. Low: Enable, High: Disable
10	Higain	Power amplifier gain switch. Low: Low gain, High: High gain
11	Booster 1	Booster (charge pump) pulse input
12	Booster 2	Booster (charge pump) pulse output
13	Boostout	Booster output. Power amplifier pre-driver power supply
14	V_{CC}	Power supply
15	Sense	Power amplifier current sense
16	PA2	PA2 output
17	OP2	Operational amplifier that operates when Vcc > 10 V independent of the $\overline{\text{CE}}$ pin. Can be used as a sensor amplifier.
18	OP2 (–)	OP2 (–) input Must be shorted to ground when unused.
19	OP2 (+)	OP2 (+) input
20	Vref5	5 V Reference voltage. Use power amplifier reference voltage.
21	C_T	$\overline{\text{Powgood}}$ falling edge delay time setting
22	V_{CC}set	V_{CC} side LVI operating voltage (V_{sd1}) setting. Must be shorted to V_{CC} if unused.
23	V_{SS}set	V_{SS} side LVI operating voltage (V_{sd2}) setting. Must be shorted to V_{CC} or V_{SS} if unused.
24	PA1	PA1 output
25	Retout	Retractor external PNP base current supply
26	Retpow	Retractor power supply. Can be used the spindle motor output.

Application



Timing Chart



Notes: These waveforms are for input frequencies less than 1 kHz.
* Current flowing from PA1 to PA2 is indicated as positive (+), and current flowing from PA2 to PA1 is indicated as negative (–).

Truth Table 1

Inputs				Outputs			
V_{CC}	V_{SS}	$\overline{CE}$*2	Higain*2	PA1	PA2	Retout	$\overline{Powgood}$
$\leq V_{sd1}$*1	$\leq V_{sd2}$*1	X	X	Disable	$V_{sat}L$*3	I_{ret}*3	I_{ret}*3
$\leq V_{sd1}$	$>V_{sd2}$						
$>V_{sd1}$	$\leq V_{sd2}$						
$>V_{sd1}$	$>V_{sd2}$	H	X	Disable	Disable	Z	L
		L	H	High gain*1	High gain*1	Z	L
			L	Low gain*1	Low gain*1	Z	L
$>V_{sd1}$	$>V_{sd2}$	X	($T_j > T_{sd}$)	Disable	$V_{sat}L$*3	I_{ret}*3	Z

Truth Table 2

Inputs	Outputs	
V_{CC}	OP1,OP2	Vref5
<7V	Disable	Disable
8 V to 12 V	Enable	Enable

Notes: 1. See the external components table.
2. Z = High impedance
H = High voltage level
L = Low voltage level
X = Irrelevant
3. See the electrical characteristics table.

External Components

Part No.	Recommended Value	Purpose	Note
R_{101}, R_{102}	2.2 Ω	Power amplifier output stabilization	
R_{103}, R_{104}	—	LVI voltage setting (V_{CC})	1
R_{105}, R_{106}	—	LVI voltage setting (V_{SS})	2
R_{107}	—	$\overline{\text{Powgood}}$ pull-up	
R_{108} to R_{111}	—	Output sense amplifier gain setting	
R_S	1.0 Ω	Power amplifier output current detection	3
Rret	—	Retractor current limiter	4
Qret	—	Retractor	4
C_{101}, C_{102}	0.1 µF	Power amplifier output stabilization	
C_{103}, C_{104}	0.1 µF, 4.7 µF	Power supply stabilization	
C_{106}	820 pF	Booster (oscillation)	
C_{107}, C_{108}	0.1 µF, 2.2 µF	Booster	
C_{109}	0.01 µF	$\overline{\text{Powgood}}$ delay setting	5
C_{110}	0.0022 µF	$\overline{\text{Powgood}}$ filter	
D_{101}	$V_F < 0.75$ V (I_F = 0.5 A)	B-EMF clamp	

Notes: 1. The LVI1 (V_{CC}) operating voltage (V_{sd1}) and hysteresis (V_{hys1}) are determined by the following formulas.

$$Vsd1 = \left(1 + \frac{R_{103}}{R_{104}}\right) \cdot Vref1\ (V)$$ (Set Vsd1 to be 9.0 V or higher.)

$$Vhys1 = \left(1 + \frac{R_{103}}{R_{104}}\right) \cdot Vhys1\ (V)$$ Vref1, Vhys1 : See the electrical characteristics table.

2. The LVI2 (V_{SS}) operating voltage (V_{sd2}) and hysteresis (V_{hys2}) are determined by the following formulas.

$$Vsd2 = \left(1 + \frac{R_{105}}{R_{106}}\right) \cdot Vref2\ (V)$$ (Set Vsd2 to be 3.0 V or higher.)

$$Vhys2 = \left(1 + \frac{R_{105}}{R_{106}}\right) \cdot Vhys2\ (V)$$ Vref2, Vhys2 : See the electrical characteristics table.

3. The relationship between the PA output current (I_O) and input voltage (V_{ctl}) is determined by the following formula.

$$I_O = \frac{(Vctl - Vref)\ Gctl}{R_S} = \frac{(Vctl - Vref) \cdot gm \cdot R'_S}{R_S}$$

Where: G_{ctl}: $g_m \cdot R_S'$ (See the electrical characteristics table.)
V_{ref}: PA1 reference voltage

4. The retract current (I_{ret}) is determined by the following formula.

$$Iret = \frac{Vretpow - Vretsat - VsatL}{R_L + R_S + Rret}$$

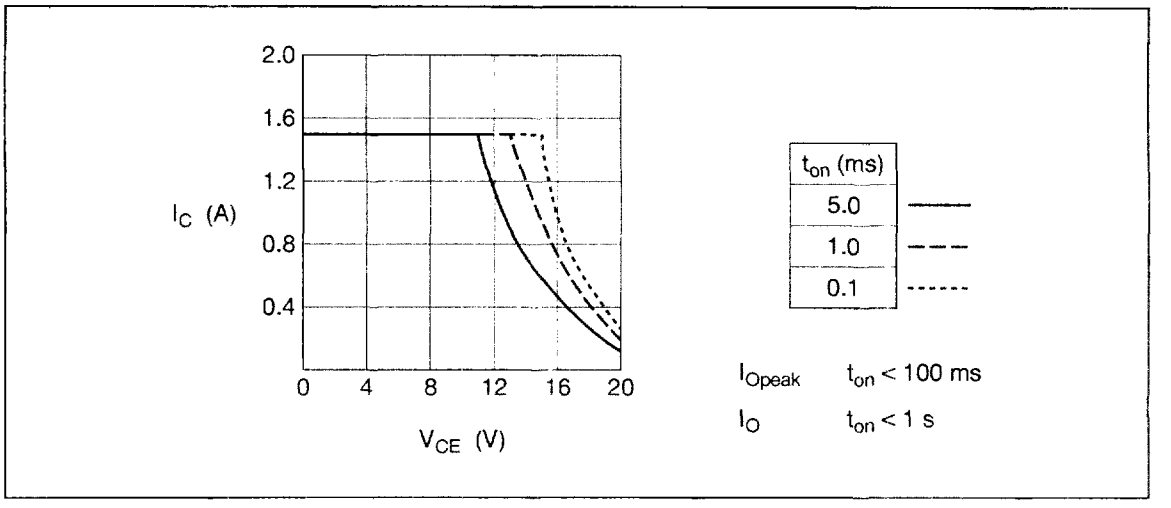
Where: V_{retpow}: Retpow voltage
V_{retsat}: Qret saturation voltage
R_L: Load resistance
V_{satL}: PA2 lower side saturation voltage (See the electrical characteristics table.)

5. The $\overline{\text{Powgood}}$ delay time (T_{por}) is determined by the following formulas.
$T_{porhl} = C_T \cdot V_{th}/I_{cha}$
$T_{porlh} \leq C_T\ (V_{CC} - V_{th})/I_{dis}$

Absolute Maximum Ratings

Item	Symbol	HA13539FP	HA13549FP	Unit	Note
Power supply voltage	V_{CC}	15	15	V	1
Peak output current	I_{opeak}	1.5	1.5	A	2
Steady-state output current	I_O	1.0	1.0	A	2
Retract current	I_{ret}	0.2	0.2	A	3
Input voltage	V_{in}	V_{CC}	V_{CC}	V	
Allowable power dissipation	P_T	6.0 (T_C = 100°C)	6.0 (T_C = 100°C)	W	4
Junction temperature	T_j	+150	+150	°C	5
Storage temperature	T_{stg}	–55 to +125	–55 to +125	°C	

Notes: 1. The operating voltage range is as follows:
V_{CC} = 10.2 V to 13.8 V
2. ASO of each output transistor is shown below. Operating locus must be within the ASO.



3. Applies to the PA2 lower side transistor. (Q_{ret})
4. Permitted value at T_C = 100°C. Thermal resistance is shown below.
$\theta_{j\text{-}c} \leq 8$ °C/W
$\theta_{j\text{-}a} \leq 35$ °C/W (when a 6-layer printed circuit board is used)
$\theta_{j\text{-}a} \leq 62$ °C/W (when a glass epoxy printed circuit board is used with a wiring density of 20%)
5. The junction operating temperature range is as follows.
T_{jopr} = 0 °C to 125 °C

Electrical Characteristics (T_a = 25°C, V_{CC} = 12 V, V_{SS} = 5 V)

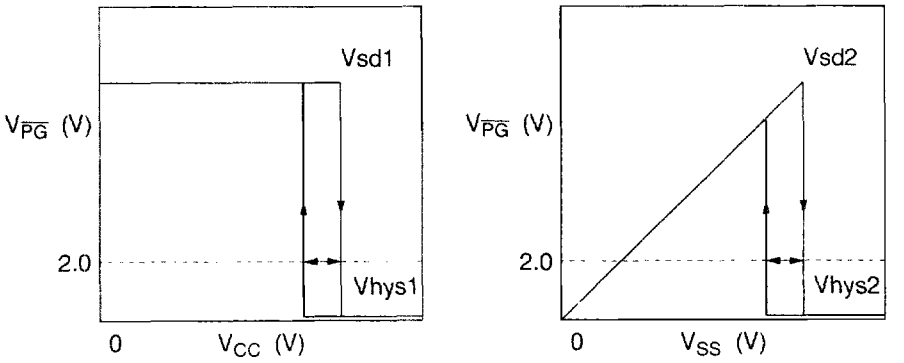
Item		Symbol	Min	Typ	Max	Unit	Test Condition	Applicable Pins	Note
Quiescent current		I_{CC0}	—	3.5	5.0	mA	$\overline{CE}$ = H	14	
		I_{CC1}	—	15	20	mA	$\overline{CE}$ = L, V_{SS} = 5V		
		I_{retpow}	—	50	70	mA	$\overline{CE}$ = L, V_{SS} = 0V V_{retpow} = 5 V	26	
$\overline{CE}$, Higain	Input current	I_{in1}	—	—	±10	µA		9, 10	
	Input high voltage	V_{ih1}	2.0	—	—	V			
	Input low voltage	V_{il1}	—	—	0.8	V			
PA1, PA2	Input resistance	R_{in} (H)	15 (22.5	20 30	25 37.5)	kΩ	Higain = H	2, 6	
		R_{in} (L)	30	40	50	kΩ	Higain = L		
	Common mode input voltage range	V_{cm} (H)	0	—	V_{CC} − 2.0	V	Higain = H		
		V_{cm} (L)	0	—	V_{CC} − 2.0	V	Higain = L		
	Output quiescent-voltage	V_q	5.6	6.0	6.4	V	R_L = 10 Ω, R_S = 1.0 Ω	16, 24	
	Output offset voltage (PA2-sense)	V_{ofs} (H)	—	—	±5	mV	Higain = H, R_S = 1.0 Ω ,R_L = 10 Ω V_{ctl} = V_{ref} = 6.0 V		
		V_{ofs} (L)	—	—	±3	mV	Higain = L, R_S = 1.0 Ω ,R_L = 10 Ω V_{ctl} = V_{ref} = 6.0 V		
	Output saturation voltage	V_{sat1}	—	0.8	1.1	V	I_O = 0.8 A		1
		V_{sat2}	—	0.4	0.55	V	I_O = 0.4 A		
	Output leak current	I_{CER}	—	—	±100	µA	V_{CE} = 15 V		2
	Transfer gain	g_m (H)	1.75 (0.86	1.87 0.93	1.99 1.00)	A/V	Higain = H, R'_S = 1.0 Ω	2, 6, 16, 24	3
		g_m (L)	0.42	0.46	0.50	A/V	Higain = L, R'_S = 1.0 Ω		
	Gain bandwidth (resistive load)	B (H)	—	45 (70)	—	kHz	Higain = H R_L = 10 Ω, R_S = 1.0 Ω		4
		B (L)	—	90	—	kHz	Higain = L R_L = 10 Ω, R_S = 1.0 Ω		
Retract	Retpow voltage	V_{retpow}	0.8	—	—	V	I_{retout} = 0.1 mA	26	
	Retout output current	I_{retout}	5.0	9.0	—	mA	V_{retpow} = 3 V	25	
	QL saturation voltage	V_{satL}	—	0.1	0.25	V	I_{ret} = 0.1 A V_{retpow} = 3 V	16	
OP1, OP2	Input current	I_{inop}	—	—	±500	nA		4, 5	
	Input offset voltage	V_{osop}	—	—	±7	mV		18, 19	

Electrical Characteristics (T_a = 25°C, V_{CC} = 12 V, V_{SS} = 5 V) (cont.)

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Applicable Pins	Note
OP1, OP2	Common mode input voltage range	V_{cmop}	0	—	V_{CC} −1.8	V		4, 5, 18, 19	
	Output high voltage	V_{ohop}	V_{CC} −1.3	—	—	V	I_{out} = 1.0 mA	3, 17	
	Output low voltage	V_{olop}	—	—	1.1	V	I_{out} = 1.0 mA		
	Open loop gain	G_{op}	—	41	—	dB	f = 10 kHz		4
	Gain bandwidth	B_{op}	—	1.5	—	MHz	G_{op} = 0 dB		
$\overline{\text{Powgood}}$	Output leak current	I_{leak}	—	—	±10	μA	V_{oh} = 15 V	1	
	Output low voltage	V_{ol}	—	0.1	0.4	V	I_{ol} = 1 mA		
Vref5	Output voltage	V_{ref5}	4.75	4.9	5.05	V	I_O = 20 mA	20	
	Output resistance	R_{out}	—	—	5	Ω	I_O = 20 mA		
LVI	Reference voltage	V_{ref1}	1.32	1.36	1.40	V	R_{103} = 62 kΩ	22, 23	
		V_{ref2}	1.28	1.32	1.36		R_{104} = 10 kΩ		
	Hysteresis	V_{hys1}	40	80	100	mV	R_{105} = 18 kΩ		
		V_{hys2}	60	105	130		R_{106} = 10 kΩ		
Delay	Threshold voltage	V_{th}	—	2.5	—	V		21	
	Ct charge current	I_{cha}	—	10	—	μA			
	Ct discharge current	I_{dis}	1.0	1.8	—	mA			
OTSD	Operating temperature	T_{sd}	125	150	—	°C			4
	Hysteresis	T_{hys}	—	25	—	°C			

Notes: 1 The output saturation voltage is the sum of the upper and lower saturation voltages.
2. The value is output transistor only, not include Feed back resistance etc.
3. The value in parentheses apply to the HA13549FP.
4. These are design center values and are not (and cannot be) tested in the mass production products.

The LVI circuit has the hysteresis, and it is shown below.



Main Characteristics

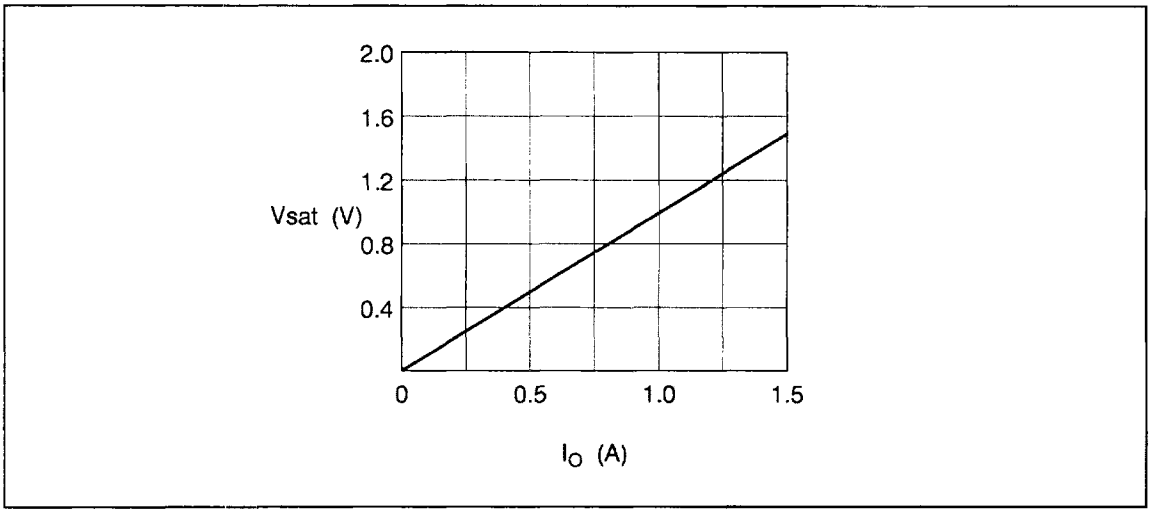


Figure 1. Output Saturation Voltage vs. Output Current

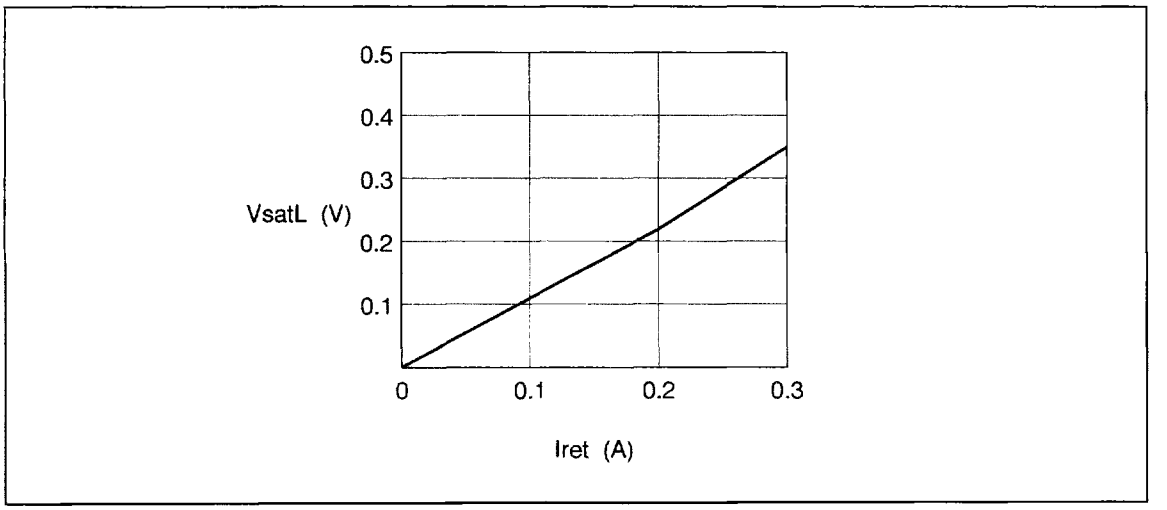


Figure 2. Lower Side Saturation Voltage vs. Retractor Current

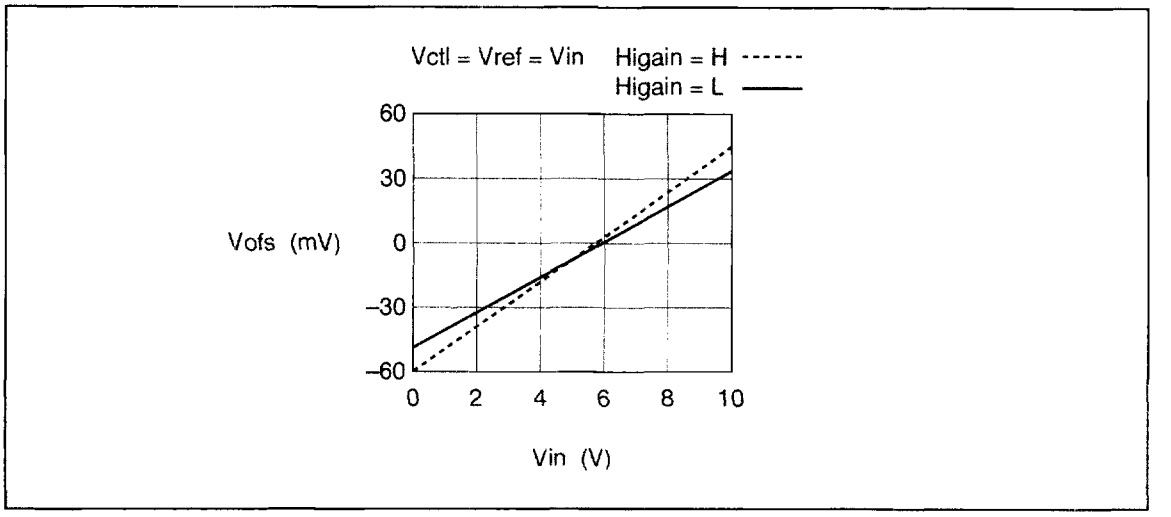


Figure 3. Input Voltage vs. Output Offset Voltage

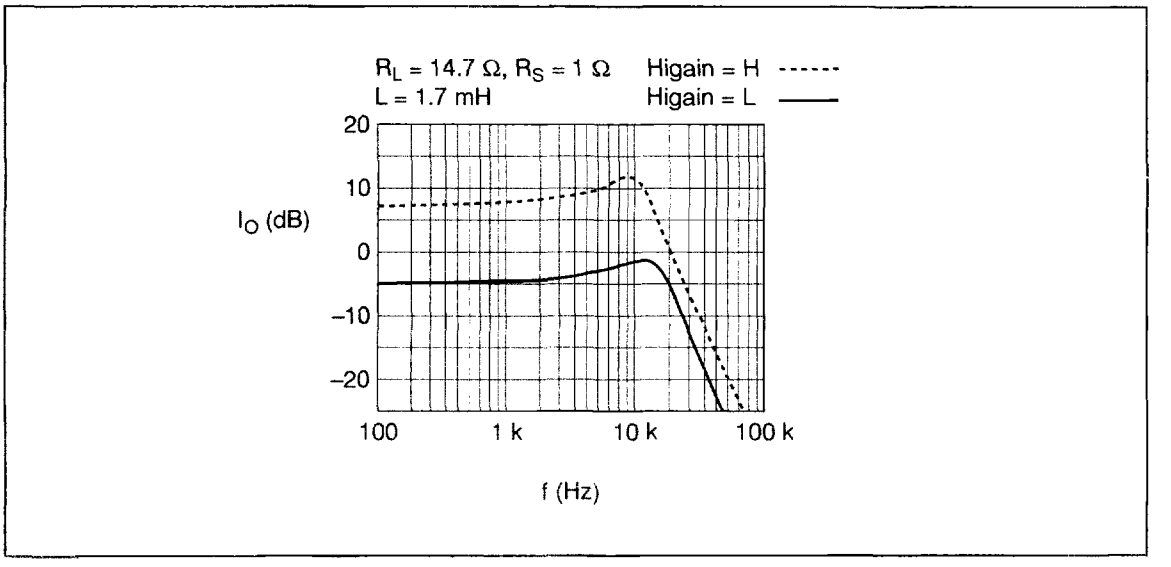


Figure 4. Output Current Frequency Characteristics