

HD74AC283/HD74ACT283

4-bit Binary Full Adder with Fast Carry

HITACHI

ADE-205-388 (Z)
1st. Edition
Sep. 2000

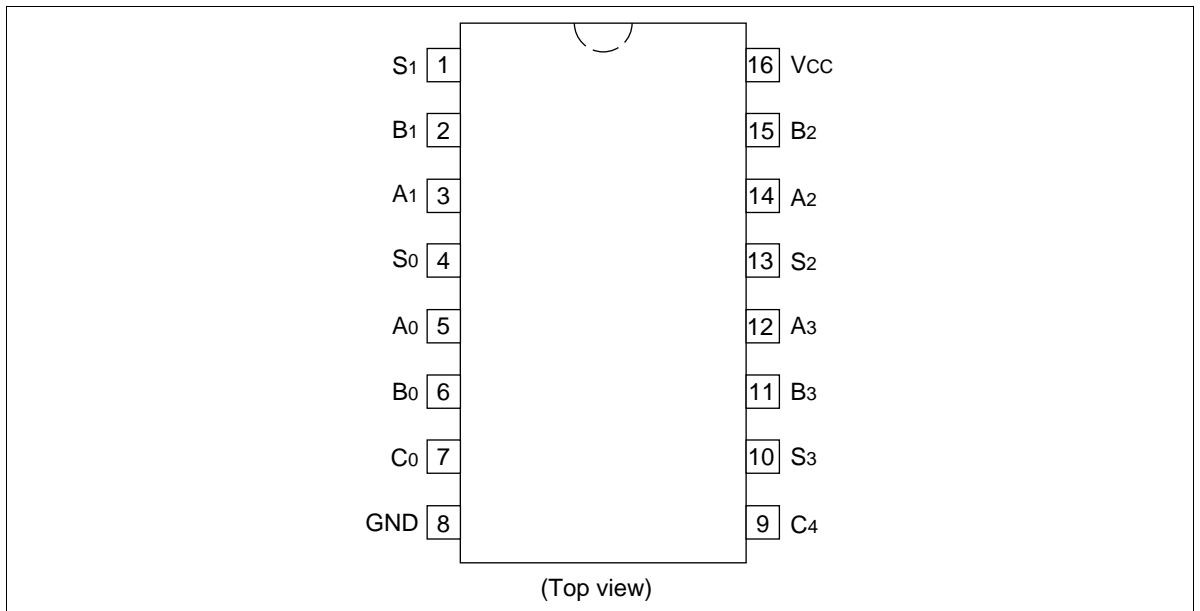
Description

The HD74AC283/HD74ACT283 high-speed 4-bit binary full adder with internal carry lookahead accepts two 4-bit binary works ($A_0 - A_3$, $B_0 - B_3$) and a Carry input (C_0). It generates the binary Sum outputs ($S_0 - S_3$) and the Carry output (C_4) from the most significant bit. The HD74AC283/HD74ACT283 will operate with either active High or active Low operands (positive or negative logic).

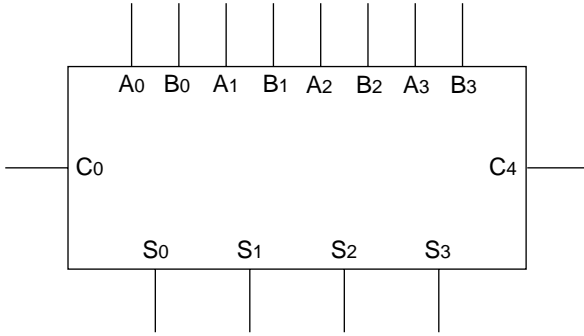
Features

- Outputs Source/Sink 24 mA
- HD74ACT283 has TTL-Cmpatible Inputs

Pin Arrangement



Logic Symbol



Pin Names

- $A_0 - A_3$ A Operand Inputs
- $B_0 - B_3$ B Operand Inputs
- C_0 Carry Input
- $S_0 - S_3$ Sum Outputs
- C_4 Carry Output

Functional Description

The HD74AC283/HD74ACT283 adds two 4-bit binary words (A plus B) plus the incoming Carry (C_0). The binary sum appears on the Sum ($S_0 - S_3$) and outgoing carry (C_4) outputs. The binary weight of the various inputs and outputs is indicated by the subscript numbers, representing powers of two.

$$2^0 (A_0 + B_0 + C_0) + 2^1 (A_1 + B_1) + 2^2 (A_2 + B_2) + 2^3 (A_3 + B_3) = S_0 + 2S_1 + 4S_2 + 8S_3 + 16C_4$$

Where (+) = plus

Interchanging inputs of equal weight does not affect the operation. Thus C_0 , A_0 , B_0 can be arbitrarily assigned to pins 5, 6 and 7 for DIPS. Due to the symmetry of the binary add function, the HD74AC283/HD74ACT283 can be used either with all inputs and outputs active High (positive logic) or with all inputs and outputs active Low (negative logic). See Figure a. Note that if C_0 is not used it must be tied Low for active High logic or tied High for active Low logic.

Due to pin limitations, the intermediate carries of the HD74AC283/HD74ACT283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. Figure b shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder (A_3 , B_3) Low makes S_3 dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle Figure c shows a way of dividing the HD74AC283/HD74ACT283 into a 2-bit and a 1-bit adder. The third stage adder (A_2 , B_2 , S_2) is used merely as a means of getting a carry (C_{10}) signal into the fourth stage (via A_2 and B_2) and bringing out the carry from the second stage on S_2 . Note that as long as A_2 and B_2 are the same, whether High or Low, they do not influence S_2 . Similarly, when A_2 and B_2 are the same the carry into the third stage does not influence the carry out of the third

stage. Figure d shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs S_0 , S_1 and S_2 present a binary number equal to the number of inputs $I_1 - I_5$ that are true. Figure e shows one method of implementing a 5-input majority gate. When three or more of the inputs $I_1 - I_5$ are true, the output M_5 is true.

Fig. a Active HIGH versus Active LOW Interpretation

| | C_0 | A_0 | A_1 | A_2 | A_3 | B_0 | B_1 | B_2 | B_3 | S_0 | S_1 | S_2 | S_3 | C_4 |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Logic levels | L | L | H | L | H | H | L | L | H | H | H | L | L | H |
| Active HIGH | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| Active LOW | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

Active HIGH: $0 + 10 + 9 = 3 + 16$

Active LOW: $1 + 5 + 6 = 12 + 0$

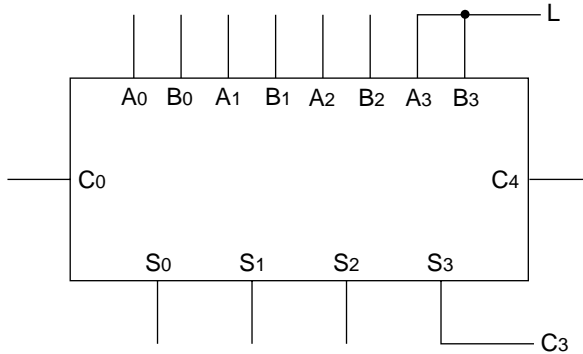


Fig. b 3-bit Adder

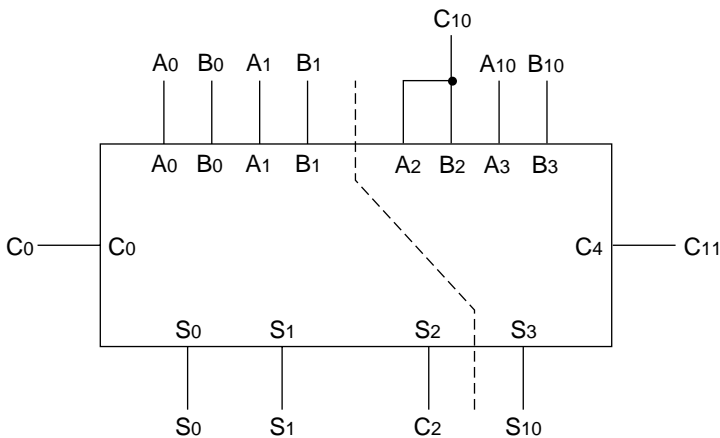


Fig. c 2-bit and 1-bit adders

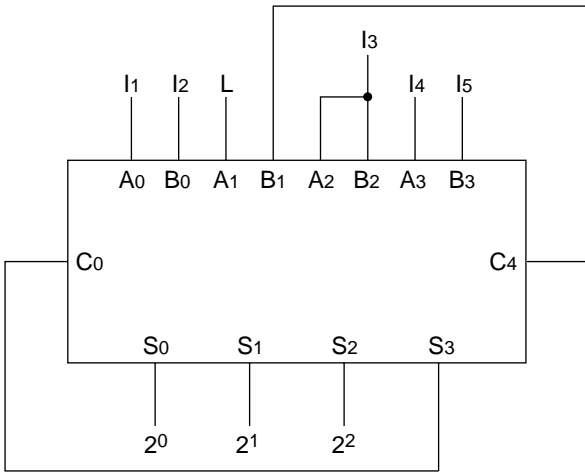


Fig. d 5-Input Encoder

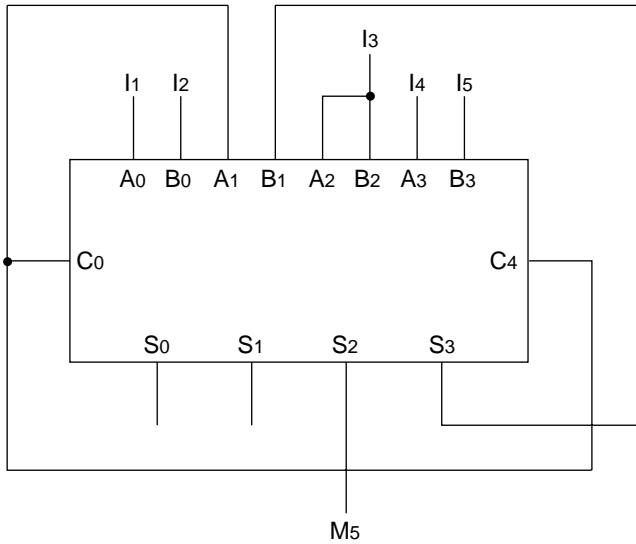
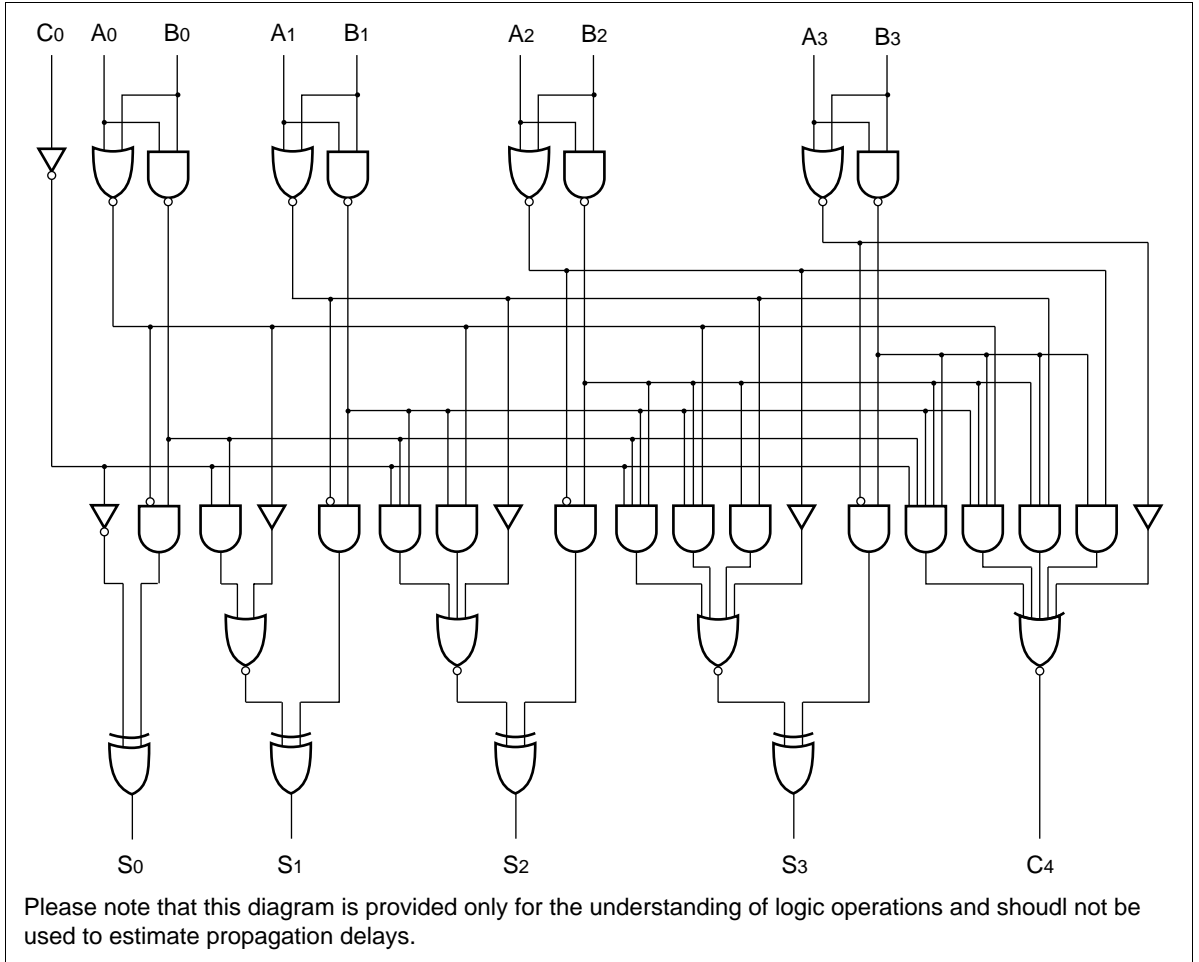


Fig. e 5-Input Majority Gate

Logic Diagram



DC Characteristics (unless otherwise specified)

| Item | Symbol | Max | Unit | Condition |
|--|-----------|-----|---------|--|
| Maximum quiescent supply current | I_{CC} | 80 | μA | $V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = \text{Worst case}$ |
| Maximum quiescent supply current | I_{CC} | 8.0 | μA | $V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = 25^\circ C$ |
| Maximum I_{CC}/input (HD74ACT283) | I_{CCT} | 1.5 | mA | $V_{IN} = V_{CC} - 2.1 V$, $V_{CC} = 5.5 V$, $T_a = \text{Worst case}$ |

HD74AC283/HD74ACT283

AC Characteristics: HD74AC283

| Item | Symbol | V _{CC} (V)* ¹ | Ta = +25°C C _L = 50 pF | | | Ta = -40°C to +85°C C _L = 50 pF | | Unit |
|--|------------------|-----------------------------------|--------------------------------------|------|------|---|------|------|
| | | | Min | Typ | Max | Min | Max | |
| Propagation delay | t _{PLH} | 3.3 | 1.0 | 11.5 | 15.0 | 1.0 | 16.5 | ns |
| C ₀ to S _n | | 5.0 | 1.0 | 9.5 | 11.5 | 1.0 | 12.5 | |
| Propagation delay | t _{PHL} | 3.3 | 1.0 | 10.5 | 14.0 | 1.0 | 15.5 | ns |
| C ₀ to S _n | | 5.0 | 1.0 | 8.5 | 10.5 | 1.0 | 11.5 | |
| Propagation delay | t _{PLH} | 3.3 | 1.0 | 14.0 | 17.0 | 1.0 | 18.5 | ns |
| A _n or B _n to S _n | | 5.0 | 1.0 | 11.5 | 13.5 | 1.0 | 14.5 | |
| Propagation delay | t _{PHL} | 3.3 | 1.0 | 13.5 | 16.5 | 1.0 | 18.0 | ns |
| A _n or B _n to S _n | | 5.0 | 1.0 | 11.0 | 13.0 | 1.0 | 14.0 | |
| Propagation delay | t _{PLH} | 3.3 | 1.0 | 9.5 | 12.5 | 1.0 | 15.5 | ns |
| C ₀ to C ₄ | | 5.0 | 1.0 | 7.5 | 9.5 | 1.0 | 10.5 | |
| Propagation delay | t _{PHL} | 3.3 | 1.0 | 10.0 | 13.0 | 1.0 | 14.0 | ns |
| C ₀ to C ₄ | | 5.0 | 1.0 | 8.0 | 10.0 | 1.0 | 11.0 | |
| Propagation delay | t _{PLH} | 3.3 | 1.0 | 11.5 | 14.5 | 1.0 | 16.0 | ns |
| A _n or B _n to C ₄ | | 5.0 | 1.0 | 9.5 | 11.5 | 1.0 | 12.5 | |
| Propagation delay | t _{PHL} | 3.3 | 1.0 | 12.0 | 15.0 | 1.0 | 16.5 | ns |
| A _n or B _n to C ₄ | | 5.0 | 1.0 | 10.0 | 12.0 | 1.0 | 13.0 | |

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics: HD74ACT283

| Item | Symbol | V _{CC} (V)* ¹ | Ta = +25°C C _L = 50 pF | | | Ta = -40°C to +85°C C _L = 50 pF | | Unit |
|---|------------------|-----------------------------------|--------------------------------------|------|------|---|------|------|
| | | | Min | Typ | Max | Min | Max | |
| Propagation delay C ₀ to S _n | t _{PLH} | 5.0 | 1.0 | 11.5 | 13.5 | 1.0 | 14.5 | ns |
| Propagation delay C ₀ to S _n | t _{PHL} | 5.0 | 1.0 | 10.0 | 12.0 | 1.0 | 13.0 | ns |
| Propagation delay A _n or B _n to S _n | t _{PLH} | 5.0 | 1.0 | 13.0 | 15.0 | 1.0 | 16.5 | ns |
| Propagation delay A _n or B _n to S _n | t _{PHL} | 5.0 | 1.0 | 12.0 | 14.0 | 1.0 | 15.5 | ns |
| Propagation delay C ₀ to C ₄ | t _{PLH} | 5.0 | 1.0 | 9.0 | 11.0 | 1.0 | 12.0 | ns |
| Propagation delay C ₀ to C ₄ | t _{PHL} | 5.0 | 1.0 | 10.0 | 12.0 | 1.0 | 13.0 | ns |
| Propagation delay A _n or B _n to C ₄ | t _{PLH} | 5.0 | 1.0 | 11.0 | 13.0 | 1.0 | 14.0 | ns |
| Propagation delay A _n or B _n to C ₄ | t _{PHL} | 5.0 | 1.0 | 11.5 | 13.5 | 1.0 | 14.5 | ns |

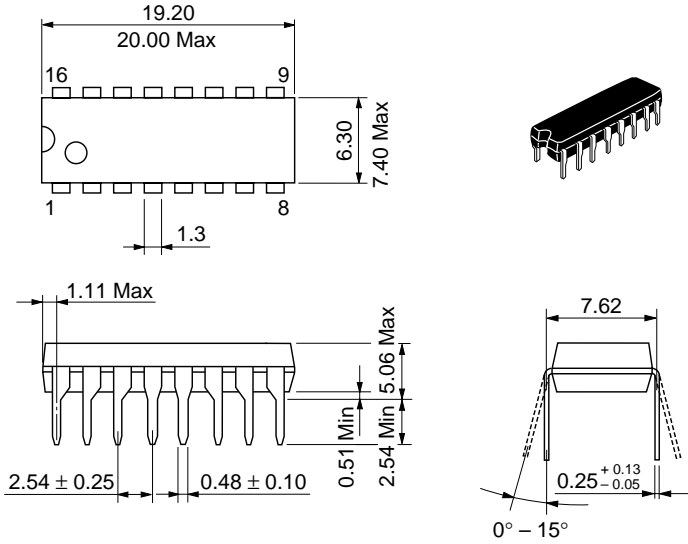
Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

| Item | Symbol | Typ | Unit | Condition |
|-------------------------------|-----------------|------|------|-------------------------|
| Input capacitance | C _{IN} | 4.5 | pF | V _{CC} = 5.5 V |
| Power dissipation capacitance | C _{PD} | 60.0 | pF | V _{CC} = 5.0 V |

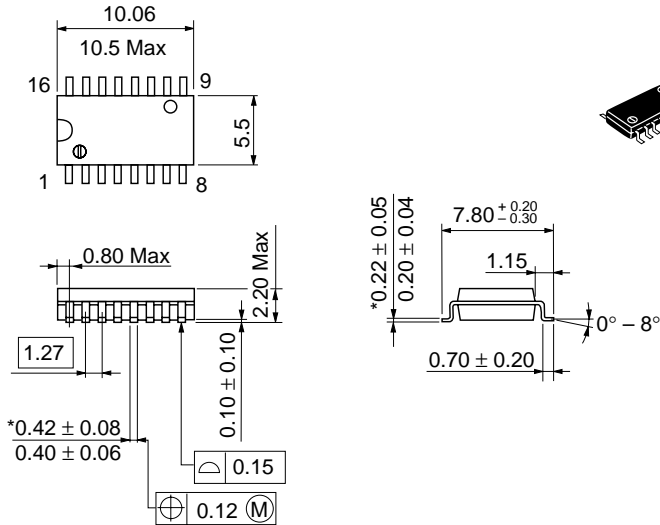
Package Dimensions

Unit: mm



| | |
|------------------------|----------|
| Hitachi Code | DP-16 |
| JEDEC | Conforms |
| EIAJ | Conforms |
| Mass (reference value) | 1.07 g |

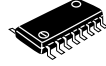
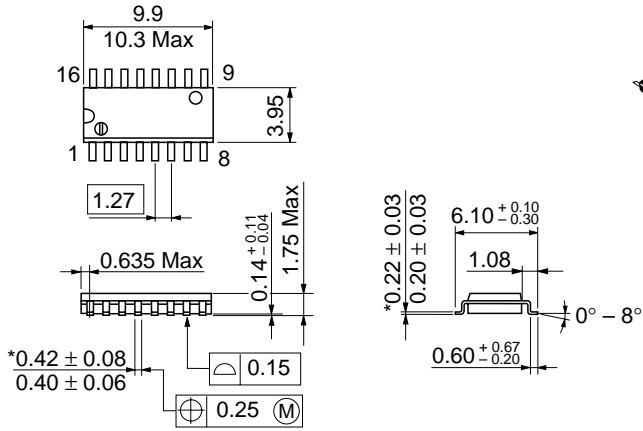
Unit: mm



*Dimension including the plating thickness
Base material dimension

| | |
|------------------------|----------|
| Hitachi Code | FP-16DA |
| JEDEC | — |
| EIAJ | Conforms |
| Mass (reference value) | 0.24 g |

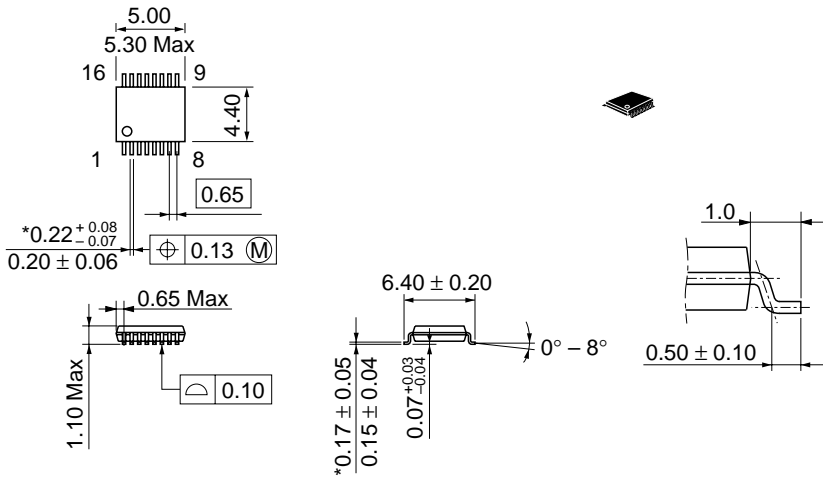
Unit: mm



*Dimension including the plating thickness
Base material dimension

| | |
|------------------------|----------|
| Hitachi Code | FP-16DN |
| JEDEC | Conforms |
| EIAJ | Conforms |
| Mass (reference value) | 0.15 g |

Unit: mm



*Dimension including the plating thickness
Base material dimension

| | |
|------------------------|----------|
| Hitachi Code | TTP-16DA |
| JEDEC | — |
| EIAJ | — |
| Mass (reference value) | 0.05 g |

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HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL North America : <http://semiconductor.hitachi.com/>
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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1> (408) 433-0223

Hitachi Europe GmbH
Electronic Components Group
Dornacher StraÙe 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 585160

Hitachi Asia Ltd.
Hitachi Tower
16 Collyer Quay #20-00,
Singapore 049318
Tel: <65>-538-6533/538-8577
Fax : <65>-538-6933/538-3877
URL : <http://www.hitachi.com.sg>

Hitachi Asia Ltd.
(Taipei Branch Office)
4/F, No. 167, Tun Hwa North Road,
Hung-Kuo Building,
Taipei (105), Taiwan
Tel: <886>-(2)-2718-3666
Fax : <886>-(2)-2718-8180
Telex : 23222 HAS-TP
URL : <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon,
Hong Kong
Tel : <852>-(2)-735-9218
Fax : <852>-(2)-730-0281
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