Micro Networks
A DIVISION OF UNITRODE CORPORATION

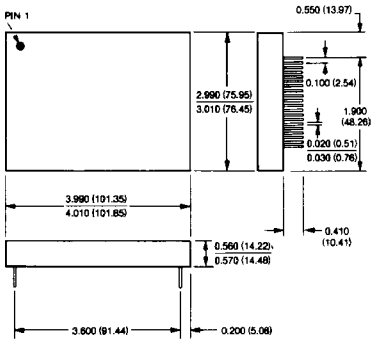
MN5420

20-Bit DYNAMIC RANGE
FLOATING-POINT
A/D CONVERTER

FEATURES

- **320kHz Conversion Rate**
- **Floating-Point 16-Bit Output:**
  12-Bit Mantissa
  4-Bit Exponent
- **120dB Dynamic Range:**
  10V Input Range
  10μV LSB
- **Instantaneous, Hardware-Controlled Gain Ranging**
- **9 Gain Ranges**
  G = 1, 2, 4, . . . 256
- **66dB Peak Signal to Peak Noise**
- **—100dB Absolute Noise Floor**
- **Differential Input, 60dB CMRR**
- **Rugged Hybrid Construction in a 3" x 4" x 5/8" Shielded Metal Case**

40 PIN MODULE



Dimensions in Inches (millimeters)

DESCRIPTION

MN5420 is a Floating-Point A/D Converter whose 16-bit digital output consists of a 12-bit mantissa and a 4-bit exponent. The device has a 10V full scale range (± 5V input range) yet is capable of resolving signals as small as 10μV. This 120dB dynamic range is equal to that of a 20-bit A/D converter, and it combines with MN5420's outstanding 320kHz conversion rate (3.125μsec conversion time) to yield an unequaled combination of resolution and speed.

MN5420 consists of a 1μsec, 12-bit ADC preceeded by a 4-bit, geometric, flash ADC, a 9-range programmable-gain amplifier (PGA) and two T/H amplifiers. The flash ADC and PGA together constitute a flash-autoranger function. The flash converter rapidly (200nsec) and coarsely digitizes the analog input. Its 4-bit, geometrically encoded, digital output programs the PGA gain to an optimum level (G = 1, 2, 4, 8, . . . 256) to ensure utilization of the full input range of the 12-bit A/D for each 12-bit sample. The PGA is preceeded and followed by T/H functions. The first T/H uses an "integrate and hold" architecture. It contributes very little broadband noise and effectively anti-alias filters the input signal with a sinx/x function. The T/H following the PGA acquires the amplified input signal and holds it constant while the 12-bit A/D performs its conversion. The output of the 12-bit A/D becomes MN5420's mantissa; the 4-bit code that programmed the PGA becomes its exponent.

MN5420 is designed for use in either time or frequency-domain applications requiring wide-dynamic-range digitizing at high speeds. In frequency-domain digital-signal-processing applications like radar or spectrum analysis, MN5420 operates almost distortion free with a −100dB noise floor while maintaining 66dB between peak signal and peak noise components in its output spectrum. In time-domain data-acquisition applications like waveform analysis, MN5420 has the effect of greatly expanding midrange resolution to 10μV while maintaining full-scale resolution at 2.4mV.

MN5420 is constructed as 4 thin-film hybrids mounted on a multilayer p.c. card. The card is shielded on 6 sides with a 3" x 4" x 5/8" aluminum shell and potted with a thermally conductive compound.

March 1988

Micro Networks
A DIVISION OF UNITRODE CORPORATION
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MN5420 FLOATING-POINT A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−25°C to +85°C
Specified Temperature Range	0°C to +70°C
Storage Temperature Range	−25°C to +85°C
$+V_{CC}$ Supply (Pins 21, 22, 23)	−0.5 to +18 Volts
$-V_{CC}$ Supply (Pins 31, 32, 33)	+0.5 to −18 Volts
$+V_{dd}$ Supply (Pins 26, 27, 28)	−0.5 to +7 Volts
Analog Input Voltage (Pin 36 or Pin 39)	± 10 Volts
Differential Input Voltage (Pin 36 to 39)	± 7.5 Volts
Digital Input Voltage (Pins 17, 20)	−0.5 to +5.5 Volts

ORDERING INFORMATION

PART NUMBER ——— **MN5420**

Standard part is specified for 0°C to +70°C operation. Please contact factory for information regarding extended temperature ranges or applicable Military screening.

SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V, +Vdd = +5V unless otherwise indicated)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range: Differential Common Mode		±5 ±5		Volts Volts
Input Impedance (Pin 36 or 39)		5		kΩ
CMRR (d.c.)		60		dB
Input Offset Voltage (Note 1): Initial (+25°C) Drift		±1 ±10		mV µV/°C
DIGITAL INPUTS (Clock, $\overline{OE}$)				
Logic Levels: Logic "1" Logic "0"	+2.4		 +0.8	Volts Volts
Logic Loading: Clock: Logic "1" (V_{IH} = +2.7V) Logic "0" (V_{IL} = +0.4V) $\overline{OE}$: Logic "1" (V_{IH} = +2.7V) Logic "0" (V_{IL} = +0.4V)			+80 −2.4 +40 −0.8	µA mA µA mA
Clock Input (Note 2): Frequency Negative Pulse Width	1.6	320	 2.4	kHz µsec
TRANSFER CHARACTERISTICS				
Gain Error (Note 3): Initial (+25°C) Drift		±1 TBD		% ppm/°C
Gain Matching Between Adjacent Gain Ranges		±0.05		%
Gain Switching Threshold Accuracy (Note 4)		±5		%
Distortion (Note 5)		−66		dB
Input Noise (d.c. to 160kHz)		60		µVrms
DYNAMIC CHARACTERISTICS				
Conversion Time Conversion Rate		3.125 320		µsec kHz
Integrate and Hold Amplifier Integrate Time (Note 6)	0.95	1	1.05	µsec
Input Signal Bandwidth (Note 6)		160		kHz
Delay Falling Edge $\overline{OE}$ to Output Data Valid Delay Rising Edge $\overline{OE}$ to Output Disabled			40 60	nsec nsec
Delay Rising Edge Clock to Output Data Valid for (n-1) Conversion (Note 7)			50	nsec
DIGITAL OUTPUTS				
Logic Levels: Logic "1" (I_{OH} = 1mA) Logic "0" (I_{OL} = −12mA)	+2.4		 +0.4	Volts Volts
POWER SUPPLIES				
Power Supply Range: ±15V Supplies +5V Logic Supply	±14.55 +4.75	±15 +5	±15.45 +5.25	Volts Volts
Power Supply Rejection: +15V Supply −15V Supply +5V Logic Supply		TBD TBD TBD		%FSR/% Supply %FSR/% Supply %FSR/% Supply
Current Drains: +15V Supply −15V Supply +5V Logic Supply		152 −158 410		mA mA mA
Power Consumption		6.7		Watts

SPECIFICATION NOTES:

1. Ideally, with an input of zero volts, MN5420's exponent output will be 0000, and its mantissa output will "flicker" between all "1's" and all "0's". Because system noise makes it impossible to measure the instantaneous input voltage at which this event actually occurs, input offset voltage or system offset voltage is defined as the average of a number of such measurements. It can also be defined as the d.c. component of an FFT for an input signal small enough to keep the PGA in the G=256 configuration.
2. MN5420's clock rate or conversion rate can be as high as 320kHz. If slower clock rates are used, one must ensure that the negative pulse width not exceed the 1.6μsec min and 2.4μsec max limits. If the positive pulse width is widened to accommodate this limitation, it simply means that output data is held longer. Please note that front-end integrate time is 1μsec regardless of clock rate.
3. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full input voltage span from the input voltage at which the output changes from 0111 1111 1110 to 0111 1111 1111 (exponent=1000) to the input voltage at which the output changes from 1000 0000 0000 to 1000 0000 0001 (exponent=1000).
4. As described in the Description of Operation, the actual input voltages at which the PGA switches gains are trimmed to be 20% below their theoretical values to avoid overranging the input of the 12-bit A/D. The actual switching voltage will be within 5% of this −20% value.
5. Distortion is defined in the frequency domain to be the difference between the signal peak and the noise peak in MN5420's output spectrum.
6. The integrate, hold and dump amplifier integrates for 1μsec ±0.05μsec. This has the effect of operating on the input signal with a sinx/x function with nulls at 1MHz, 2MHz, etc..
7. Because of MN5420's "pipelined" conversion technique, output data for the (n−1) conversion becomes valid on the rising clock edge halfway through the nth conversion. Output data for the nth conversion becomes valid halfway through the (n+1) conversion. See timing diagram.

Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

APPLICATIONS INFORMATION

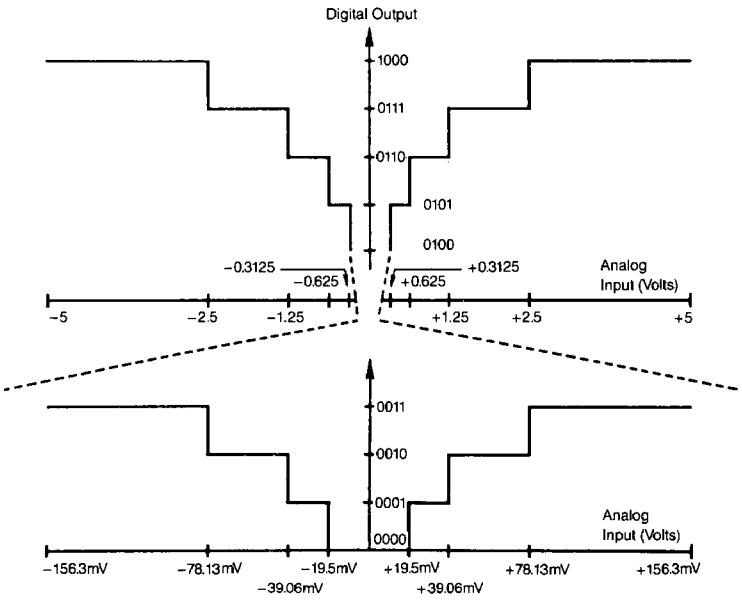
DESCRIPTION OF OPERATION—MN5420 wide-dynamic-range, floating-point A/D converter produces a 16-bit stream of data (4 bits of exponent, 12 bits of mantissa) at a 320kHz rate (3.1μsec conversion time) and can digitize signals as large as 10V or as small as 10μV for an impressive 120dB dynamic range.

As shown in the adjacent block diagram, MN5420 consists of a 12-bit A/D converter preceeded by a 4-bit flash A/D converter, a 9-range programmable-gain amplifier (PGA) and two track-hold (T/H) amplifiers. The 12-bit A/D has a 1μsec conversion time and uses two's complement coding. Impressive in its own right, the 12-bit A/D is immediately preceeded by one of the track-hold amplifiers and the programmable-gain amplifier with its 9 gain ranges (1, 2, 4, 8, 16, 32, 64, 128, 256). The gain of the PGA is controlled by a 4-bit word, and at any instant, the selected gain is such that the largest possible signal is always presented to the 12-bit A/D. When the input signal is small, the PGA gain is high; when the input signal is large, the PGA gain is low. For input signals smaller than ±19.5mV, for example, the PGA gain will be 256. The value of an LSB at this point is 39mV/4096=9.5μV.

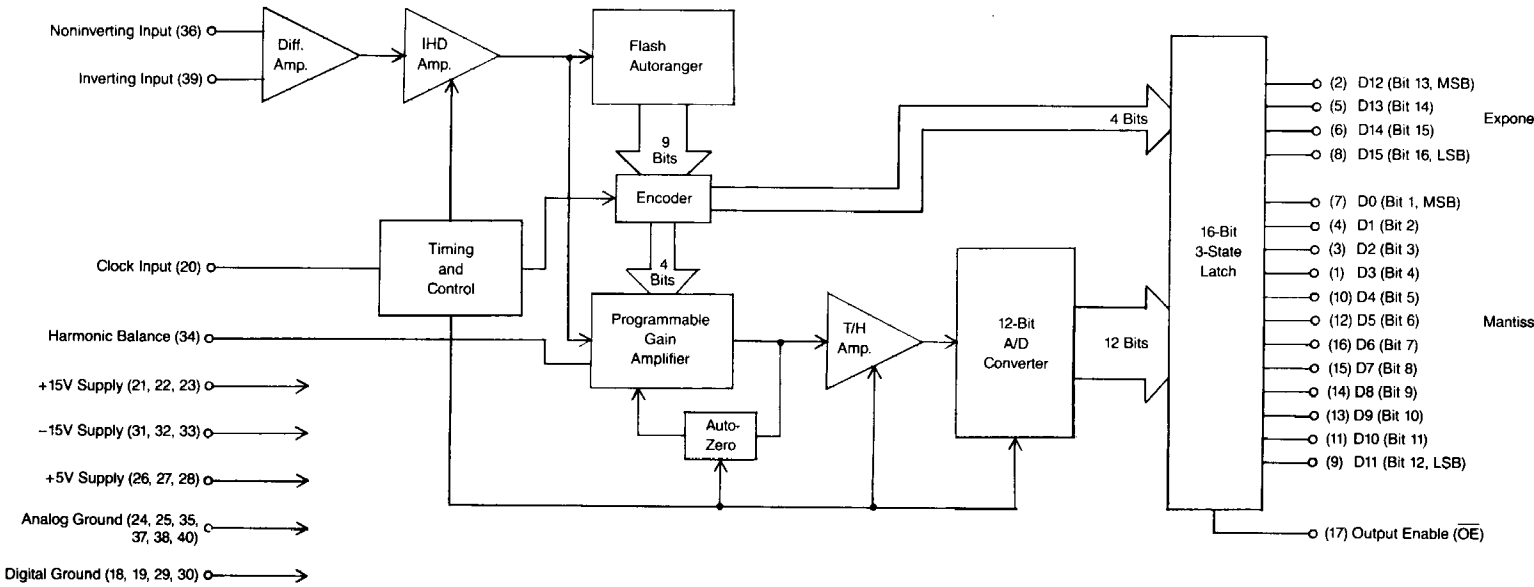
The gain of the PGA is selected by the flash autoranger. The flash autoranger is a flash type A/D converter with a geometric rather than a binary input-output transfer function. The flash autoranger has only 4-bits of resolution, but it is very fast (200nsec conversion time). It rapidly and coarsely determines the approximate amplitude of the input signal and uses the information to set the gain of the PGA. The 4-bit output of the flash autoranger also becomes the 4-bit exponent output of the MN5420.

The geometric transfer function of the flash autoranger is shown below. The 4-bit output changes codes each time the input voltage doubles or halves. Subsequently, the gain of the PGA is doubled whenever the input to the A/D falls below half scale, and the PGA gain is halved whenever the input to the A/D reaches full scale.

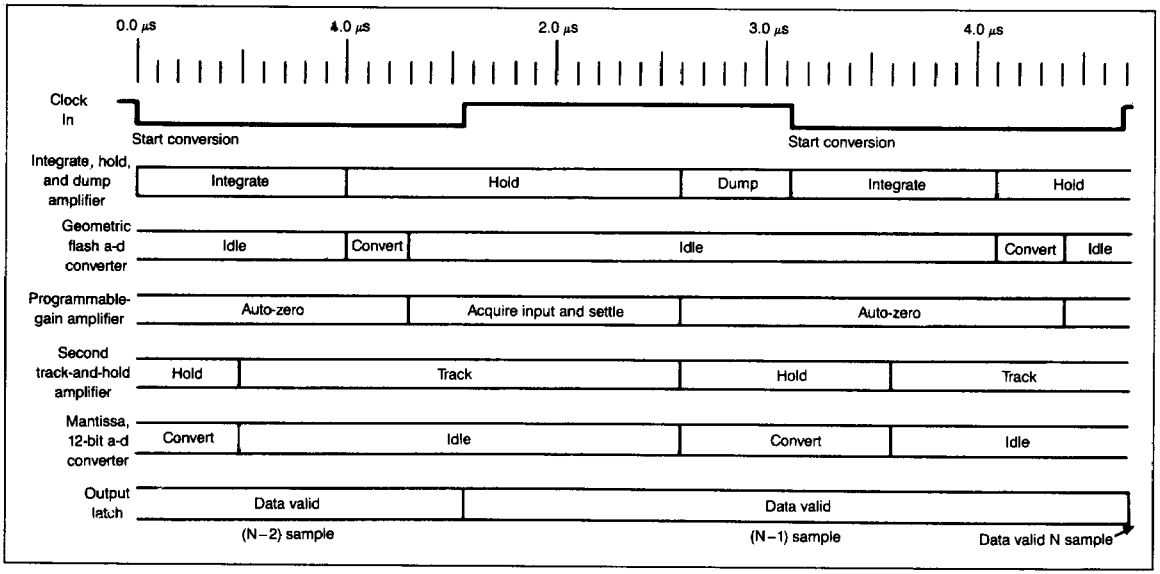
In the actual implementation of the flash autoranger, the transition voltages are trimmed to be 20% below the theoretical voltages shown above. The transition from G=1 to G=2, for example, occurs at ±2V rather than ±2.5V. This is to ensure, given the gain inaccuracies of other components in the system, that the 12-bit A/D is never "overranged" by having its input exceed ±5V.



BLOCK DIAGRAM



TIMING DIAGRAM



TIMING DIAGRAM NOTES:

1. MN5420's clock rate or conversion rate can be as high as 320kHz. If slower clock rates are used, one must ensure that the negative pulse width not exceed the 1.6μsec min and 2.4μsec max limits. If the positive pulse width is widened to accommodate this limitation, it simply means that output data is held longer. Please note that front-end integrate time is 1μsec regardless of clock rate.
2. The integrate, hold and dump amplifier integrates for 1μsec ± 0.05μsec. This has the effect of operating on the input signal with a sinx/x function with nulls at 1MHz, 2MHz, etc..
3. Because of MN5420's "pipelined" conversion technique, output data for the (n−1) conversion becomes valid on the rising clock edge halfway through the nth conversion. Output data for the nth conversion becomes valid halfway through the (n+1) conversion. See timing diagram.

The flash autoranger is preceeded by a newly developed circuit called an Integrate, Hold and Dump amplifier (IHD). This block is similar to a sample-hold or track-hold amplifier in that it holds the input signal constant while the flash autoranger and PGA operate on it. The integrate and hold technique gives it fast acquisition time (1μsec), low noise and narrow bandwidth. The dumping action clears the hold capacitor after each sample and eliminates hysteresis or memory of any previous samples.

Referring to the timing diagram, one sees that the falling edge of clock fires a one-shot that drives the integrate and hold into the integrate mode for 1μsec (±0.5μsec). This is followed by a 300nsec interval during which the flash autoranger programs the gain of the PGA. The PGA and second T/H amplifier require approximately 1.3μsec to settle and acquire. After the second T/H goes into hold, the 12-bit A/D requires 1μsec to perform its conversion.

Because of the "pipelined" aspect of MN5420's conversion process, output data for the nth conversion does not become valid until sometime during the (n+1) conversion. Output data becomes valid 50nsec (max) after the next **rising** clock edge and remains valid until the subsequent rising clock edge.

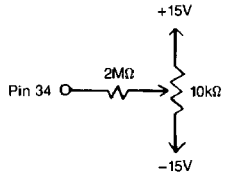
LAYOUT CONSIDERATIONS AND GROUNDING—Proper attention to layout and grounding is necessary to achieve the specified performance from MN5420. The unit's Analog Ground pins (pins 24, 25, 35, 37, 38, 40) and Digital Ground pins (pins 18, 19, 29, 30) are not connected to each other internally. They must be tied together as close to the device as possible and connected to system analog ground preferably through a very large ground plane beneath the device.

Coupling between analog inputs and digital signals should be minimized to avoid noise pick-up. Care should be taken to avoid long runs or analog runs close to digital lines. Input signal lines should be as short as possible.

MN5420's power supply pins are bypassed internal to the device with 2μF tantalum capacitors paralleled with 0.1μF ceramic capacitors.

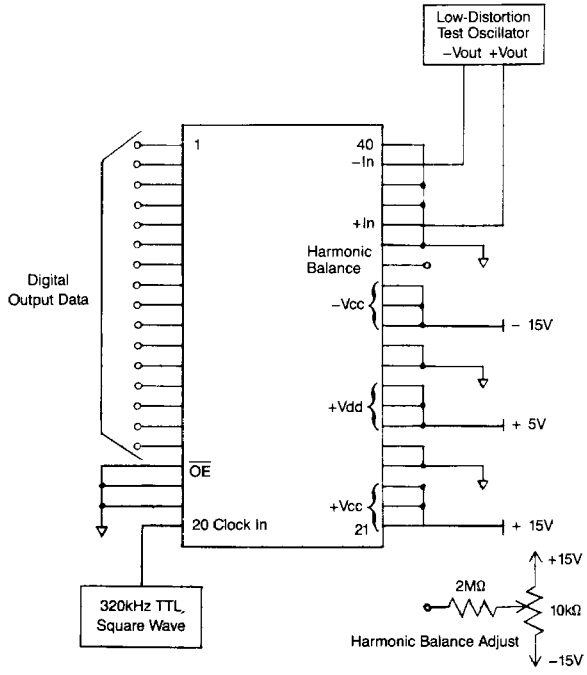
HARMONIC BALANCE—The Harmonic Balance input (pin 34) on the MN5420 is used to minimize even-order harmonic distortion. These distortions arise as a result of discountinuities in the transfer function of the A/D at gain switching points. The discontinuities are caused by offset voltage error in the internal programmable gain amplifier and may get worse as a function of temperature.

The diagram below shows a manual adjustment circuit which may be used to minimize the offset voltage error, and thereby the harmonic distortion, at a given temperature.This pin may also be driven by a D/A converter through the 2 MΩ resistor shown as part of an automatic calibration scheme. Leave pin 34 open if harmonic adjust feature is not used.



HARMONIC ADJUST CIRCUIT

MN5420 TEST CIRCUIT LAYOUT



TEST CIRCUIT NOTES:

1. Analog Grounds (pins 24, 25, 35, 37, 38, 40) and Digital Grounds (pins 18, 19, 29, 30) must be tied together as close to the device as possible and connected to system analog ground preferably through a very large ground plane beneath the package. See Layout Considerations and Grounding section of this data sheet.
2. Bypass supply pins with 15μF tantalum capacitors in parallel with 0.01 μF ceramic capacitors.
3. Even order harmonic distortion components seen in the MN5420's output spectrum can be minimized by connecting the Harmonic Balance Adjust circuit shown above to pin 34. This pin may also be driven by the output of a D/A converter through the 2MΩ resistor as part of an automatic calibration scheme. See the Harmonic Balance section of this data sheet.

PIN DESIGNATIONS

1	Bit 4 (D3)	40	Analog Ground
2	Bit 13 (D12)	39	Inverting Input (−In)
3	Bit 3 (D2)	38	Analog Ground
4	Bit 2 (D1)	37	Analog Ground
5	Bit 14 (D13)	36	Noninverting Input (+In)
6	Bit 15 (D14)	35	Analog Ground
7	Bit 1 (D0)	34	Harmonic Balance
8	Bit 16 (D15)	33	−15V Supply (−Vcc)
9	Bit 12 (D11)	32	−15V Supply (−Vcc)
10	Bit 5 (D4)	31	−15V Supply (−Vcc)
11	Bit 11 (D10)	30	Digital Ground
12	Bit 6 (D5)	29	Digital Ground
13	Bit 10 (D9)	28	+5V Supply (+Vdd)
14	Bit 9 (D8)	27	+5V Supply (+Vdd)
15	Bit 8 (D7)	26	+5V Supply (+Vdd)
16	Bit 7 (D6)	25	Analog Ground
17	Output Enable ($\overline{OE}$)	24	Analog Ground
18	Digital Ground	23	+15V Supply (+Vcc)
19	Digital Ground	22	+15V Supply (+Vcc)
20	Clock Input	21	+15V Supply (+Vcc)

MN5420 DIGITAL OUTPUT CODING—The digital output coding of MN5420 consists of mantissa and exponent information. The four bits of exponent are straight binary coded, and they appear on data lines D12(MSB)–D15(LSB). As shown in the following tables, the code 0000 corresponds to an exponent value of 0 and a PGA gain of 256; the code 1000 corresponds to an exponent value of 8 and a PGA gain of 1, etc. The 12 bits of mantissa are two's complement coded, and they appear on data lines D0(MSB)–D11(LSB). The mantissa is the direct output of MN5420's internal 12-bit A/D, and the input-output coding of that device is also detailed in the following table.

MN5420's input-output coding is most easily understood if one views the device as 9 12-bit A/D converters, each with an input voltage range ½ that of the previous converter and each with an LSB value ½ that of the previous converter. The exponent tells which of the 9 A/D's has been used for a given conversion, and the mantissa is the 12-bit result of that conversion.

The digital output coding of the 12-bit A/D alone is shown on the next page. The value of an instantaneous LSB (ILSB) is equivalent to MN5420's instantaneous input voltage range (IFSR) (indicated by the exponent) divided by 4096. In the table, the analog-input voltages listed are the theoretical values for the digital output code transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated.

For example, with PGA G=1 (exponent=1000=8), the value of the LSB will be 2.44mV, and the transition from output code 0111 1111 1110 to code 0111 1111 1111 will ideally occur at an input voltage of +4.99756V. Subsequently, any voltage greater than 4.99756V will give a digital output of 0111 1111 1111. The transition from digital code 0011 1111 1111 to 0100 0000 0000 will ideally occur at an input voltage of +2.5V when PGA gain=1. Since this is also the theoretical voltage at which the PGA gain may switch from 1 to 2, the 12-bits of A/D output may go to 0111 1111 1111 (equal to positive full scale) if PGA G=2 (exponent=0111=7).

Reconstructing analog signal levels from digital output information is accomplished using the following formula:

$$V_{in} = \left(\frac{\text{Mantissa Count}}{2^n}\right) \text{IFSR} - \frac{1}{2}\text{IFSR} + \left(\frac{1}{2^{n+1}}\right)\text{IFSR}$$

where:

n=number of bits (12) in the mantissa. $2^n = 4096$

Mantissa count $= (\overline{MSB} \times 2^{11}) + (\text{Bit } 2 \times 2^{10}) + \ldots + (\text{LSB} \times 2^0)$

IFSR=Instantaneous Full Scale Range=$\frac{10 \times 2^{exp}}{256}$ Volts

exp=exponent=$(MSB \times 2^3) + (\text{bit } 2 \times 2^2) + (\text{bit } 3 \times 2^1) + (LSB \times 2^0)$

(Mantissa Count÷4096) indicates what percentage of IFSR the digital output corresponds to. After this is multiplied by IFSR, ½IFSR is subtracted to account for the fact that the device has a bipolar input range. $\left(\frac{1}{2^{n+1}}\right)$ IFSR corresponds to ½LSB, and this is added to account for the fact that MN5420's transfer function is symmetrically located in its input voltage range with the negative full-scale output transition occuring at −F.S. +1LSB and the positive full-scale output transition occuring at +F.S.−1LSB.

Therefore:

$$V_{in} = \left[\left(\frac{\text{Mantissa Count}}{2^n}\right)\text{IFSR}\right] - \left[\frac{1}{2}\text{IFSR}\right] + \left[\left(\frac{1}{2^{n+1}}\right)\text{IFSR}\right]$$

$$V_{in} = \left[\left(\frac{\text{Mantissa Count}}{2^n}\right) - \frac{1}{2} + \left(\frac{1}{2^{n+1}}\right)\right]\text{IFSR}$$

$$V_{in} = \left[\left(\frac{\text{Mantissa Count}}{4096}\right) - \frac{1}{2} + \frac{1}{8192}\right]\text{IFSR}$$

$$V_{in} = \left(\frac{\text{Mantissa Count}}{4096} - \frac{4095}{8192}\right)\left(\frac{10 \times 2^{exp.}}{256}\right) \text{ Volts}$$

Examples:

mantissa = 0111 1111 1111 = 4095
exponent = 1000 = 8

$$V_{in} = \left(\frac{4095}{4096} - \frac{4095}{8192}\right)\left(\frac{10 \times 256}{256}\right) \text{ Volts}$$

$$V_{in} = 10\left(\frac{4095}{8192}\right) \text{ Volts}$$

$$V_{in} = +4.9988 \text{ Volts}$$

mantissa = 1000 0000 0000 = 0
exponent = 1000 = 8

$$V_{in} = \left(\frac{0}{4096} - \frac{4095}{8192}\right)\left(\frac{10 \times 256}{256}\right) \text{ Volts}$$

$$V_{in} = -10\left(\frac{4095}{8192}\right) \text{ Volts}$$

$$V_{in} = -4.9988 \text{ Volts}$$

mantissa = 0000 0000 0001 = 2049
exponent = 0000 = 0

$$V_{in} = \left(\frac{2049}{4096} - \frac{4095}{8192}\right)\left(\frac{10 \times 1}{256}\right) \text{ Volts}$$

$$V_{in} = \left(\frac{3}{8192}\right)\left(\frac{10}{256}\right) \text{ Volts}$$

$$V_{in} = +14.305\mu V$$

PGA Gain Codes

Exponent (D12-D15)	Exponent Value	PGA Gain	Approximate Input Range	Mantissa LSB Value
1000	8	1	±5V	2.44mV
0111	7	2	±2.5V	1.22mV
0110	6	4	±1.25V	610μV
0101	5	8	±0.625V	305μV
0100	4	16	±0.3125V	152.6μV
0011	3	32	±0.15625V	76.3μV
0010	2	64	±0.078125V	38.15μV
0001	1	128	±0.039063V	19.07μV
0000	0	256	±0.019531V	9.54μV

PGA Gain Switching Thresholds

PGA Code Transition (D12-D15)	PGA Gain Change	Theoretical Input Voltage	Actual Voltage (Note)
(D12-D15) → (D12-D15)			
1000 → 0111	1 → 2	±2.5V	±2.0V
0111 → 0110	2 → 4	±1.25V	±1.0V
0110 → 0101	4 → 8	±0.625V	±0.5V
0101 → 0100	8 → 16	±0.3125V	±0.25V
0100 → 0011	16 → 32	±0.15625V	±0.125V
0011 → 0010	32 → 64	±0.078125V	±0.0625V
0010 → 0001	64 → 128	±0.039063V	±0.03125V
0001 → 0000	128 → 256	±0.019531V	±0.015625V

Note: In order to avoid overranging the input to the 12-bit A/D, the PGA's gain-switching thresholds are adjusted to be approximately 20% below the theoretical levels discussed in the Description of Operation.

12-BIT A/D DIGITAL OUTPUT CODING

Analog voltages listed are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated. For example, the transition from output code 0111 1111 1110 to code 0111 1111 1111 will ideally occur at an input voltage of +F.S.−1LSB. Subsequently, any voltage greater than this level will give an output of a "0" and all "1's". The transition from output code 1111 1111 1111 to code 0000 0000 0000 will ideally occur at zero volts. The 1000 0000 0000 to 1000 0000 0001 transition will ideally occur at an input voltage of −F.S.+1LSB. An input more negative than this level will give an output of a "1" and all "0's".

12-Bit A/D Digital Output Coding

Analog Input	Digital Output D0 → D11 (MSB → LSB)
+Full Scale	0111 1111 1111
+F.S. − 1 LSB	0111 1111 111Ø
+½ F.S. + 1 LSB	0100 0000 000Ø
+½ F.S.	ØØØØ ØØØØ ØØØØ
+½ F.S. − 1 LSB	0011 1111 111Ø
+1 LSB	0000 0000 000Ø
0.0000V	ØØØØ ØØØØ ØØØØ
−1 LSB	1111 1111 111Ø
−½ F.S. + 1 LSB	1100 0000 000Ø
−½ F.S.	1ØØØ ØØØØ ØØØØ
−½ F.S. − 1 LSB	1011 1111 111Ø
−F.S. + 1 LSB	1000 0000 000Ø
−Full Scale	1000 0000 0000

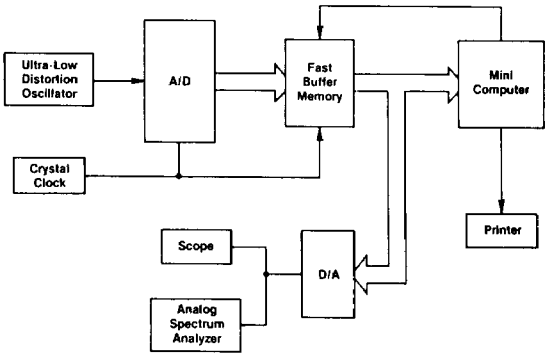
MN5420 Overall Input-Output Coding

Input Voltage (Volts)	PGA Gain	Exponent (MSB — LSB)	Mantissa (MSB — LSB)	Mantissa LSB Value
+5	1	1000	0111 1111 1111	2.44mV
+4.99756	1	1000	0111 1111 111Ø	2.44mV
+2.50244	1	1000	0100 0000 000Ø	2.44mV
+2.5	1	1000	0ØØØ ØØØØ ØØØØ	2.44mV
+2.5	2	0111	0111 1111 1111	1.22mV
+2.49878	2	0111	0111 1111 111Ø	1.22mV
+1.25122	2	0111	0100 0000 000Ø	1.22mV
+1.25	2	0111	0ØØØ ØØØØ ØØØØ	1.22mV
+1.25	4	0110	0111 1111 1111	610μV
+1.24939	4	0110	0111 1111 111Ø	610μV
+0.62561	4	0110	0100 0000 000Ø	610μV
+0.625	4	0110	0ØØØ ØØØØ ØØØØ	610μV
+0.625	8	0101	0111 1111 1111	305μV
+0.62470	8	0101	0111 1111 1111Ø	305μV
+0.312805	8	0101	0100 0000 000Ø	305μV
+0.3125	8	0101	0ØØØ ØØØØ ØØØØ	305μV
+0.3125	16	0100	0111 1111 1111	153μV
+0.312347	16	0100	0111 1111 111Ø	153μV
+0.156403	16	0100	0100 0000 000Ø	153μV
+0.15625	16	0100	0ØØØ ØØØØ ØØØØ	153μV
+0.15625	32	0011	0111 1111 1111	76μV
+0.156174	32	0011	0111 1111 111Ø	76μV
+0.078201	32	0011	0100 0000 000Ø	76μV
+0.078125	32	0011	0ØØØ ØØØØ ØØØØ	76μV
+0.078125	64	0010	0111 1111 1111	38μV
+0.078087	64	0010	0111 1111 111Ø	38μV
+0.039101	64	0010	0100 0000 000Ø	38μV
+0.039063	64	0010	0ØØØ ØØØØ ØØØØ	38μV
+0.039063	128	0001	0111 1111 1111	19μV
+0.039044	128	0001	0111 1111 111Ø	19μV
+0.019550	128	0001	0100 0000 000Ø	19μV
+0.019531	128	0001	0ØØØ ØØØØ ØØØØ	19μV
+0.019531	256	0000	0111 1111 1111	9.5μV
+0.0195215	256	0000	0111 1111 111Ø	9.5μV
+0.0097656	256	0000	0ØØØ ØØØØ ØØØØ	9.5μV
+0.0048828	256	0000	00ØØ ØØØØ ØØØØ	9.5μV
+0.0000095	256	0000	0000 0000 000Ø	9.5μV
0.0000000	256	0000	ØØØØ ØØØØ ØØØØ	9.5μV
−0.0000095	256	0000	1111 1111 111Ø	9.5μV
−0.0048828	256	0000	11ØØ ØØØØ ØØØØ	9.5μV
−0.0097656	256	0000	1ØØØ ØØØØ ØØØØ	9.5μV
−0.0195215	256	0000	1000 0000 000Ø	9.5μV
−0.019531	256	0000	1000 0000 0000	9.5μV
−0.019531	128	0001	1ØØØ ØØØØ ØØØØ	19μV
−0.019550	128	0001	1000 0000 000Ø	19μV

CODING NOTES:
1. The output bits indicated as Ø will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated.
2. As described in the Description of Operation, the actual input voltages at which the PGA switches gains are trimmed to be 20% below their theoretical values to avoid overranging the input of the 12-bit A/D. The actual switching voltage will be within 5% of this −20% value.

MN5420 FFT CHARACTERIZATION—MN5420 has been characterized using discrete Fourier analysis on a system developed specifically to evaluate high-speed A/D converters in the frequency domain. As shown in the following diagram, the system consists of four main parts: a signal source, a system clock, a high-speed buffer-memory box, and a minicomputer. The signal generator is an ultra low distortion device, and the system clock is a quartz-crystal type. Together they ensure that input-signal distortion and clock jitter are not significant factors in the output spectrum. The signal generator creates clean sine waves of assorted amplitudes that are digitized by the A/D under test at a fixed sampling rate controlled by the system clock. The A/D under test has its output data strobed into the high-speed buffer-memory box, and the data is eventually transmitted to the minicomputer which generates a discrete Fourier transform using an FFT algorithm. The resulting spectrum is then displayed and eventually printed if necessary.

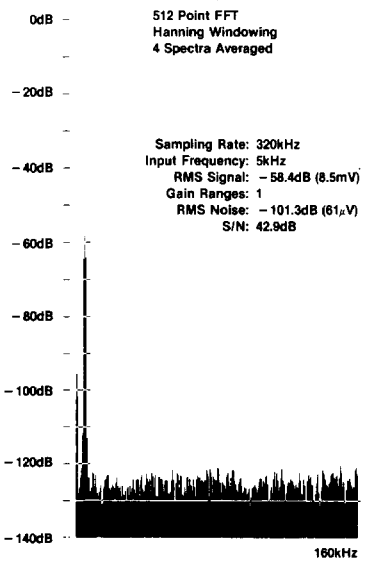
Frequency-Domain Testing of A/D Converters

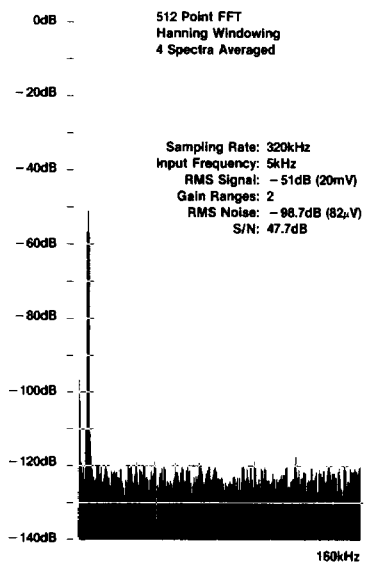


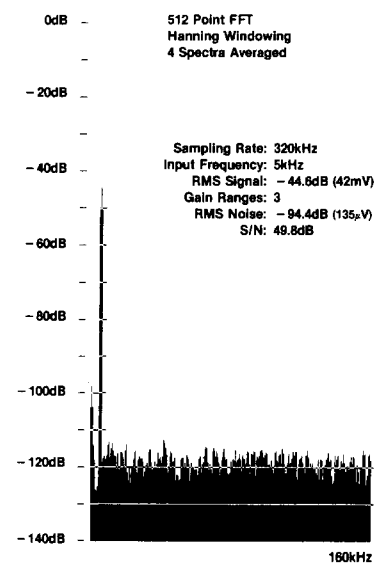
The ADC under test is continuously converting. Conversions are initiated on the falling edge of each clock pulse, and output data from the previous conversion is strobed into a three-state output latch on the rising edge. At the start of the test program, the minicomputer enables the fast buffer memory which rapidly acquires a preset number of successive samples. This sample sequence can be from 256 to 2048 words long, and each word can be up to 16 bits wide. The data is read from the buffer memory into the memory of the minicomputer which applies a Hanning window function to the sample sequence and performs the FFT. The resulting spectrum is then analyzed to determine rms signal level, rms noise level, and signal-to-noise ratio (SNR), and the spectrum and data are printed on the dot-matrix printer. If desired, up to 256 spectra can be taken in succession, and the spectra average used as the output.

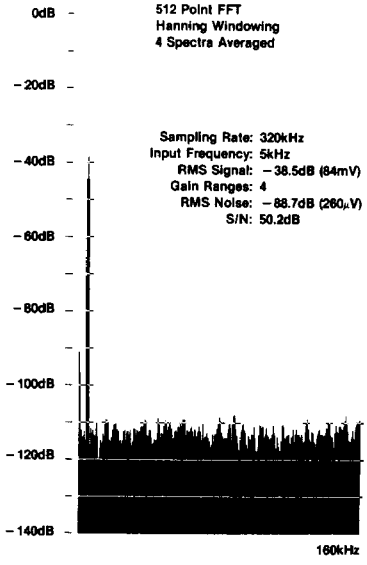
The following set of 9 FFT's are each 512-point transforms, and each represents the average of 4 spectra. For each successive spectrum, the input signal to MN5420 has been increased so as to exercise an additional gain range on the PGA. In the first spectrum, for example, an rms input signal of 8.5mV keeps the PGA locked in the gain=256 configuration. In the last spectrum, a full-scale input signal exercises all 9 gains of the PGA 4 times every signal period. The 5kHz input signal is sampled approximately 64 times each period, and the PGA will change gain 36 times during each period.

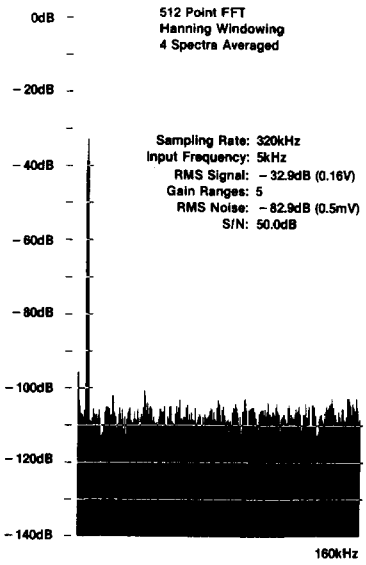
Note, in the first spectrum, that with very small input signals, MN5420's output noise level is approximately 100dB down and that all individual noise components are at least 120dB down. Note also that for any input amplitude, MN5420 maintains 66dB between its signal peak and the peak of any component in the noise floor be it harmonic or spurious.

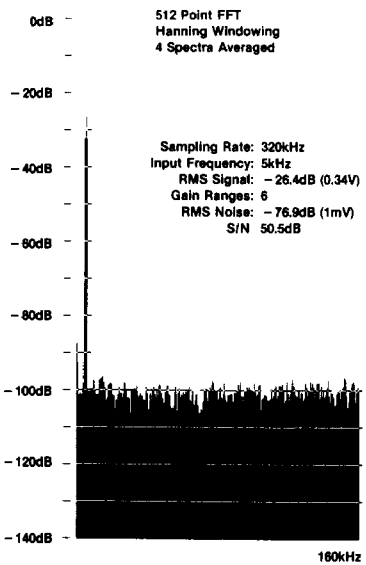


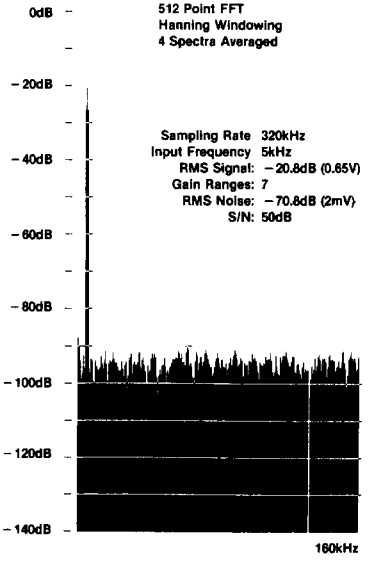


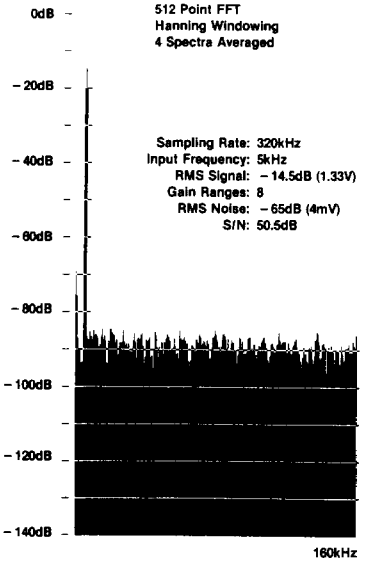


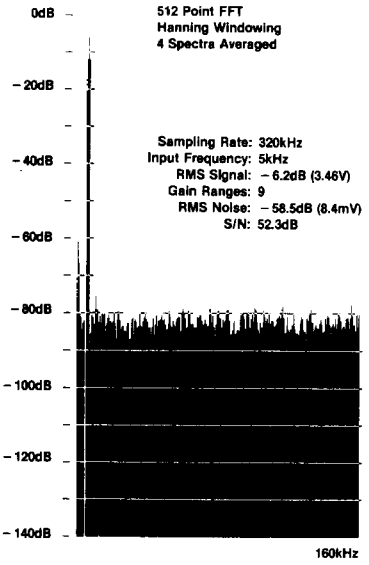

0dB
-20dB
-40dB
-60dB
-80dB
-100dB
-120dB
-140dB
512 Point FFT
Hanning Windowing
4 Spectra Averaged
Sampling Rate: 320kHz
Input Frequency: 5kHz
RMS Signal: -38.5dB (84mV)
Gain Ranges: 4
RMS Noise: -88.7dB (260μV)
S/N: 50.2dB
160kHz


0dB
-20dB
-40dB
-60dB
-80dB
-100dB
-120dB
-140dB
512 Point FFT
Hanning Windowing
4 Spectra Averaged
Sampling Rate: 320kHz
Input Frequency: 5kHz
RMS Signal: -32.9dB (0.16V)
Gain Ranges: 5
RMS Noise: -82.9dB (0.5mV)
S/N: 50.0dB
160kHz


0dB
-20dB
-40dB
-60dB
-80dB
-100dB
-120dB
-140dB
512 Point FFT
Hanning Windowing
4 Spectra Averaged
Sampling Rate: 320kHz
Input Frequency: 5kHz
RMS Signal: -26.4dB (0.34V)
Gain Ranges: 6
RMS Noise: -76.9dB (1mV)
S/N 50.5dB
160kHz


0dB
-20dB
-40dB
-60dB
-80dB
-100dB
-120dB
-140dB
512 Point FFT
Hanning Windowing
4 Spectra Averaged
Sampling Rate 320kHz
Input Frequency 5kHz
RMS Signal: -20.8dB (0.65V)
Gain Ranges: 7
RMS Noise: -70.8dB (2mV)
S/N: 50dB
160kHz


0dB
-20dB
-40dB
-60dB
-80dB
-100dB
-120dB
-140dB
512 Point FFT
Hanning Windowing
4 Spectra Averaged
Sampling Rate: 320kHz
Input Frequency: 5kHz
RMS Signal: -14.5dB (1.33V)
Gain Ranges: 8
RMS Noise: -65dB (4mV)
S/N: 50.5dB
160kHz


0dB
-20dB
-40dB
-60dB
-80dB
-100dB
-120dB
-140dB
512 Point FFT
Hanning Windowing
4 Spectra Averaged
Sampling Rate: 320kHz
Input Frequency: 5kHz
RMS Signal: -6.2dB (3.46V)
Gain Ranges: 9
RMS Noise: -58.5dB (8.4mV)
S/N: 52.3dB
160kHz