155MBPS - 1.25GBPS Post Amplifier and LD Driver

GENERAL DESCRIPTION

CS6718 integrated two main functions in a single chip providing optimal solutions for various fiber module applications. The functional blocks include a 1.25G post-amplifier, a continuous mode LD driver.

The post-amplifier receives AC coupled differential signal from pre-amplifier and performs the quantization amplifications. There are total four amplification stages excluding the output stage. The offset cancellation is built-in on chip. The output of the post-amplifier is configured as PECL. The LOS power threshold level is configurable by SD_SET voltage.

The LD driver performs the transmit function that receives the PECL differential signal TXINP/TXINN and convert to drive LD output driver. The LD driver is also controlled by TX_DIS signal. The laser driver includes differential modulation outputs and DC bias control output. The setting of output power level is controlled through automatic power control loop and is configurable by R_{MPD}. The setting of output power modulation level is configurable by MOD_SET voltage. The output can be connected to Laser diode either by AC or DC coupled.

CS6718 integrates essential building blocks for Fiber module design. Using CS6718, the module can achieve low cost and high performance fiber module and can be applied in FTTH, BPON, and GEPON.

APPLICATIONS

- SONET/SDH, FTTH, GEPON

FEATURES

Post Amplifier

- 155MBPS - 1.25GBPS
- -3dB bandwidth 850MHz – 20KHz
- 2mV sensitivity
- On-chip offset cancellation
- Programmable LOS function and Power detection
  - External ADC channel control
- LOS/SD programmable PECL/CMOS output
- Programmable power down

LD Driver

- Bias current up to 100mA
- Differential modulation current outputs up to 80mA
- Programmable bias and modulation current control
- Digital automatic power control loop
- Rise/Fall time < 200psec
- Continuous mode compatible

General

- Low power consumption (300mW)
- Single 3.3V supply with on-chip regulator
- Extended temperature range -40°C ~ +85°C
- QFN-28
- RoHS compliance package

BLOCK DIAGRAM

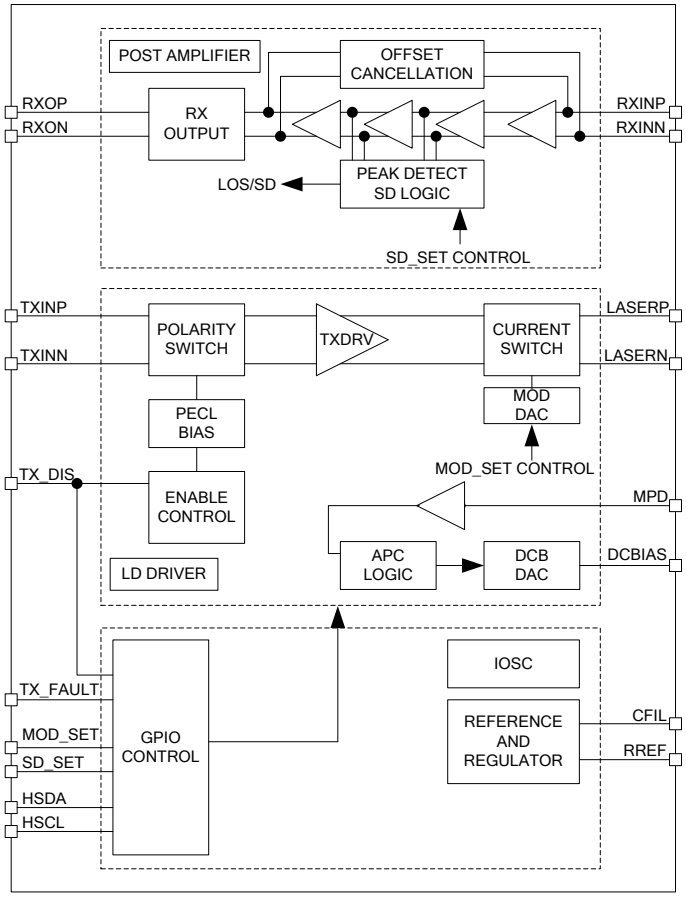


Figure 1 Block Diagram

PIN CONNECTION DIAGRAM

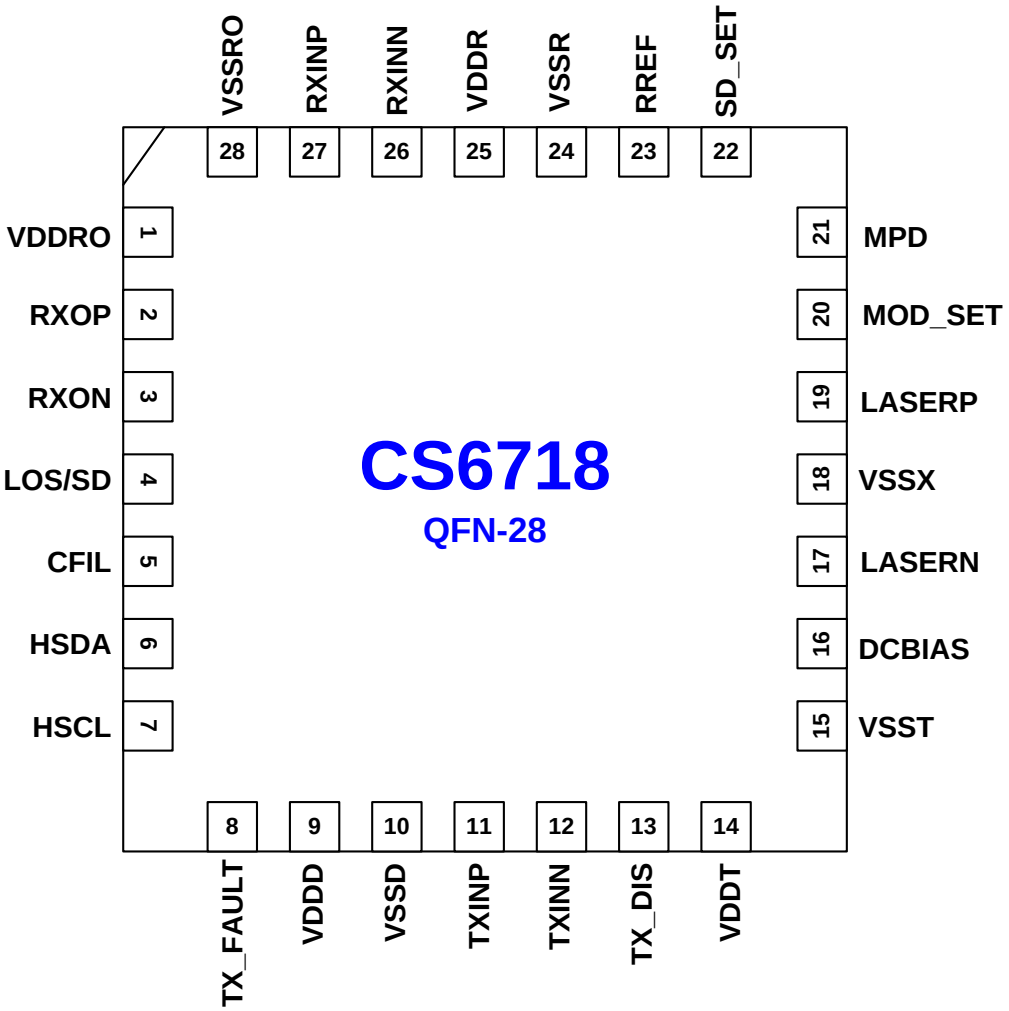


Figure 2 Pin Connection Diagram

PIN DESCRIPTION

NAME	PIN #	TYPE	DESCRIPTION
VDDRO	1	P	3.3V supply for the receive output buffers. Should have good decoupling to VSSRO
RXOP	2	A, OUT	Post amplifier positive data output.
RXON	3	A, OUT	Post amplifier negative data output.
LOS/SD	4	AD	Loss of Signal(SFP module)/signal detect signal(1*9 module). This pin can be configured in Open Drain output in SFP application, and be configured in CMOS or PECL output in 1*9 application.
CFIL	5	P	Internal 1.8V regulator output. The regulator supplies internal analog circuits and digital core logic. A good decoupling should be connected from this pin to VSS, typically 0.1uF in parallel with 10uF.
HSDA	6	D, OD, IO	ISP Interface Data. This pin is connected to host data line for performing in system programming function.
HSCL	7	D, OD, IO	ISP Interface Clock. This pin is connected to host data line for performing in system programming. This pin must be short to VDD in SFP mode, and this pin must be short to VSS in 1*9 mode
TX_FAULT	8	D, IO	FAIL Status Output. This pin is connected the APC fail status in SFP mode. For 1*9 module application, this pin must be short to VDD in SD PECL output, and be short to VSS in SD CMOS output.
VDDD	9	P	Digital Circuit Supply 3.3V. This pin should be connected to external 3.3V supply with good decoupling to VSSD.
VSSD	10	G	Digital Circuit Ground 0V. This pin connects to internal digital circuit ground and should have good decoupling to VDDD.
TXINP	11	A, I	Transmit Data Positive. This is positive of differential transmit data signals. This pin is internally biased to PECL level through 10K resistor.
TXINN	12	A, I	Transmit Data Negative. This is negative of differential transmit data signals. This pin is internally biased to PECL level through 10K resistor.
TX_DIS	13	I	TX_ disable Positive. This pin is TX_DISABLE control and can be in single-ended CMOS level,.
VDDT	14	P	3.3V supply for transmit output driver. Should have good decoupling to VSST.
VSST	15	G	LD DC Bias Driver Circuit Ground 0V. This pin connects to the ground of the Bias current source and should have good decoupling to VDDT.
DCBIAS	16	A, O	LD DC Bias Current Output. This pin sinks a DC bias current for the laser diode. The current sink is controlled by APC loop. In burst-mode, the current sink is turned-off during burst disable state.
LASERN	17	A, O	LD AC Modulation Current Negative Output. This pin switches modulation current depending on the TXIP and TXIN and the polarity can be controlled.
VSSX	18	G	LD AC Modulation Driver Circuit Ground 0V. This pin connects to the ground of the modulation current source and should have good decoupling to VDDT as well supply connecting to laser.
LASERP	19	A, O	LD AC Modulation Current Positive Output. This pin switches modulation current depending on the TXIP and TXIN and the polarity can be controlled.
MOD_SET	20	A	This pin is configured as modulation current.
MPD	21	A, I	Power Monitor Diode Input. This pin should connect to the power monitor diode of the laser.

NAME	PIN #	TYPE	DESCRIPTION
SD_SET	22	A	This pin is configured as signal detect level
RREF	23	A, I	Current Reference Setting Resistor. An external precision 10K Ohm resistor should be connected between this pin and VSSR. The resistor should be placed as close as possible to the device.
VSSR	24	G	Analog and Receive Path Circuits Ground 0V. This pin connects to circuit grounds of the reference and receive path. This pin should have good decoupling to VDDR. These are very sensitive circuit and thus should be isolated from transmit supply to avoid board-level crosstalk.
VDDR	25	P	Analog and Receive Path Circuits Supply 3.3V. An external very clean and noise free 3.3V should be connected to this pin. This pin connects to circuit grounds of the reference and receive path. This pin should have good decoupling to VDDR. These are very sensitive circuit and thus should be isolated from transmit supply to avoid board-level crosstalk.
RXINN	26	A, I	Post Amplifier Negative Input. This pin is typically connected to PIN-TIA through AC coupling. This pin is internally biased. The AC coupling capacitor and internally bias resistor (10K) set the 3dB low frequency.
RXINP	27	A, I	Post Amplifier Positive Input. This pin is typically connected to PIN-TIA through AC coupling. This pin is internally biased. The AC coupling capacitor and internally bias resistor (10K) set the 3dB low frequency.
VSSRO	28	G	Receive Output Buffer Ground 0V. This pin connects to circuit grounds of the receive output buffer. This pin should have good decoupling to VDDRO.

FUNCTIONAL DESCRIPTION

1. Post Amplifier Configuration

1.1 PA Signal Detect Level Setting

The signal detect (SD) level setting of post amplifier is completed by configuring PIN22 SD_SET input voltage which is also the output voltage of PIN5 CFIL ranging from 0V to1.8V. An appropriate input voltage value of SD_SET can be obtained through CFIL calibrating voltage value with resistors so that the right SD level setting is accomplished. The SD hysteresis level is fixed 1.8dB (10log). The adjusting area of input differential voltage regarding SD level ranges from 2mV to 160mV.

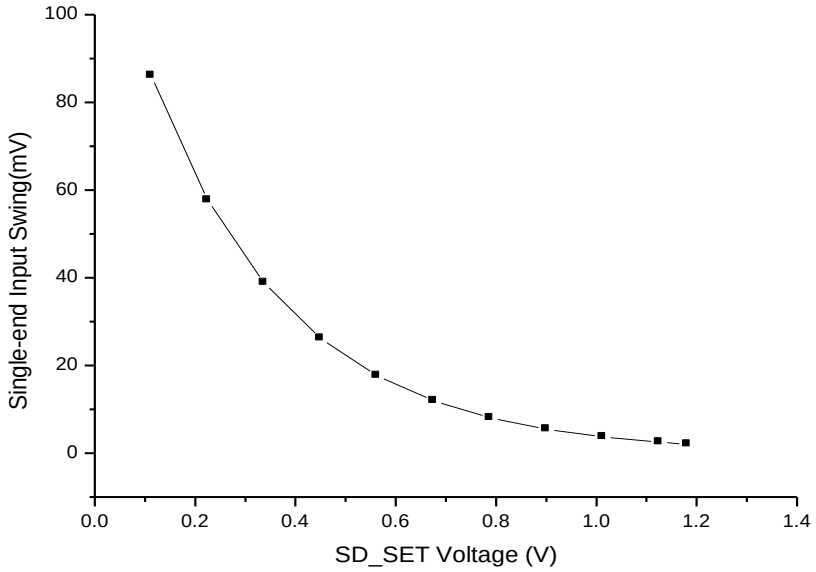


Figure 3 SD_SET Voltage versus Single-end Input Swing Voltage

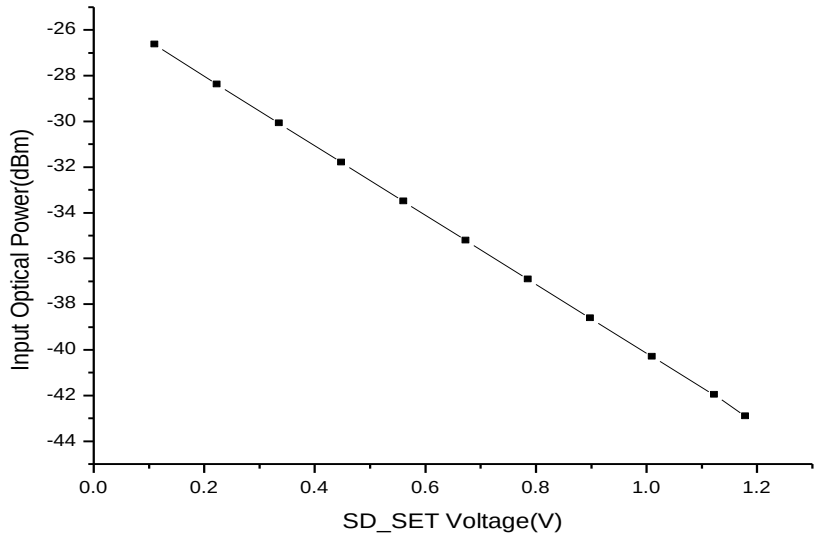


Figure 4 SD_SET Voltage versus Input Optical Power

1.2 SD Level Output Configuration

PIN4 is connected to detecting signal LOS/SD. CS6718's chip application environment is allowed to be chosen between SFP module and 1X9 module. In SFP module, PIN7 HSCL is connected to 3.3V, PIN4 outputs LOS signal by open drain level: 0 indicates input optic power is higher than threshold setting, 1 indicates input optic power is lower than threshold setting. In 1X9 module, PIN7 HSCL is connected to VSS, PIN4 outputs SD signal: 0 indicates input optic power is lower than threshold setting, 1 indicates input optic power is higher than threshold setting

In 1X9 module, PIN4 output way can be also configured by PIN8. When PIN8 is connected to VDD, SD output, needs to be extra loaded, can be PECL level. When PIN8 is connected to VSS, SD output can be CMOS level. While in SFP module, PIN8 is TX_FAULT output pin.

2. Laser Diode Driver Configuration

2.1 Modulation Current Configuration

PIN20 MOD_SET is used for modulation current setting of laser diode driver. Through configuring the input voltage of MOD_SET, the modulation current can be obtained from 0 to 80mA. The input voltage of MOD_SET is also PIN5 CFIL output voltage (V_{CFIL}) ranges from 0V to 1.8V. An appropriate input voltage value of MOD_SET can be obtained through CFIL calibrating voltage value with resistors .The relationship between MOD_SET input voltage (V_{MOD_SET}) and modulation current (I_{MOD}) is as follows:

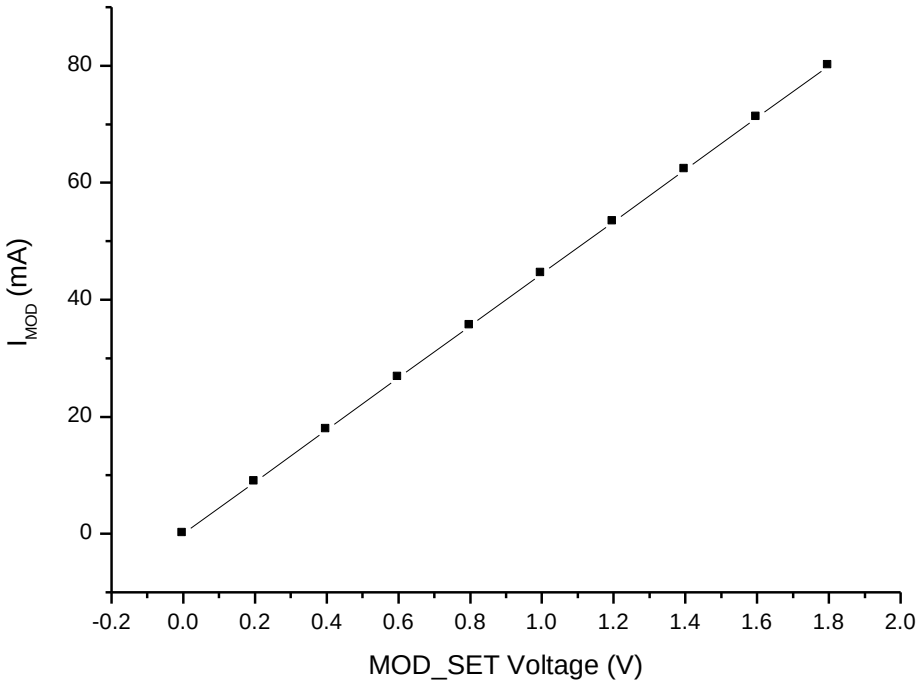


Figure 5 MOD_SET versus I_{MOD}

2.2 MPD Current Configuration

The desired output optic power can be obtained by automatic power control (APC) loop in the chip which can adjust bias current of Laser diode automatically. Before APC working, PIN MPD of TOSA should be connected to CS6718's PIN21 (MPD) with a pull down resistor Rmpd to VSS. When APC works, TOSA MPD output current can be changed by adjusting bias current to control laser diode optic power, in the mean time; PIN21's voltage is locked to 1.4V. On the other hand, the finally locked MPD current (I_{MPD}) can be controlled by choosing different value of pull down resistor R_{MPD}, the relationship is as follows:

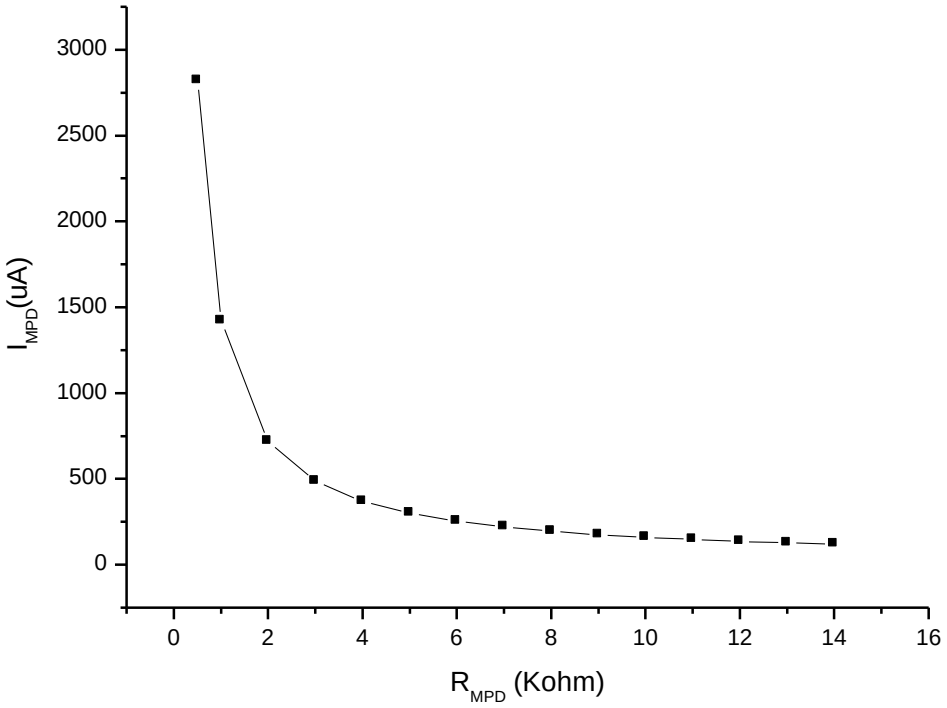


Figure 6 R_{MPD} versus I_{MPD}

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

SYMBOL	PARAMETER	RRATING	UNIT
VDD	Positive Power Supply	3.6	V
T_A	Ambient Operating Temperature	-40 to 85	°C
T_{STG}	Storage Temperature	-65 to 150	°C

Recommend Operating Condition

SYMBOL	PARAMETER	RRATING	UNIT
VDD	Positive Power Supply	3.0 to 3.6	V
T_A	Ambient Operating Temperature	-40 to 85	°C

DC/AC Electrical Characteristics VDD = 3.0V to 3.6V, TA = -40°C to 85°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTE
Power Supply Current						
IDD, VDDD	Supply Current for Core and Peripherals	-	12	16	mA	1
IDD, VDDR	Supply Current for Receive Path and Analog Circuit	-	15	20	mA	2
IDD, VDDRO	Supply Current for Receive Output Buffer	-	20	30	mA	3
IDD, VDDT	Supply Current for Transmit Path and Driver	-	12	16	mA	4
Digital IO Characteristics						
VOH	IOH = 1mA	VDD-0.5	-	VDD	V	
VOL	IOL = 4mA	0	-	0.5	V	
IIN	Input Current	-50	0	50	uA	
Internal 1.8V Regulator						
V_{DD18}	Internal 1.8V regulator output	1.6	1.8	2.0	V	5

Note 1. Measured through VDDD pin at 12.5MHz clock rate.
2. Measured through VDDR pin.
3. Measured through VDDRO pin including load current of two external 120 Ohm pull down resistors.
4. Measured though VDDT pin at 10Mbps rate. Does not include any load current.
5. Internal regulator output on CFIL pin. This regulator can be trimmed by register setting.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTE
Post Amplifier						
V, In	Input Sensitivity at 1.25Gbps	4	2	1	mV	
V, Out	Differential Output Swing	640	800	960	mV	RXOP/RXON
T, Rise/Fall	Output Rise/Fall Time	-	100	150	psec	
F, 3dB High	Bandwidth	800	950	1150	MHz	
F, 3dB Low	Low Cut-Off Frequency	-	50	100	KHz	
VIN, HYS	Hysteresis, Electrical	-	2.5	-	dB	
LD Driver						
V, In, Swing	Differential Input Swing	300	1200	2400	mV	TXINP/TXINN
V, In, V_{CM}	PECL Input Common Voltage	Vcc-1.4	Vcc-1.3	Vcc-1.2	V	TXINP/TXINN
I, DCB	DCB Bias Current Range	1	40	100	mA	
I, MOD	MOD Current Range	4	35	80	mA	
T, Rise/Fall	Output Rise/Fall Time	50	100	150	psec	Electrical
T, Ben	Burst Enable and Disable time	2	3	6	nsec	Electrical
V, Out	Minimum Output Voltage at DCB and LASERP, LASERN	0.8	1.0	-	V	
I, MPD	MPD Input Current Range	-	-	2.5	mA	
V, MPD	MPD Input Voltage	-	1.2	-	V	

APPLICATION DIAGRAM

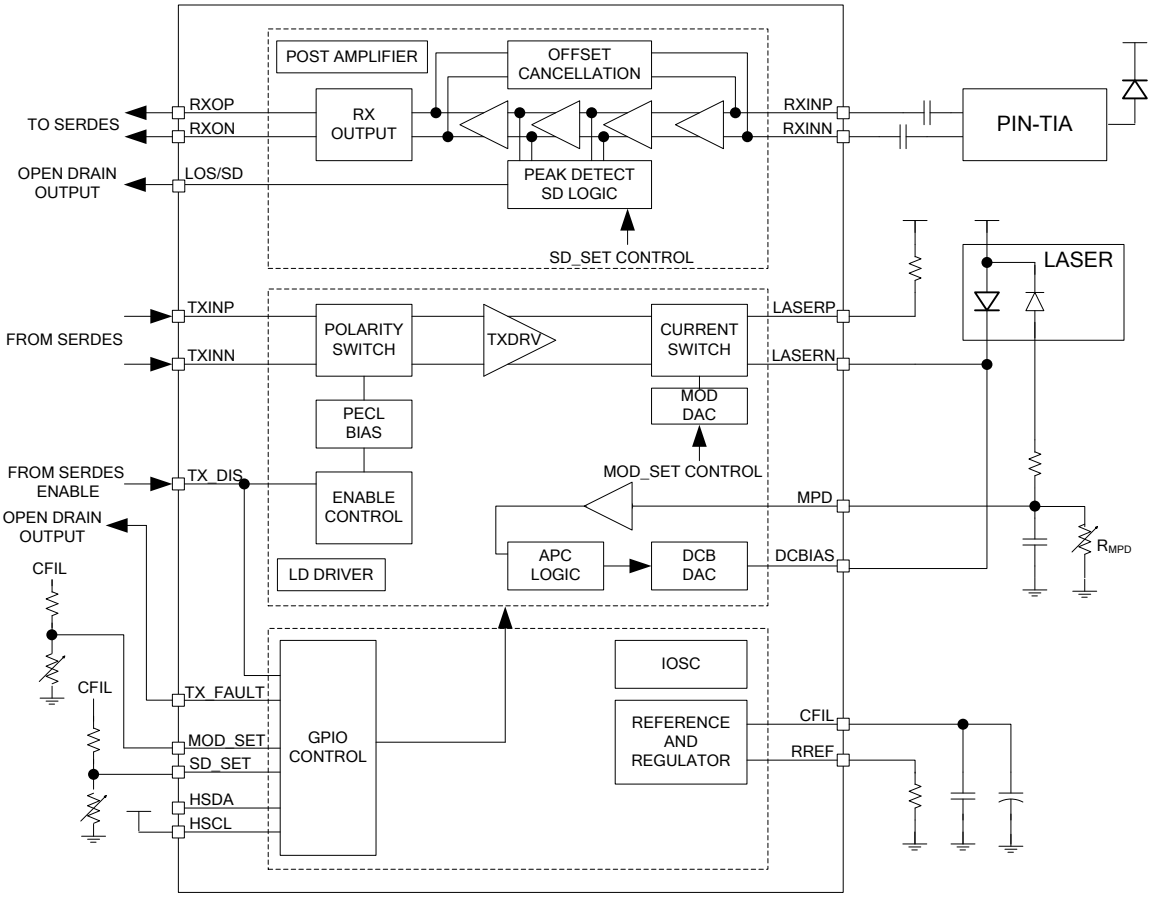


Figure 7 SFP Module Application Diagram

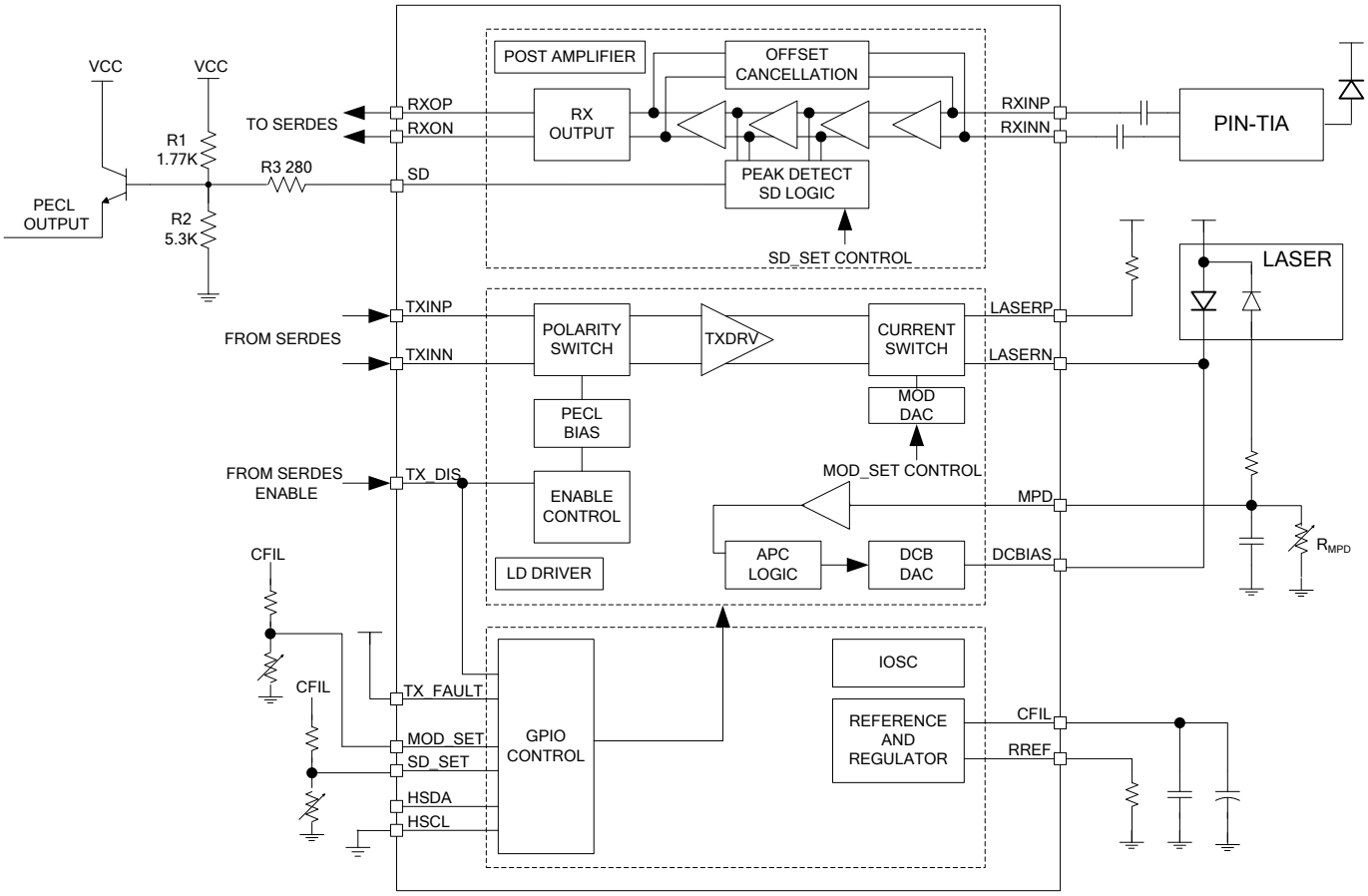


Figure 8 1*9 Module Application Diagram (SD PECL OUTPUT)

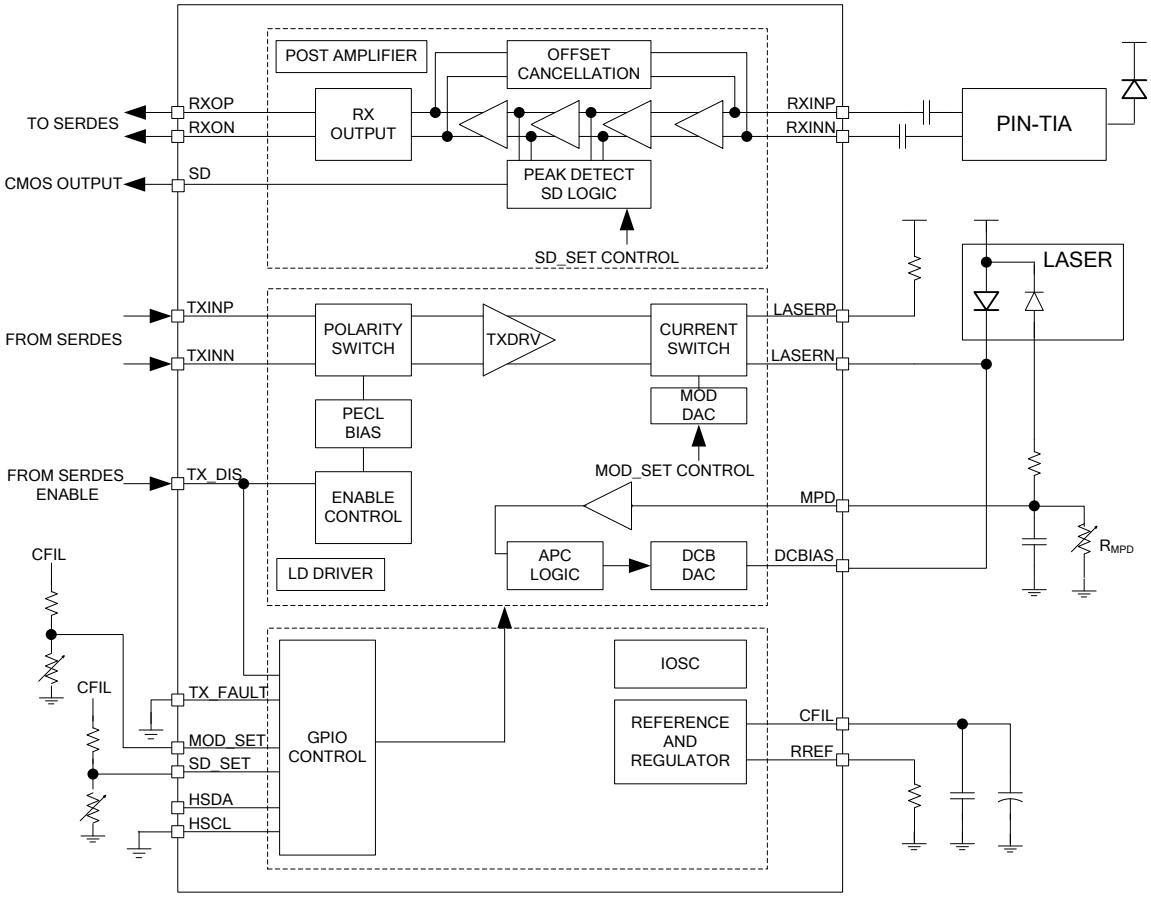
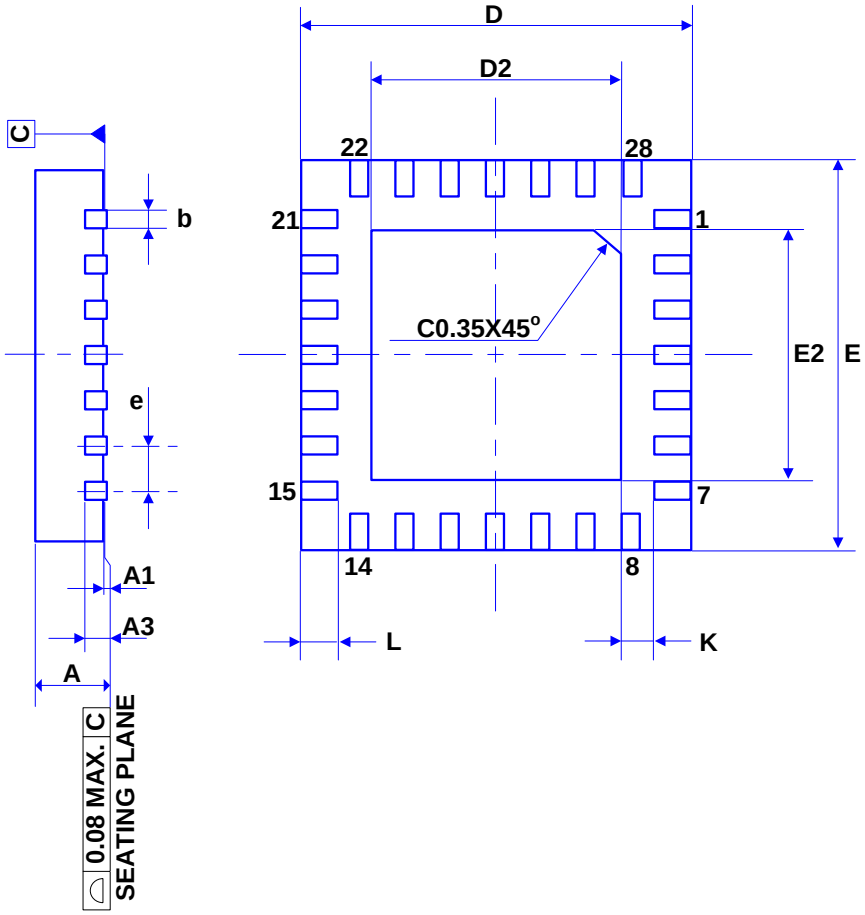


Figure 9 1*9 Module Application Diagram (SD CMOS OUTPUT)

PACKAGE OUTLINE: 28-pin QFN



Symbol	Dimensions in Millimeters		
	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.17	0.22	0.27
e		0.45 BSC	
D		4.00 BSC	
E		4.00 BSC	
L	0.35	0.40	0.45
K	0.20	-	-

	Dimensions in Millimeters					
	D2			E2		
EXPOSED PAD	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
114×114 MIL	2.30	2.40	2.45	2.30	2.40	2.45

Notes:

1. JEDEC Outline: N/A.
2. Dimension b applies to metal terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.
3. The minimum “K” value of 0.20mm applies.
4. Bilateral co-planarity zone applies to the exposed heat sink slug as well as the terminals.

ORDERING INFORMATION

Prefix	Part Number	Package Type
CS	6718	W: 28-pin QFN

Example: CS 6718 W

DISCLAIMER AND DECLARATION