FEDL6588-6588L-04
Issue Date: Jan. 25, 2002

OKI Semiconductor

MSM6588/6588L

ADPCM Solid-State Recorder (for Serial Registers)

GENERAL DESCRIPTION

The MSM6588/6588L is a "solid-state recorder" IC developed using the ADPCM method. By externally connecting a microphone, a speaker, a speaker amplifier and a serial register or other memory device to store ADPCM data, it can record and playback voice data like a tape recorder.
The MSM6588/6588L has a stand-alone mode and a microcontroller interface mode. In stand-alone mode, record or playback can be selected via a pin and it is possible to control the MSM6588 at a simple drive timing. In microcontroller interface mode, record/playback can be controlled by commands from the microcontroller, the MSM6588/6588L is much more flexible in microcontroller mode than in stand-alone mode. In addition, recording and playback with fixed message are easily implemented by connecting a serial voice ROM.
The MSM6588 and the MSM6588L support 5 V and 3 V operation respectively.

FEATURES

- 12-bit A/D converter
- 12-bit D/A converter
- Microphone amplifier
- Low-pass filter (LPF)
  Filter characteristics –40 dB/oct
- Serial registers
  MSM6588
  Up to four 1M bit serial registers (MSM6389C) can be driven directly
  One 512K bit serial register (MSM6587) can be driven directly
  One 256K bit serial register (MSM6586) can be driven directly
  MSM6588L
  Up to four 1M bit serial registers (MSM63V89C) can be driven directly
- Serial Voice ROMs
  1M bit serial voice ROM (MSM6595A-xxx)
  2M bit serial voice ROM (MSM6596A-xxx)
  3M bit serial voice ROM (MSM6597A-xxx)
- Maximum recording time
  262 seconds (when using 3-bit ADPCM, 5.3 kHz sampling)
- Voice triggered starting
- Pause function
- Master clock frequency: 4.096 to 8.192 MHz
- Power supply voltage
  MSM6588: Single 5 V Power supply
  MSM6588L: Single 3 V Power supply
- Package options:

44-pin plastic QFP	(QFP44-P-910-0.80-2K)	(MSM6588GS-2K)
44-pin plastic QFP	(QFP44-P-910-0.80-2K)	(MSM6588LGS-2K)
44-pin plastic TQFP	(TQFP44-P-1010-0.80-K)	(MSM6588LTB)

• Differences between MSM6588 and MSM6588L

The major differences between the MSM6588 and the MSM6588L are shown below.

Parameter	MSM6588	MSM6588L
Operating voltage	3.5 to 5.5 V	2.7 to 3.6 V
Full scale of A/D and D/A converters	0 to V_{DD}	$\frac{1}{4}$ V_{DD} to $\frac{3}{4}$ V_{DD}
Voice detection level for voice triggered starting	$\pm\frac{V_{DD}}{64}$, $\pm\frac{V_{DD}}{32}$, $\pm\frac{V_{DD}}{16}$	$\pm\frac{V_{DD}}{128}$, $\pm\frac{V_{DD}}{64}$, $\pm\frac{V_{DD}}{32}$
External only register	1M bits (MSM6389C) 512K bits (MSM6587) 256K bits (MSM6586)	1M bits (MSM63V89C)

1. Characteristics in stand-alone mode

• 3-bit ADPCM
• Sampling frequency:
  5.3 kHz or 8.0 kHz (when the oscillator operates at 4.096 MHz)
  10.6 kHz or 16.0 kHz (when the oscillator operates at 8.192 MHz)
• Number of phrases: 1, 2, 4 or 8

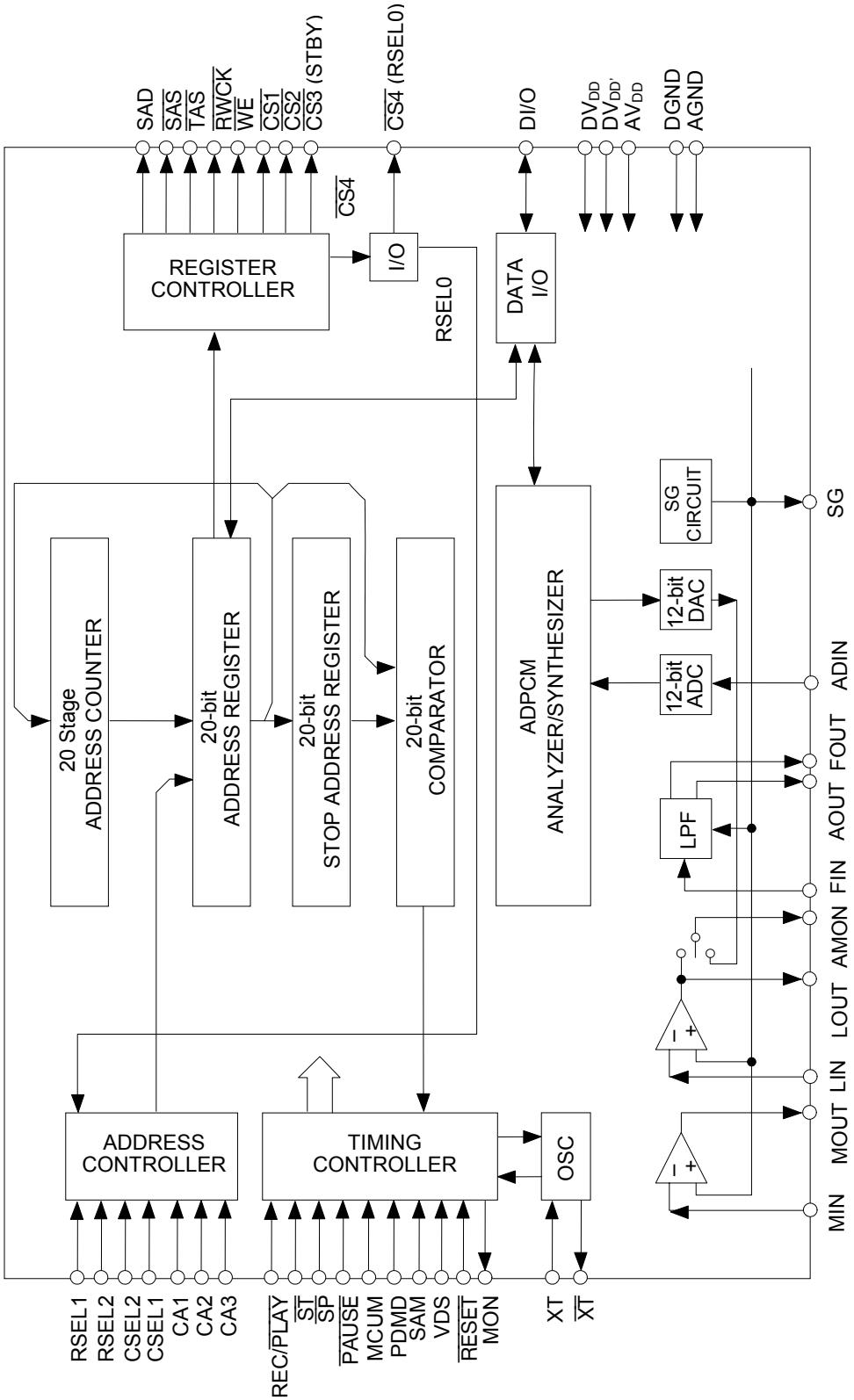
2. Characteristics in microcontroller interface mode

• 3-bit/4-bit ADPCM selectable
• Sampling frequency:
  4.0 kHz, 5.3 kHz, 6.4 kHz or 8.0 kHz (when the oscillator operates at 4.096 MHz)
  8.0 kHz, 10.6 kHz, 12.8 kHz or 16.0 kHz (when the oscillator operates at 8.192 MHz)
• Condition setting, start, and stop of record/playback controllable by 13 commands.

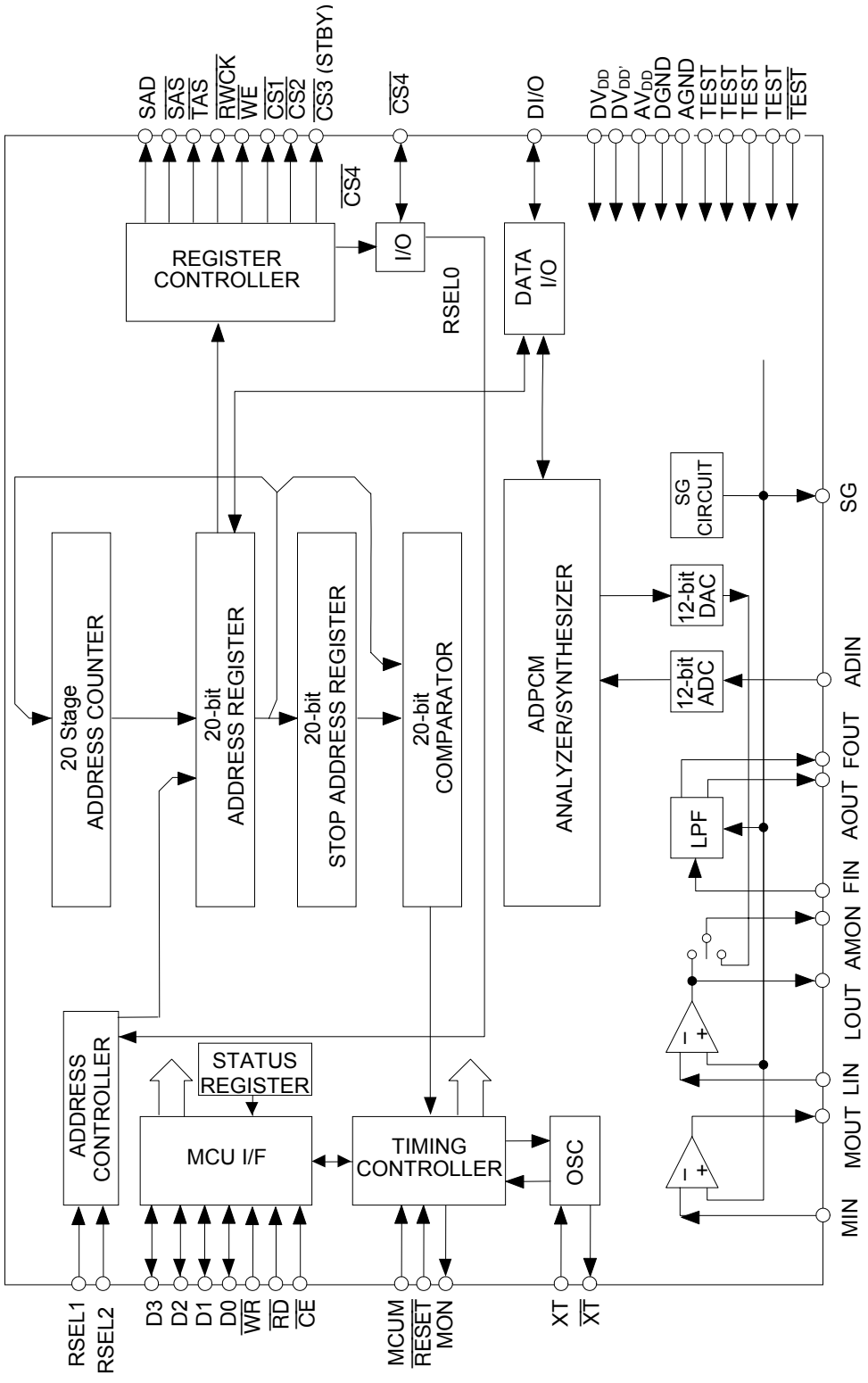
CONTENTS

BLOCK DIAGRAM

Stand-Alone Mode

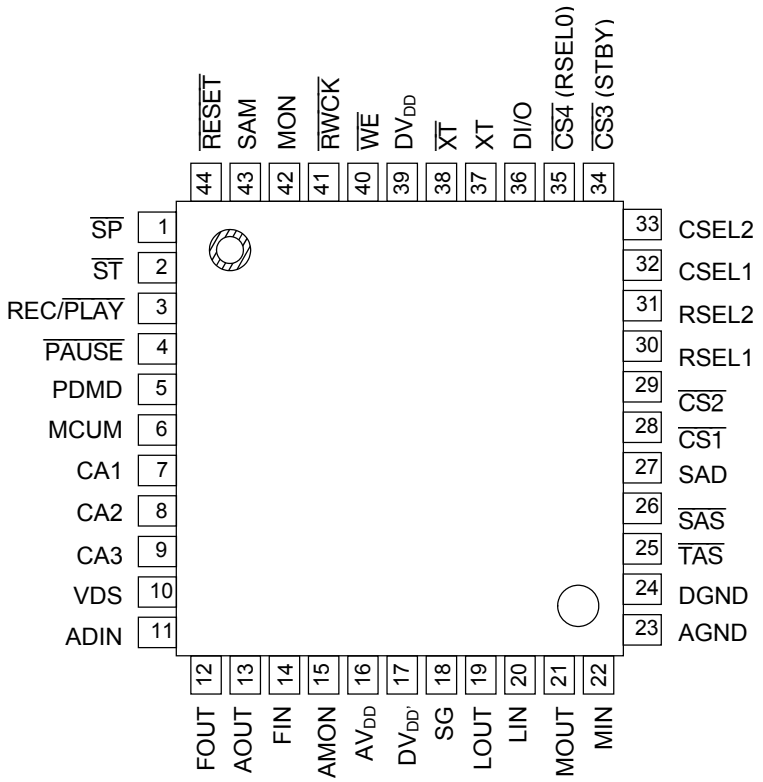


Microcontroller Interface Mode



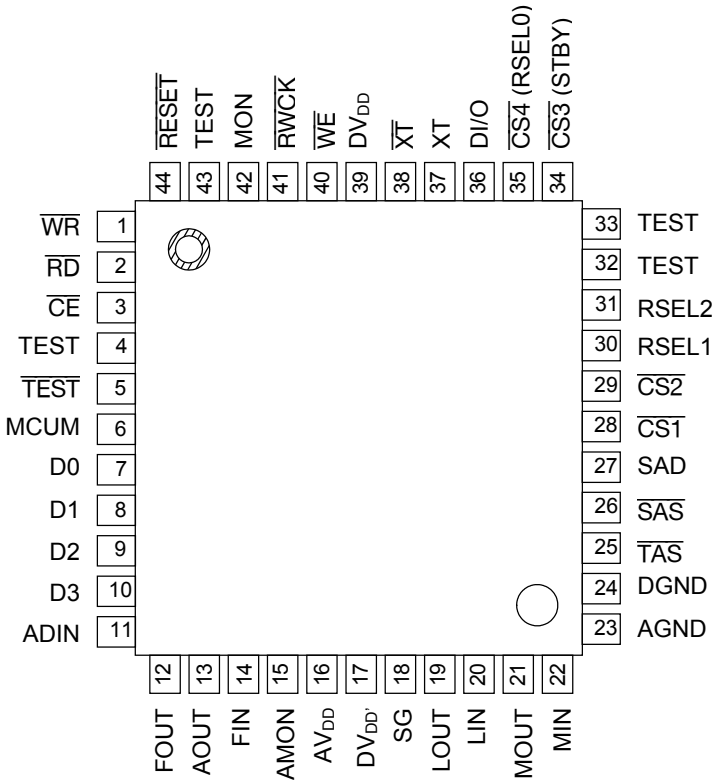
PIN CONFIGURATION (TOP VIEW)

1. Stand-alone mode (MCUM pin = "L")



44-Pin Plastic QFP
44-Pin Plastic TQFP

2. Microcontroller interface mode (MCUM pin = "H")



44-Pin Plastic QFP
44-Pin Plastic TQFP

Selection of stand-alone mode or microcontroller interface mode is controlled by the level of the MCUM pin.
MCUM = "H": microcontroller interface mode
MCUM = "L": stand-alone mode

PIN DESCRIPTIONS

Common Functions in Stand-Alone Mode and Microcontroller Interface Mode

Pin	Symbol	Type	Description
39	DV_{DD}	—	Digital power supply pin. Insert a bypass capacitor of 0.1 μF or more between this pin and the DGND pin.
17	$DV_{DD'}$	—	Digital power supply pin
16	AV_{DD}	—	Analog power supply pin. Insert a bypass capacitor of 0.1 μF or more between this pin and the AGND pin.
24	DGND	—	Digital GND pin
23	AGND	—	Analog GND pin
18	SG	O	Output pin for analog circuit reference voltage (signal ground)
22 20	MIN LIN	I	Inverting input pin for the built-in OP amplifier. Non-inverting input pin is connected to SG internally.
21 19	MOUT LOUT	O	MOUT and LOUT are output pins of the built-in OP amplifier for MIN and LIN, respectively.
15	AMON	O	This pin is connected to the LOUT pin in recording mode and to the DA converter output in playing mode. Connected to the built-in LPF input (FIN pin).
14	FIN	I	Input pin for the built-in LPF
12	FOUT	O	Output pin of the built-in LPF. Connected to the AD converter (ADIN pin) input.
11	ADIN	I	Input pin for the built-in 12-bit AD converter
13	AOUT	O	Output pin for the built-in LPF. Output pin for playback waveform. Connected to the speaker drive amplifier.
27	SAD	O	(Serial Address Data) Connected to the SAD pin of serial register. This pin outputs the Read/Write header address.
26	$\overline{SAS}$	O	(Serial Address Strobe) Connected to the $\overline{SAS}$ pin of serial register. Clock pin to write the serial address.
25	$\overline{TAS}$	O	(Transfer Address Strobe) Connected to the $\overline{TAS}$ pin of serial register. Clock pin which transfers the serial address data to the address counter inside the serial register.

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>41</td><td>$\overline{\text{RWCK}}$</td><td>O</td><td>(Read/Write Clock) Connected to the $\overline{\text{RWCK}}$ pin of the serial register.
Clock pin for reading and writing data to the serial registers.</td></tr>
<tr><td>40</td><td>$\overline{\text{WE}}$</td><td>O</td><td>(Write Enable) Connected to the $\overline{\text{WE}}$ pin of serial register. The pin to select read or write mode.</td></tr>
<tr><td>36</td><td>DI/O</td><td>I/O</td><td>(Data I/O) Connected to the DIN and DOUT pins of serial register.
Data input and output mode.</td></tr>
<tr><td>28
29
34
35</td><td>$\overline{\text{CS1}}$
$\overline{\text{CS2}}$
$\overline{\text{CS3}}$ (STBY)
$\overline{\text{CS4}}$ (RSEL0)</td><td>O
O
O
I/O</td><td>(Chip Select) Connected to the $\overline{\text{CS}}$ pin of the serial register.
$\overline{\text{CS3}}$ pin and $\overline{\text{CS4}}$ pin have different functions depending on the number of serial registers to be connected. The number of serial registers is selected by the RSELI and RSEL2 pins.
$\overline{\text{CS3}}$ (STBY) pin becomes $\overline{\text{CS3}}$ when four serial registers are used, otherwise it is the STBY pin which outputs a “H” level at power down.
$\overline{\text{CS4}}$ (RSEL0) pin becomes $\overline{\text{CS4}}$ when four serial registers are used, otherwise it is the RSEL0-pin used to select the number of serial registers used.
<table>
<tr><td>RSEL2</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>RSEL1</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>$\overline{\text{CS3}}$ (STBY)</td><td>STBY</td><td>STBY</td><td>STBY</td><td>$\overline{\text{CS3}}$</td></tr>
<tr><td>$\overline{\text{CS4}}$ (RSEL0)</td><td>RSEL0
(I)</td><td>RSEL0
(I)</td><td>RSEL0
(I)</td><td>$\overline{\text{CS4}}$
(O)</td></tr>
</table></td></tr>
<tr><td>35
30
31</td><td>$\overline{\text{CS4}}$ (RSEL0)
RSEL1
RSEL2</td><td>I/O
I
I</td><td>(Register Select) Those pins are to select the number of serial registers to be connected.
<table>
<tr><td>RSEL2</td><td colspan="2">L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>RSEL1</td><td colspan="2">L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>RSEL0
($\overline{\text{CS4}}$)</td><td>L
(I)</td><td>L
(I)</td><td>—
(I)</td><td>—
(I)</td><td>$\overline{\text{CS4}}$
(O)</td></tr>
<tr><td>Number of serial voice registers</td><td>One
256K bit</td><td>One
512K bit</td><td>One
1M bit</td><td>Two
1M bit</td><td>Four
1M bit</td></tr>
</table></td></tr>
<tr><td>6</td><td>MCUM</td><td>I</td><td>This pin is to select stand-alone mode or microcontroller interface mode.
“L” level ---- stand-alone mode
“H” level ---- microcontroller interface mode</td></tr>
<tr><td>44</td><td>$\overline{\text{RESET}}$</td><td>I</td><td>The IC is initialized and goes into the power-down state by input of a “L” level.</td></tr>
<tr><td>37</td><td>XT</td><td>I</td><td>Connect to an oscillator. Use this input when providing an external clock. When at power down input the GND level instead.</td></tr>
<tr><td>38</td><td>$\overline{\text{XT}}$</td><td>O</td><td>Connect to an oscillator. Leave open when using an external clock.</td></tr>
</table>

Stand-Alone Mode

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>3</td><td>REC/$\overline{\text{PLAY}}$</td><td>I</td><td>This pin is to select recording or playback.
When a “H” level is input, the IC is in record mode.</td></tr>
<tr><td>2</td><td>$\overline{\text{ST}}$</td><td>I</td><td>When a “L” level pulse is input, record/playback is started.
Internal pull up connected</td></tr>
<tr><td>1</td><td>$\overline{\text{SP}}$</td><td>I</td><td>When a “L” level pulse is input, record/playback is ended.
Internal pull up connected.</td></tr>
<tr><td>4</td><td>$\overline{\text{PAUSE}}$</td><td>I</td><td>When a “L” level pulse is input, record/playback is suspended.
Internal pull up connected.</td></tr>
<tr><td>32
33</td><td>CSEL1
CSEL2</td><td>I</td><td>These pins are to select the number of recorded words and control mode. When the number of the recorded words is wished to be selected in one word, select Flex mode.
<table>
<tr><td>CSEL2</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>CSEL1</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>Number of recorded word</td><td>8</td><td>4</td><td>2</td><td>8</td></tr>
<tr><td>Control mode</td><td colspan="3">fixed</td><td>flex</td></tr>
</table></td></tr>
<tr><td>7
8
9</td><td>CA1
CA2
CA3</td><td>I</td><td>These pins are to specify the channel.
(Refer to Explanation of Functions.)</td></tr>
<tr><td>43</td><td>SAM</td><td>I</td><td>This pin is to select the sampling frequency.
The following is the relation between the master clock frequency (f_{OSC}) and sampling frequency (f_{samp}).
Numbers inside the parentheses ( ) are for f_{OSC} = 4.096 MHz
<table>
<tr><td>SAM</td><td>L</td><td>H</td></tr>
<tr><td>f_{samp}</td><td>$\frac{f_{OSC}}{768}$
(5.3 kHz)</td><td>$\frac{f_{OSC}}{512}$
(8.0 kHz)</td></tr>
</table></td></tr>
<tr><td>5</td><td>PDMD</td><td>I</td><td>This pin selects transition to the power down state.
“L” level ---- The IC enters power down state automatically except during record/playback.
“H” level ---- The IC enters standby state except during record/playback. The power down state can be entered by the $\overline{\text{RESET}}$ pin. This mode must be active when using the built-in LPF in an external circuit.</td></tr>
<tr><td>10</td><td>VDS</td><td>I</td><td>This pin is to select voice triggered starting that starts recording when the voice input exceeds the preset amplitude. Input a “H” level and the voice activation circuit is enabled. Input a “L” level to disable the voice activation circuit.</td></tr>
<tr><td>42</td><td>MON</td><td>O</td><td>Outputs a “H” level during record/playback.</td></tr>
</table>

Microcontroller Interface Mode

Pin	Symbol	Type	Description
7 8 9 10	D0 D1 D2 D3	I/O	Bi-directional data bus. Performs input/output of commands and data with an external microcontroller.
1	$\overline{WR}$	I	This pin is to input WRITE pulses. Input is a “L” pulse when commands or data to the D0 to D3 pins are to be input.
2	$\overline{RD}$	I	This pin is to input READ pulses. Input is a “L” pulse when output status or data from the D0 to D3 pins is to read.
3	$\overline{CE}$	I	Chip enable. A“H” level on this pin disables WRITE (WR)/READ ($\overline{RD}$) input pulses. Input/output of data through the D0 to D3 pins is disabled.
42	MON	O	Outputs a “H” level during record/playback. When record/playback is in operation using the EXT command, clocks for synchronization are output.
4, 32, 33, 43 5	TEST $\overline{TEST}$	I	These pins are for IC testing at the factory. Input a “L” level to the TEST pin and a “H” level to the $\overline{TEST}$ pin.

ABSOLUTE MAXIMUM RATINGS (for MSM6588 (5 V Version))

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta = 25°C	–0.3 to +7.0	V
Input voltage	V_{IN}		–0.3 to V_{DD} +0.3	V
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (for MSM6588 (5 V Version))

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD}	DGND = AGND = 0 V	3.5 to 5.5 (Note 5)	V
Operating temperature	T_{OP}	—	–40 to +85	°C
Master clock frequency	f_{OSC}	—	4.0 to 8.192	MHz

ELECTRICAL CHARACTERISTICS (for MSM6588 (5 V Version))

DC Characteristics

$DV_{DD} = DV_{DD'} = AV_{DD}$ = 4.5 to 5.5 V (Note 5), DGND = AGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	$0.8 \times V_{DD}$	—	—	V
"L" input voltage	V_{IL}	—	—	—	$0.2 \times V_{DD}$	V
"H" output voltage	V_{OH}	I_{OH} = –40 µA	V_{DD} –0.3	—	—	V
"L" output voltage	V_{OL}	I_{OL} = 2 mA	—	—	0.45	V
"H" input current (Note 1)	I_{IH1}	$V_{IH} = V_{DD}$	—	—	10	µA
"H" input current (Note 2)	I_{IH2}	$V_{IH} = V_{DD}$	—	—	20	µA
"L" input current (Note 3)	I_{IL1}	V_{IL} = GND	–10	—	—	µA
"L" input current (Note 2)	I_{IL2}	V_{IL} = GND	–20	—	—	µA
"L" input current (Note 4)	I_{IL3}	V_{IL} = GND	–400	—	–20	µA
Operating current consumption	I_{DD}	f_{OSC} = 8 MHz, no load	—	7	15	mA
Standby current Consumption	I_{DDS}	When power down, no load Ta = –40 to +70°C	—	—	10	µA
		When power down, no load Ta = –40 to +85°C	—	—	50	µA

Notes: 1. Applicable to all input pins, excluding the XT pin.
2. Applicable to the XT pin.
3. Applicable to all input pins without pull-up resistors, excluding the XT pin.
4. Applicable to input pins ($\overline{ST}$, $\overline{SP}$, $\overline{PAUSE}$) with pull-up resistors, excluding the XT pin.
5. Recording and playback should be performed at a power supply voltage of 4.5 to 5.5 V. For other operations such as backing up a serial register, the IC operates at 3.5 to 5.5 V.

Analog Characteristics

DV_{DD} = $DV_{DD'}$ = AV_{DD} = 4.5 to 5.5 V, DGND = AGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DA output relative error	$\|V_{DAE}\|$	no load	—	—	10	mV
FIN admissible input voltage range	V_{FIN}	—	1	—	V_{DD}–1	V
FIN input impedance	R_{FIN}	—	1	—	—	MΩ
ADIN admissible input voltage range	V_{ADIN}	—	0	—	V_{DD}	V
ADIN input impedance	R_{ADIN}	—	1	—	—	MΩ
Op-amp open loop gain	G_{OP}	f_{IN} = 0 to 4 kHz	40	—	—	dB
Op-amp input impedance	R_{INA}	—	1	—	—	MΩ
Op-amp load resistance	R_{OUTA}	—	200	—	—	kΩ
AOUT load resistance	R_{AOUT}	—	50	—	—	kΩ
FOUT load resistance	R_{FOUT}	—	50	—	—	kΩ

AC Characteristics

1. Common characteristics in stand-alone mode and microcontroller interface mode

DV_{DD} = $DV_{DD'}$ = AV_{DD} = 4.5 to 5.5 V, DGND = AGND = 0 V, Ta = –40 to +85°C

When f_{samp} = 8 kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
$\overline{\text{RESET}}$ pulse width		t_{RST}	1	—	—	μs
$\overline{\text{RESET}}$ execution time (Note 1)	*	t_{REX}	—	125	—	μs

Item with * is proportional to the period of sampling frequency (f_{samp}).

Note: 1. The oscillation stable time is added to t_{REX}.
The oscillation stable time is several tens of milliseconds for crystal oscillators and is several hundreds of microseconds.

2. Stand-alone mode

The AC characteristics values of stand-alone mode are proportional to the period of the sampling frequency (f_{samp}).

DV_{DD} = $DV_{DD'}$ = AV_{DD} = 4.5 to 5.5 V, DGND = AGND = 0 V, Ta = –40 to +85°C
When f_{samp} = 8 kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
$\overline{ST}$ pulse width (Note 1)		t_{ST}	40	—	—	µs
$\overline{SP}$ pulse width		t_{SP}	40	—	—	µs
$\overline{PAUSE}$ pulse width		t_{PSE}	40	—	—	µs
Hold time of CA1, CA2, CA3, REC/$\overline{PLAY}$ for MON rise		t_{CAH}	1	—	—	ms
Address control time at the start of record/playback		t_{AD1}	—	1	—	ms
Address control time at the end of recording		t_{AD2}	—	1	—	ms
Time until the release of recording standby after input of $\overline{SP}$ pulse during voice standby		t_{SPV}	—	—	500	µs
Silence during repeated playback		t_{MID}	—	1.5	—	ms
Time from input of $\overline{PAUSE}$ pulse until pause		t_{PP}	—	—	250	µs
Time from input of $\overline{ST}$ pulse to the continuation of record/playback during pause		t_{PSP}	—	—	500	µs
PDMD = "L"	Oscillator stable time after input of $\overline{ST}$ pulse	t_{ANA}	—	32	—	ms
	$\overline{SP}$ pulse (during recording) to the fall of MON	t_{SPM1}	—	—	1	ms
	$\overline{SP}$ pulse (during playback) to the fall of MON	t_{SPM2}	—	—	260	ms
	Standby transient time at start of playback	t_{AOR}	—	64	—	ms
	Standby transient time at end of playback	t_{AOF}	—	256	—	ms
	Time from fall of MON to power down state at the end of playback	t_{MS}	—	70	—	µs
	$\overline{SP}$ pulse during pause to record end	t_{PSP1}	—	—	1	ms
	$\overline{SP}$ pulse during pause to playback end	t_{PSP2}	—	—	260	ms
PDMD = "H"	$\overline{ST}$ pulse to MON rise	t_{STM}	—	—	1	ms
	$\overline{SP}$ pulse to MON fall	t_{SPM1}	—	—	1	ms
	$\overline{ST}$ pulse to voice standby state	t_{STV}	—	—	1	ms
	$\overline{SP}$ pulse during pause to record/playback end	t_{PSP1}	—	—	1	ms

Note: 1. When the PDMD pin is "L", the oscillation stable time is added to t_{ST}. The oscillation stable time is several tens of milliseconds for crystal oscillators and is several hundreds of microseconds for ceramic oscillators.

3. Microcontroller interface mode

$DV_{DD} = DV_{DD'} = AV_{DD}$ = 4.5 to 5.5 V, DGND = AGND = 0 V, Ta = –40 to +85°C
When f_{samp} = 8 kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
$\overline{RD}$ pulse width		t_{RR}	200	—	—	ns
Setup and hold time of $\overline{CE}$ for $\overline{RD}$		t_{CR}	0	—	—	ns
Data valid from fall of $\overline{RD}$		t_{DRE}	—	—	200	ns
Data Hi-Z from rise of $\overline{RD}$		t_{DRF}	—	10	50	ns
$\overline{WR}$ pulse width		t_{WW}	200	—	—	ns
Setup and hold time of $\overline{CE}$ from $\overline{WR}$		t_{CW}	0	—	—	ns
Data setup time to rise of $\overline{WR}$		t_{DWS}	100	—	—	ns
Data Hold time from rise of $\overline{WR}$		t_{DWH}	30	—	—	ns
Disable time for $\overline{RD}$ and WR		t_{DRW}	250	—	—	ns
BUSY time after release of $\overline{RESET}$ (Note 1)	*	t_{BR}	—	—	125	µs
BUSY time after input of 1 nibble command	*	t_{B1}	—	—	16	µs
BUSY time after input of 2 nibble command	*	t_{B2}	—	—	16	µs
BUSY time after input of 2 nibble command data	*	t_{BD}	—	—	16	µs
BUSY time after input of ADRWR command	*	t_{BAW}	—	—	270	µs
BUSY time after input address data of ADRWR command	*	t_{BAD}	—	—	50	µs
Data input time after input of ADRRD command	*	t_{WAR}	270	—	—	µs
Time between output of address data nibbles during ADRRD command	*	t_{WDR}	50	—	—	µs

Items with * are proportional to the period of sampling frequency (f_{samp}).

Note: 1. The oscillation stable time is added to t_{BR}.
The oscillation stable time is several tens of milliseconds for crystal oscillators and is several hundred of microseconds for ceramic oscillators.

Parameter			Symbol	Min.	Typ.	Max.	Unit
Address control time at start of record/playback		*	t_{AD1}	—	1	—	ms
Address control time at end of recording		*	t_{AD2}	—	1	—	ms
START command to rise of MON		*	t_{STCM}	—	—	1	ms
STOP command to fall of MON		*	t_{SPCM}	—	—	1	ms
START command to RPM bit set (“H” level)		*	t_{STCR}	—	—	16	µs
START command (during voice triggered starting) to VPM bit set (“H” level)		*	t_{STCV}	—	—	16	µs
STOP command to release of voice standby (during voice triggered starting)		*	t_{SPCV}	—	—	500	µs
PAUSE command to VPM bit set (“H” level)		*	t_{PSCP}	—	—	16	µs
START command (during pause) to VPM bit reset (“L” level)		*	t_{STCP}	—	—	500	µs
STOP command (during pause) to VPM bit reset (“L” level)		*	t_{SPCP}	—	—	500	µs
When DTRW command is being executed	Delay time after input of DTRW command	*	t_{WRW}	16	—	—	µs
	Delay time after input of lower 4-bit of X address	*	t_{WXA1}	16	—	—	µs
	Delay time after input of middle 4-bit of X address	*	t_{WXA2}	16	—	—	µs
	Delay time after input of upper 4-bit of X address	*	t_{WXA3}	270	—	—	µs
	Delay time after input of REC command	*	t_{WRC}	16	—	—	µs
	Delay time after input of write data	*	t_{WWD}	50	—	—	µs
	Delay time after input of PLAY command	*	t_{WPL}	50	—	—	µs
	Delay time after input of STOP command	*	t_{WSP}	16	—	—	µs
When executing EXT command	EXT command to rise of MON	*	t_{EM}	125	—	330	µs
	“H” level time of MON	*	t_{MH}	—	31	—	µs
	“L” level time of MON	*	t_{ML}	—	94	—	µs
	MON rise to $\overline{RD}$ pulse rise (during recording)	*	t_{ERD}	—	—	120	µs
	MON rise to $\overline{WR}$ pulse rise (during playback)	*	t_{EWR}	—	—	120	µs
	ADPCM data write pulse to input of STOP command	*	t_{WE1}	16	—	—	µs
	STOP command until rise of MON	*	t_{ESP}	—	—	100	µs
	STOP command to record/playback end	*	t_{WEX}	—	—	250	µs

Items with * are proportional to the period of sampling frequency (f_{samp}).

ABSOLUTE MAXIMUM RATINGS (for MSM6588L (3 V Version))

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta = 25°C	–0.3 to +7.0	V
Input voltage	V_{IN}		–0.3 to V_{DD}+0.3	V
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (for MSM6588L (3 V Version))

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD}	DGND = AGND = 0 V	2.7 to 3.6	V
Operating temperature	T_{OP}	—	–40 to +85	°C
Master clock frequency	f_{OSC}	—	4.0 to 8.192	MHz

ELECTRICAL CHARACTERISTICS (for MSM6588L (3 V Version))

DC Characteristics

DV_{DD} = $DV_{DD'}$ = AV_{DD} = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	$0.85 \times V_{DD}$	—	—	V
"L" input voltage	V_{IL}	—	—	—	$0.15 \times V_{DD}$	V
"H" output voltage	V_{OH}	I_{OH} = –40 µA	V_{DD}–0.3	—	—	V
"L" output voltage	V_{OL}	I_{OL} = 2 mA	—	—	0.45	V
"H" input current (Note 1)	I_{IH1}	$V_{IH} = V_{DD}$	—	—	10	µA
"H" input current (Note 2)	I_{IH2}	$V_{IH} = V_{DD}$	—	—	20	µA
"L" input current (Note 3)	I_{IL1}	V_{IL} = GND	–10	—	—	µA
"L" input current (Note 2)	I_{IL2}	V_{IL} = GND	–20	—	—	µA
"L" input current (Note 4)	I_{IL3}	V_{IL} = GND	–400	—	–10	µA
Operating current consumption	I_{DD}	f_{OSC} = 8 MHz, no load	—	7	15	mA
Standby current consumption	I_{DDS}	When power down, no load Ta = –40 to +70°C	—	—	15	µA
		When power down, no load Ta = –40 to +85°C	—	—	100	µA

Notes: 1. Applicable to all input pins, excluding the XT pin.
2. Applicable to the XT pin.
3. Applicable to all input pins without pull-up resistors, excluding the XT pin.
4. Applicable to input pins ($\overline{ST}$, $\overline{SP}$, $\overline{PAUSE}$) with pull-up resistors, excluding the XT pin.

Analog Characteristics

DV_{DD} = $DV_{DD'}$ = AV_{DD} = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DA output relative error	$\|V_{DAE}\|$	no load	—	—	5	mV
FIN admissible input voltage range	V_{FIN}	—	$1/4 \times V_{DD}$	—	$3/4 \times V_{DD}$	V
FIN input impedance	R_{FIN}	—	1	—	—	MΩ
ADIN admissible input voltage range	V_{ADIN}	—	$1/4 \times V_{DD}$	—	$3/4 \times V_{DD}$	V
ADIN input impedance	R_{ADIN}	—	1	—	—	MΩ
Op-amp open loop gain	G_{OP}	f_{IN} = 0 to 4 kHz	40	—	—	dB
Op-amp input impedance	R_{INA}	—	1	—	—	MΩ
Op-amp load resistance	R_{OUTA}	—	200	—	—	kΩ
AOUT load resistance	R_{AOUT}	—	50	—	—	kΩ
FOUT load resistance	R_{FOUT}	—	50	—	—	kΩ

AC Characteristics

1. Common characteristics in stand-alone mode and microcontroller interface mode

DV_{DD} = $DV_{DD'}$ = AV_{DD} = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = –40 to +85°C

When f_{samp} = 8 kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
$\overline{\text{RESET}}$ pulse width		t_{RST}	1	—	—	μs
$\overline{\text{RESET}}$ execution time (Note 1)	*	t_{REX}	—	125	—	μs

Item with * is proportional to the period of sampling frequency (f_{samp}).

Note: 1. The oscillation stable time is added to t_{REX}.
The oscillation stable time is several tens of milliseconds for crystal oscillators and is several hundreds of microseconds.

2. Stand-alone mode

The AC characteristics values of stand-alone mode are proportional to the period of the sampling frequency (f_{samp}).

$DV_{DD} = DV_{DD'} = AV_{DD}$ = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = –40 to +85°C
When f_{samp} = 8 kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
$\overline{ST}$ pulse width (Note 1)		t_{ST}	40	—	—	µs
$\overline{SP}$ pulse width		t_{SP}	40	—	—	µs
$\overline{PAUSE}$ pulse width		t_{PSE}	40	—	—	µs
Hold time of CA1, CA2, CA3, REC/$\overline{PLAY}$ for MON rise		t_{CAH}	1	—	—	ms
Address control time at the start of record/playback		t_{AD1}	—	1	—	ms
Address control time at the end of recording		t_{AD2}	—	1	—	ms
Time until the release of recording standby after input of $\overline{SP}$ pulse during voice standby		t_{SPV}	—	—	500	µs
Silence during repeated playback		t_{MID}	—	1.5	—	ms
Time from input of $\overline{PAUSE}$ pulse until pause		t_{PP}	—	—	250	µs
Time from input of $\overline{ST}$ pulse to the continuation of record/playback during pause		t_{PSP}	—	—	500	µs
PDMD = "L"	Oscillator stable time after input of $\overline{ST}$ pulse	t_{ANA}	—	32	—	ms
	$\overline{SP}$ pulse (during recording) to the fall of MON	t_{SPM1}	—	—	1	ms
	$\overline{SP}$ pulse (during playback) to the fall of MON	t_{SPM2}	—	—	260	ms
	Standby transient time at start of playback	t_{AOR}	—	64	—	ms
	Standby transient time at end of playback	t_{AOF}	—	256	—	ms
	Time from fall of MON to power down state at the end of playback	t_{MS}	—	70	—	µs
	$\overline{SP}$ pulse during pause to record end	t_{PSP1}	—	—	1	ms
	$\overline{SP}$ pulse during pause to playback end	t_{PSP2}	—	—	260	ms
PDMD = "H"	$\overline{ST}$ pulse to MON rise	t_{STM}	—	—	1	ms
	$\overline{SP}$ pulse to MON fall	t_{SPM1}	—	—	1	ms
	$\overline{ST}$ pulse to voice standby state	t_{STV}	—	—	1	ms
	$\overline{SP}$ pulse during pause to record/playback end	t_{PSP1}	—	—	1	ms

Note: 1. When the PDMD pin is "L", the oscillation stable time is added to t_{ST}. The oscillation stable time is several tens of milliseconds for crystal oscillators and is several hundreds of microseconds for ceramic oscillators.

3. Microcontroller interface mode

DV_{DD} = $DV_{DD'}$ = AV_{DD} = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = –40 to +85°C
When f_{samp} = 8 kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
$\overline{RD}$ pulse width		t_{RR}	200	—	—	ns
Setup and hold time of $\overline{CE}$ for $\overline{RD}$		t_{CR}	0	—	—	ns
Data valid from fall of $\overline{RD}$		t_{DRE}	—	—	200	ns
Data Hi-Z from rise of $\overline{RD}$		t_{DRF}	—	10	50	ns
$\overline{WR}$ pulse width		t_{WW}	200	—	—	ns
Setup and hold time of $\overline{CE}$ from $\overline{WR}$		t_{CW}	0	—	—	ns
Data setup time to rise of $\overline{WR}$		t_{DWS}	100	—	—	ns
Data hold time from rise of $\overline{WR}$		t_{DWH}	30	—	—	ns
Disable time for $\overline{RD}$ and $\overline{WR}$		t_{DRW}	250	—	—	ns
BUSY time after release of $\overline{RESET}$ (Note 1)	*	t_{BR}	—	—	125	µs
BUSY time after input of 1 nibble command	*	t_{B1}	—	—	16	µs
BUSY time after input of 2 nibble command	*	t_{B2}	—	—	16	µs
BUSY time after input of 2 nibble command data	*	t_{BD}	—	—	16	µs
BUSY time after input of ADRWR command	*	t_{BAW}	—	—	270	µs
BUSY time after input address data of ADRWR command	*	t_{BAD}	—	—	50	µs
Data input time after input of ADRRD command	*	t_{WAR}	270	—	—	µs
Time between output of address data nibbles during ADRRD command	*	t_{WDR}	50	—	—	µs

Items with * are proportional to the period of sampling frequency (f_{samp}).
Note: 1. The oscillation stable time is added to t_{BR}.
The oscillation stable time is several tens of milliseconds for crystal oscillators and is several hundred of microseconds for ceramic oscillators.

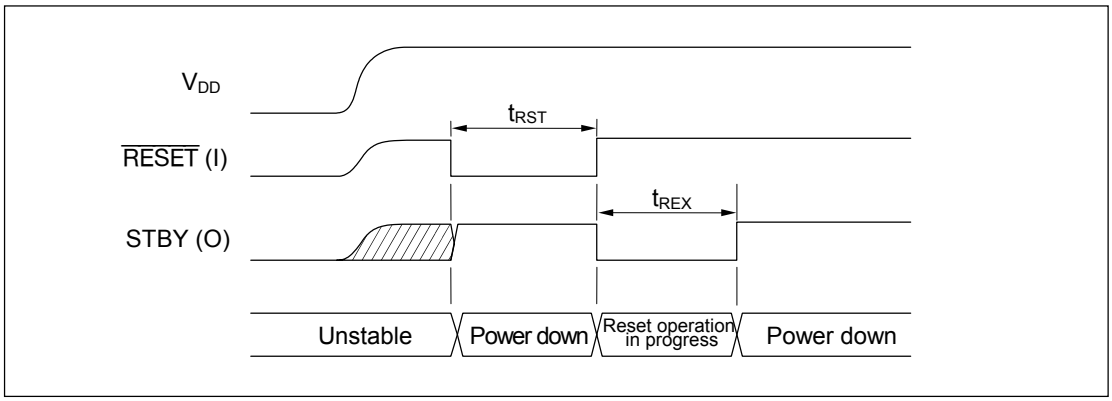
Parameter			Symbol	Min.	Typ.	Max.	Unit
Address control time at start of record/playback		*	t_{AD1}	—	1	—	ms
Address control time at end of recording		*	t_{AD2}	—	1	—	ms
START command to rise of MON		*	t_{STCM}	—	—	1	ms
STOP command to fall of MON		*	t_{SPCM}	—	—	1	ms
START command to RPM bit set (“H” level)		*	t_{STCR}	—	—	16	µs
START command (during voice triggered starting) to VPM bit set (“H” level)		*	t_{STCV}	—	—	16	µs
STOP command to release of voice standby (during voice triggered starting)		*	t_{SPCV}	—	—	500	µs
PAUSE command to VPM bit set (“H” level)		*	t_{PSCP}	—	—	16	µs
START command (during pause) to VPM bit reset (“L” level)		*	t_{STCP}	—	—	500	µs
STOP command (during pause) to VPM bit reset (“L” level)		*	t_{SPCP}	—	—	500	µs
When DTRW command is being executed	Delay time after input of DTRW command	*	t_{WRW}	16	—	—	µs
	Delay time after input of lower 4-bit of X address	*	t_{WXA1}	16	—	—	µs
	Delay time after input of middle 4-bit of X address	*	t_{WXA2}	16	—	—	µs
	Delay time after input of upper 4-bit of X address	*	t_{WXA3}	270	—	—	µs
	Delay time after input of REC command	*	t_{WRC}	16	—	—	µs
	Delay time after input of write data	*	t_{WWD}	50	—	—	µs
	Delay time after input of PLAY command	*	t_{WPL}	50	—	—	µs
	Delay time after input of STOP command	*	t_{WSP}	16	—	—	µs
When executing EXT command	EXT command to rise of MON	*	t_{EM}	125	—	330	µs
	“H” level time of MON	*	t_{MH}	—	31	—	µs
	“L” level time of MON	*	t_{ML}	—	94	—	µs
	MON rise to $\overline{RD}$ pulse rise (during recording)	*	t_{ERD}	—	—	120	µs
	MON rise to $\overline{WR}$ pulse rise (during playback)	*	t_{EWR}	—	—	120	µs
	ADPCM data write pulse to input of STOP command	*	t_{WE1}	16	—	—	µs
	STOP command until rise of MON	*	t_{ESP}	—	—	100	µs
	STOP command to record/playback end	*	t_{WEX}	—	—	250	µs

Items with * are proportional to the period of sampling frequency (f_{samp}).

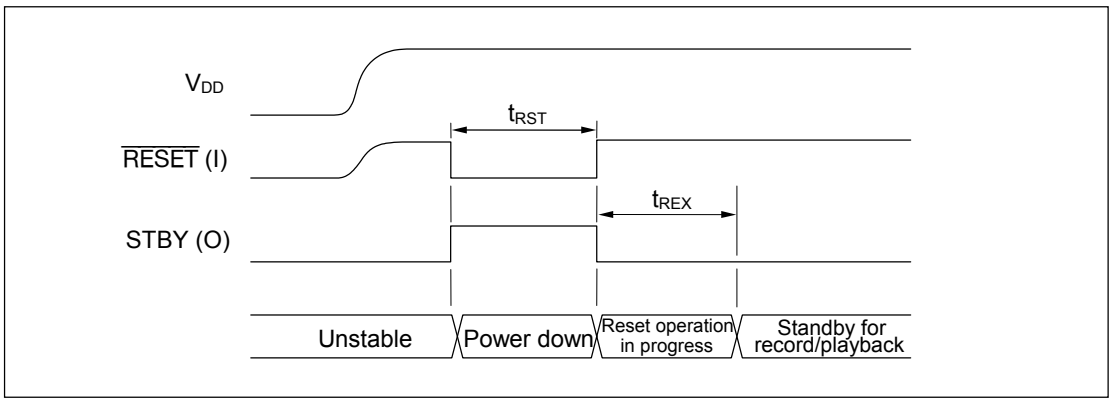
TIMING DIAGRAMS

Reset Function and Power Down Function

1. Stand-alone mode when the PDMD pin is “L”.

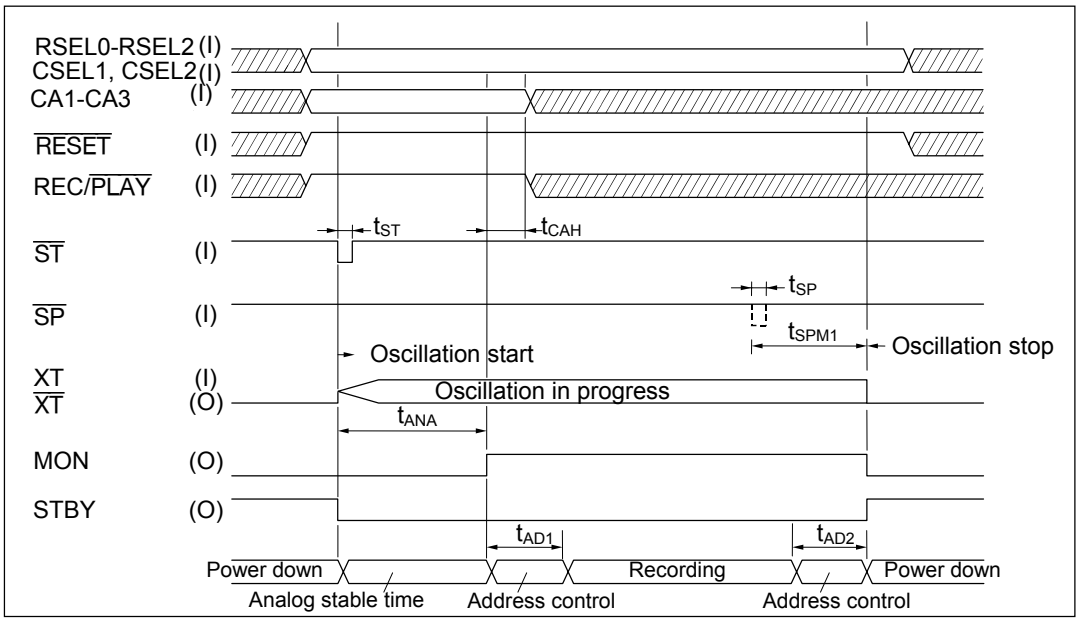


2. Stand-alone mode when the PDMD pin is “H” and in microcontroller interface mode.

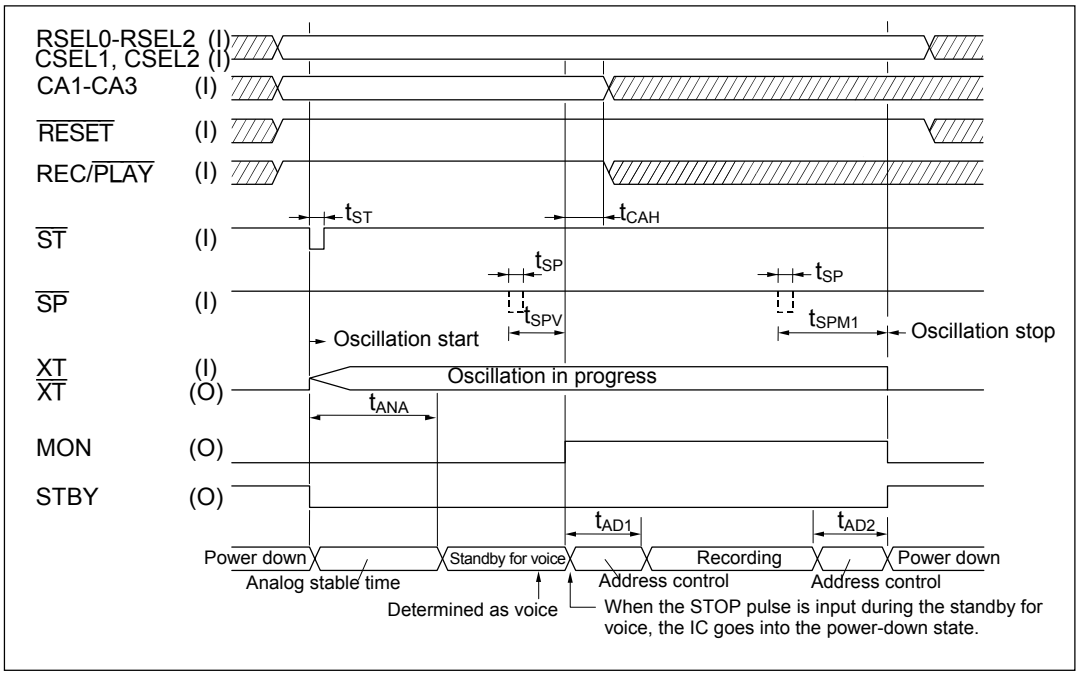


Stand-alone Mode

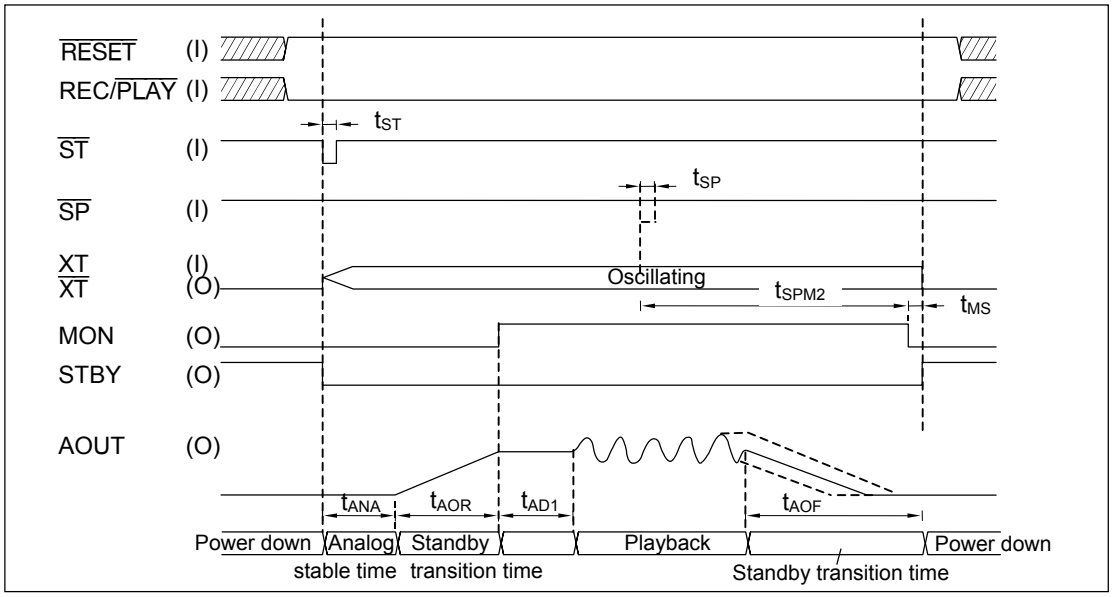
1. Timing during recording (PDMD pin = “L”, VDS pin = “L”)



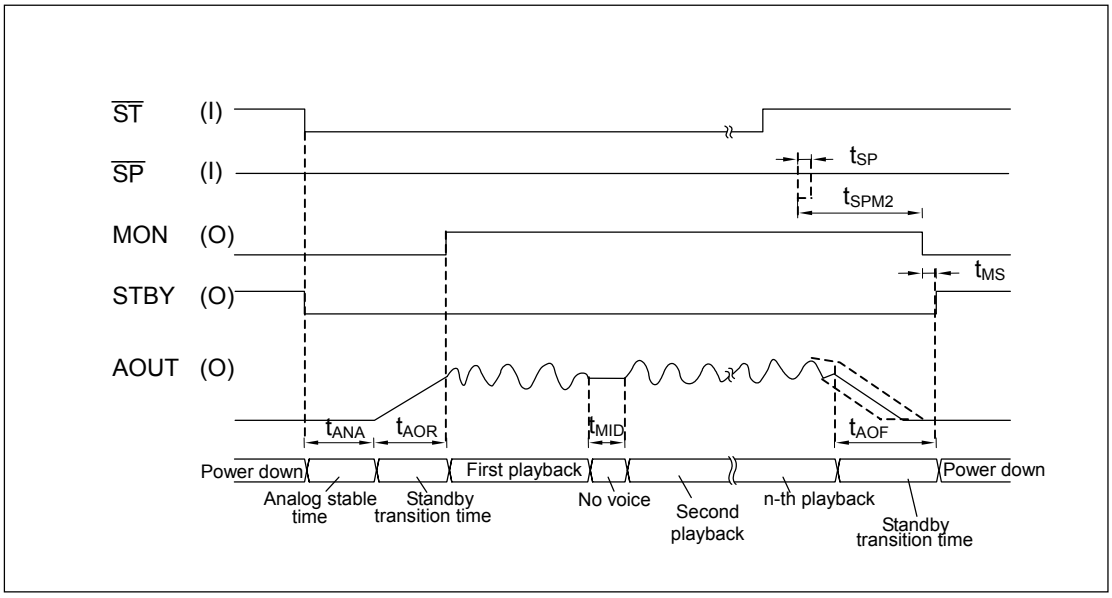
2. Timing during recording by voice triggered starting (PDMD pin = “L”, VDS pin = “H”)



3. Timing during playback (PDMD pin = “L”)

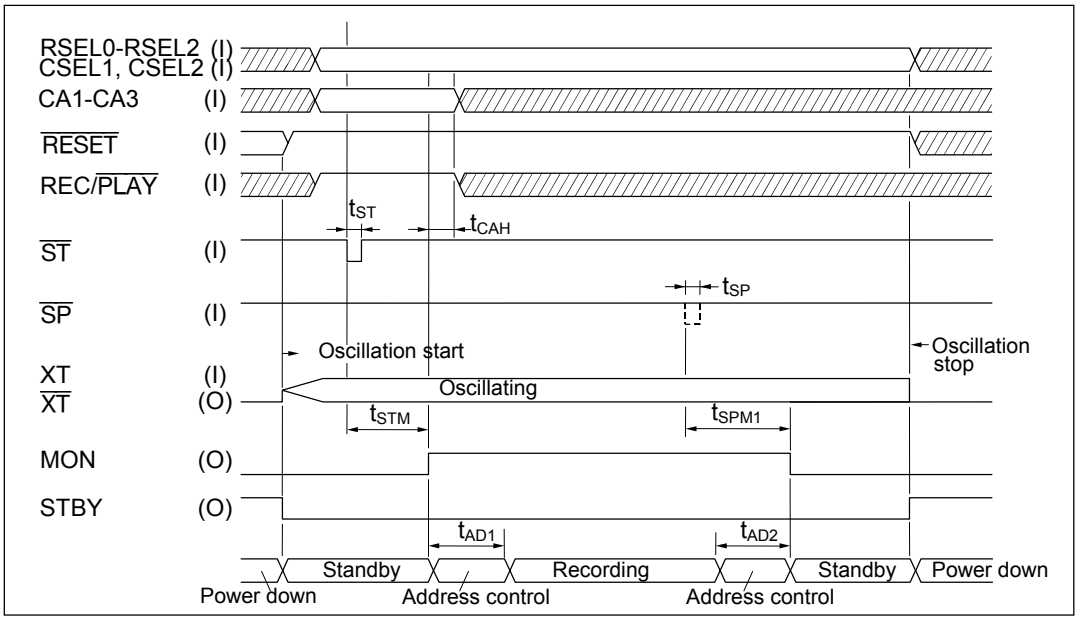


4. Timing during repeated playback (PDMD pin = “L”)

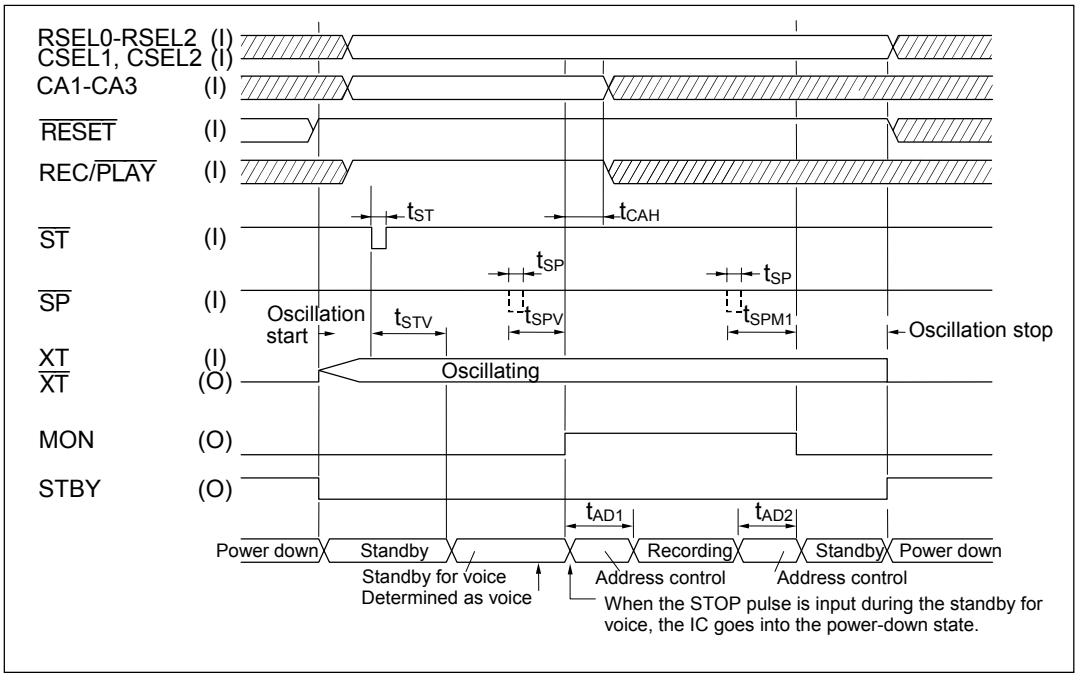


Note: Repeated playback is executed only when only one serial register is connected.

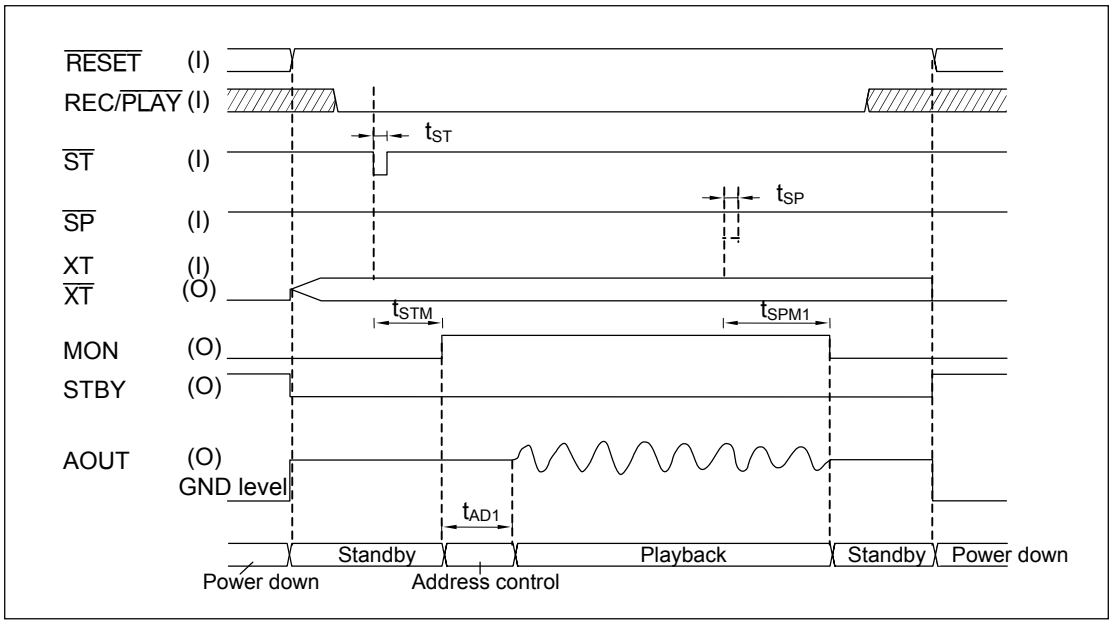
5. Timing during recording (PDMD pin = “H”, VDS pin = “L”)



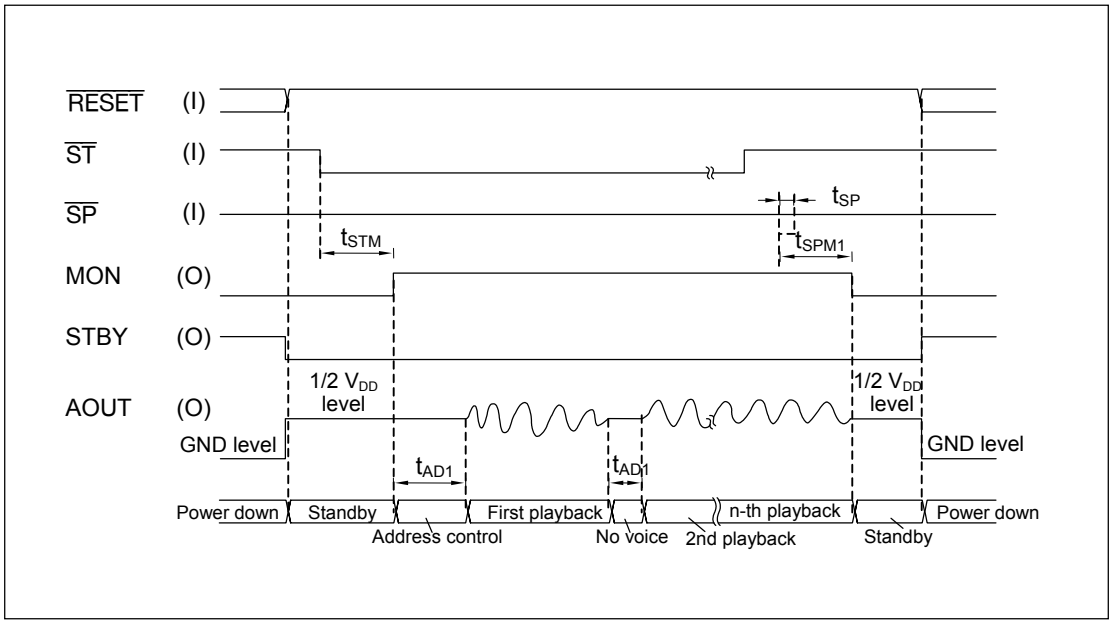
6. Timing during recording by voice triggered starting (PDMD pin = “H”, VDS pin = “H”)



7. Timing during playback (PDMD pin = "H")

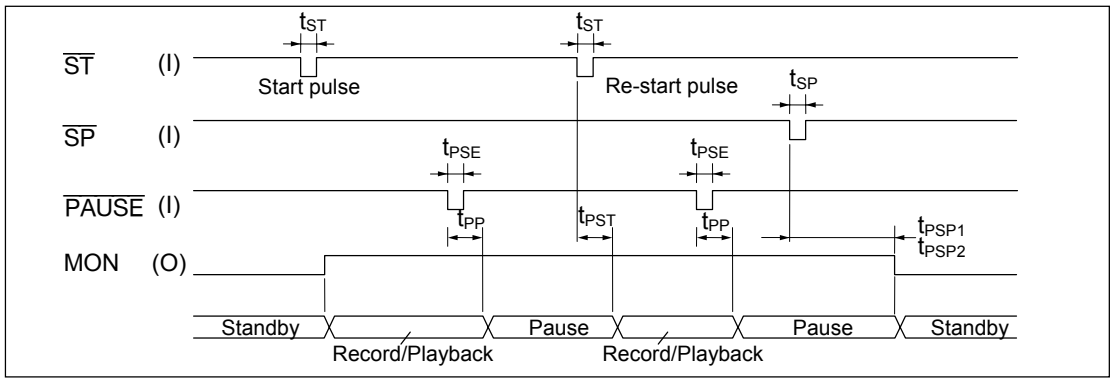


8. Timing during repeated playback (PDMD pin = "H")



Note: Repeated playback is executed only when only one serial register is connected.

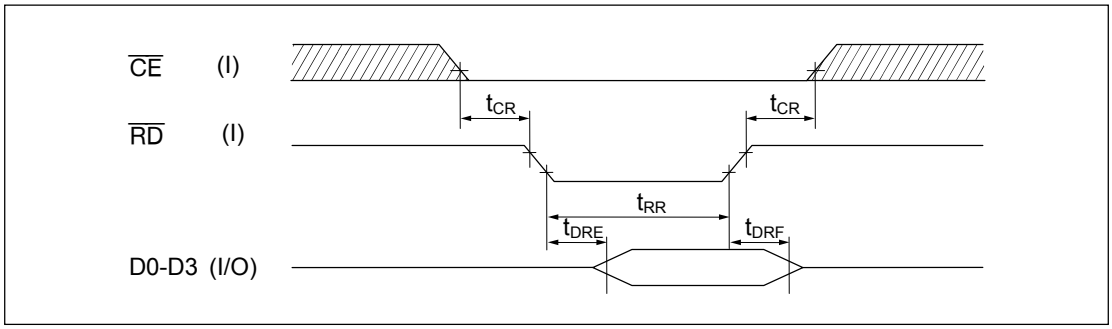
9. Timing of pause in record/playback



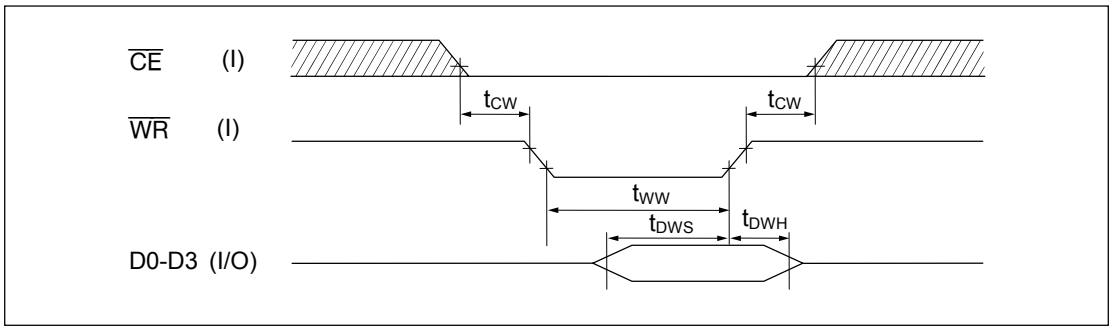
Note: t_{PSP1}: for recording or playback with the PDMD pin = “H”
t_{PSP2}: for recording or playback with the PDMD pin = “L”

Microcontroller Interface

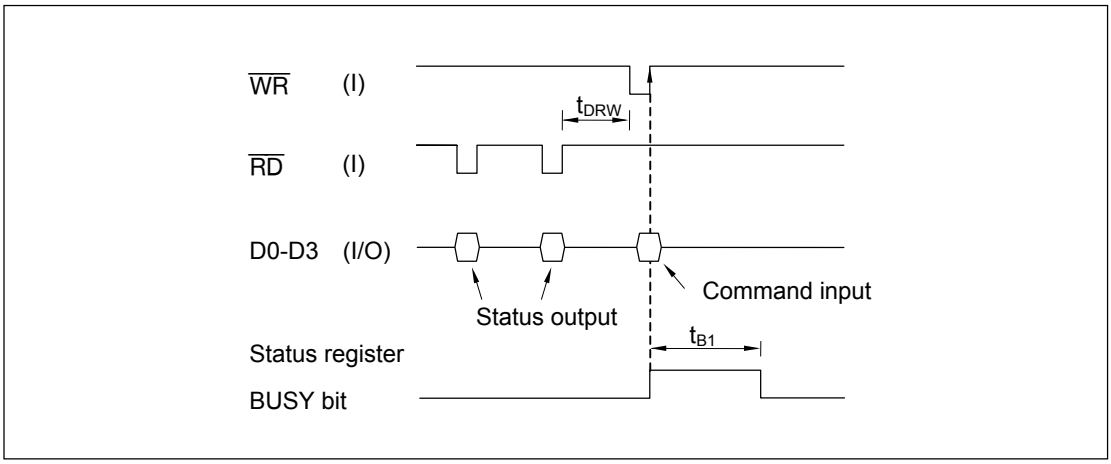
1. Data read ($\overline{RD}$ pulse)



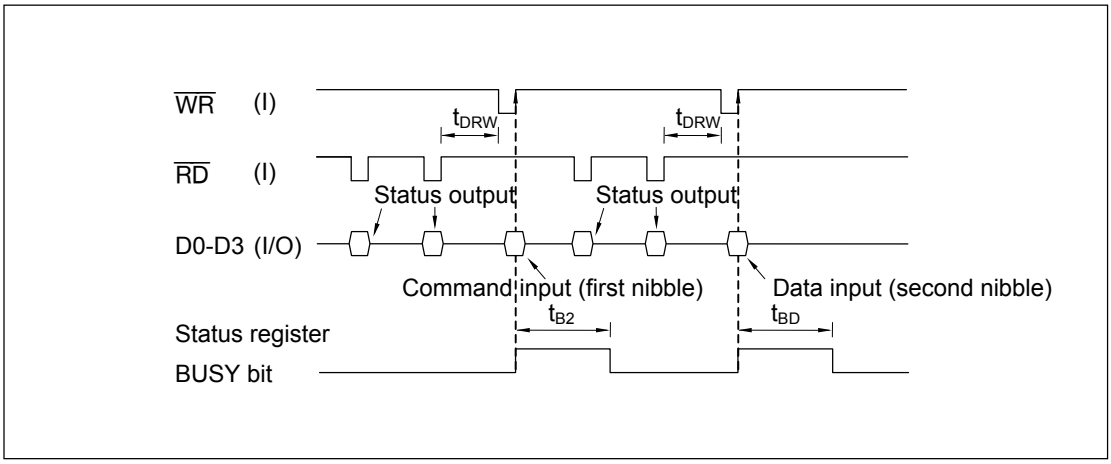
2. Data write ($\overline{WR}$ pulse)



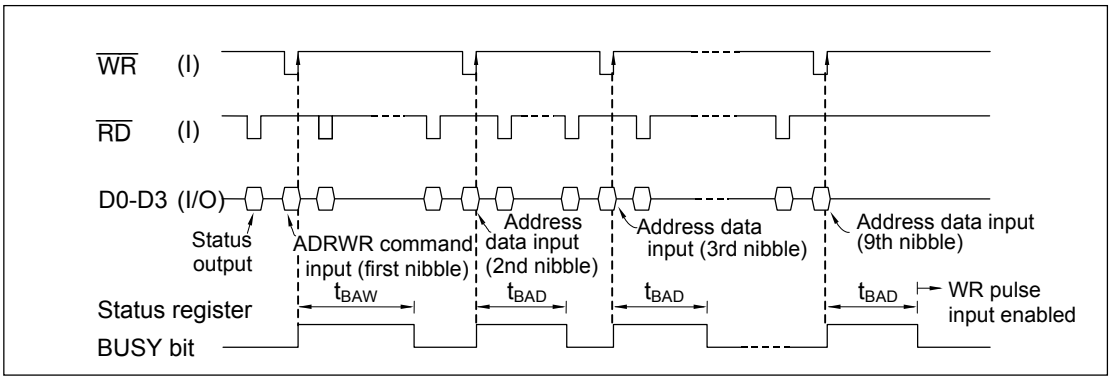
3. Input method of 1 nibble command (NOP, PAUSE, PLAY, REC, START and STOP commands)



4. Input method of 2 nibble command (SAMP, CHAN and VDS commands)

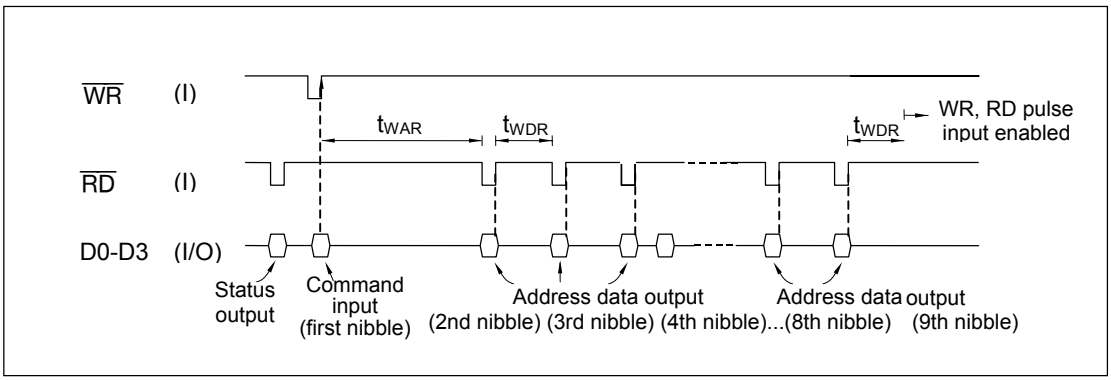


5. Input method of ADRWR command



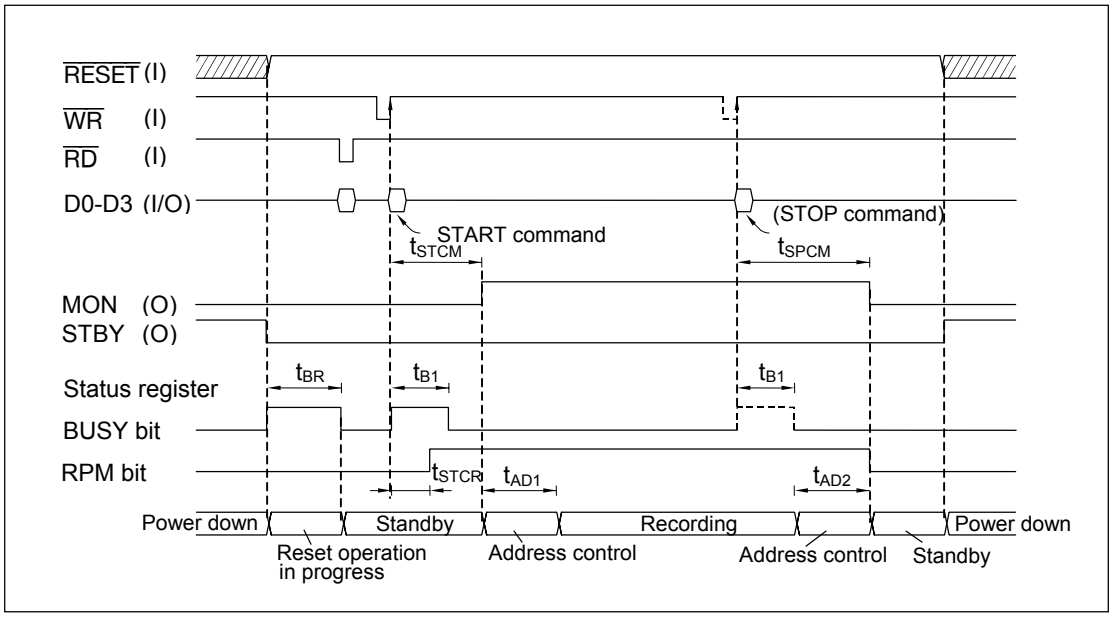
Notes: 1. In the BUSY bit of the status register, input the command after checking that it is not in the BUSY state.
2. Next, input the address data into 2nd through 9th nibble command, but after checking that the status is not BUSY by either method as follows.
- Check on the Busy bit of the status register
- Input the next $\overline{WR}$ pulse after the waiting time of t_{BAW} or t_{BAD}

6. Input method of ADRRD command

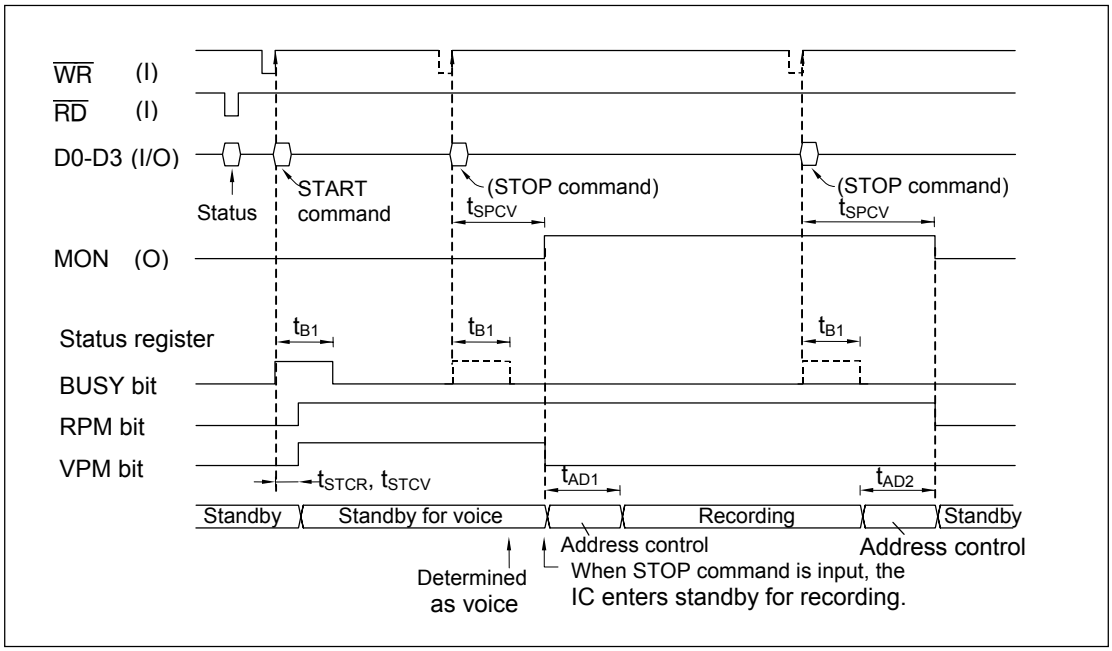


Notes: 1. In the BUSY bit of the status register, input the command after checking that it is not in the BUSY state.
2. Next, read out the address data into 2nd through 9th nibble command, but this can not check the BUSY bit by the $\overline{RD}$ pulse input. Input the next $\overline{RD}$ pulse after waiting time of t_{WAR} or t_{WDR}.

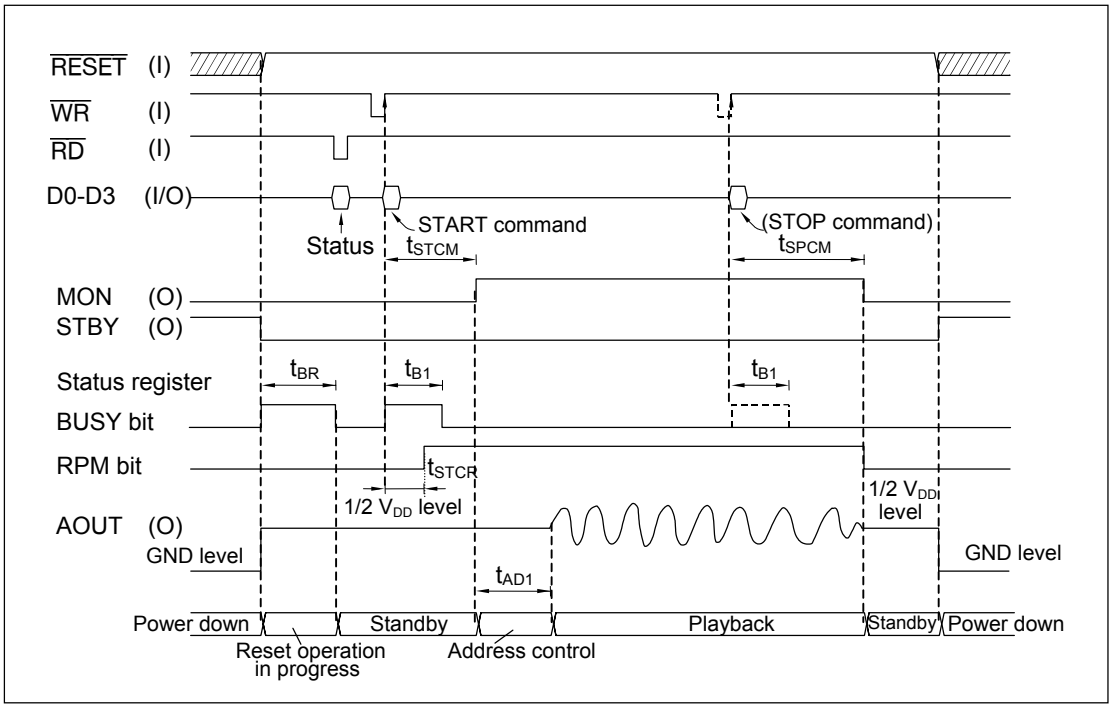
7. Recording method by START command



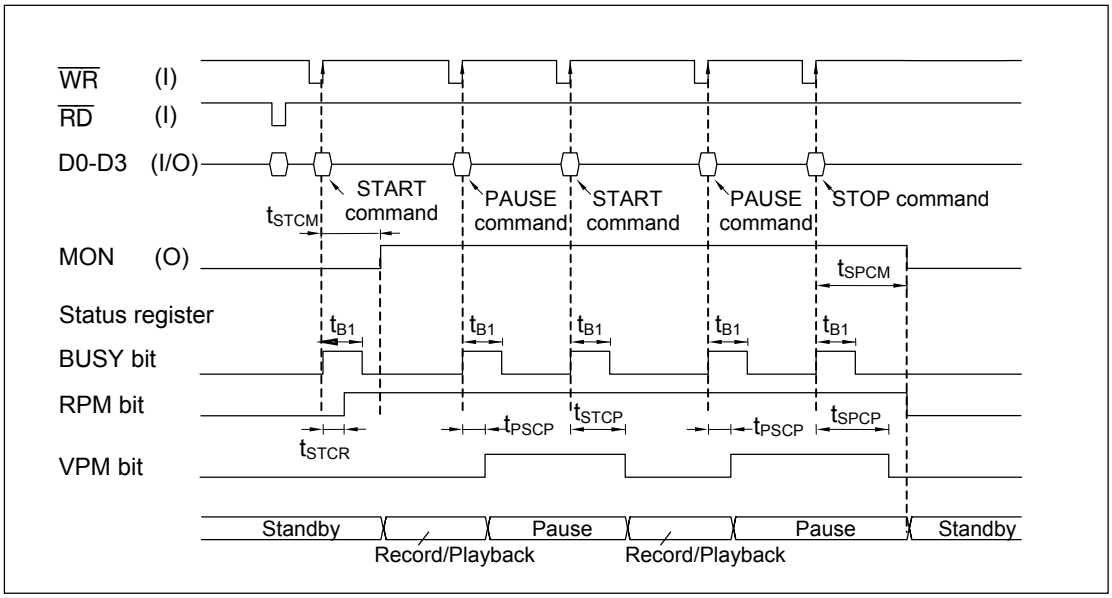
8. Timing of voice triggered starting



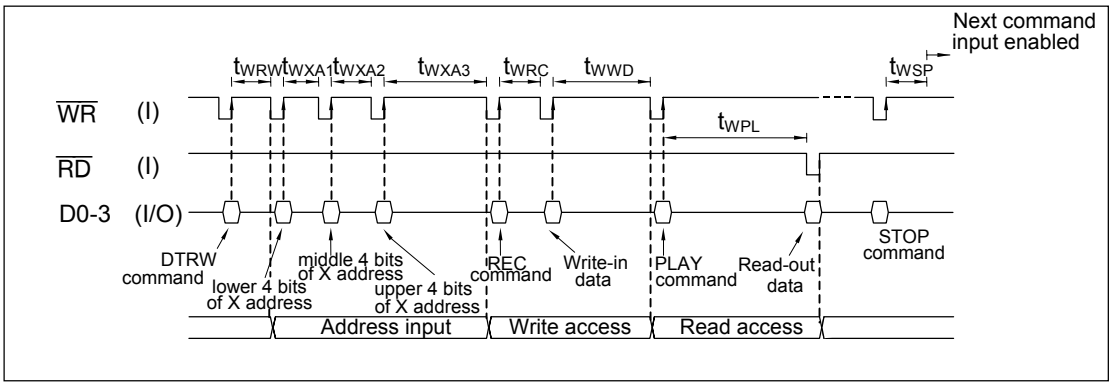
9. Playback method using START command



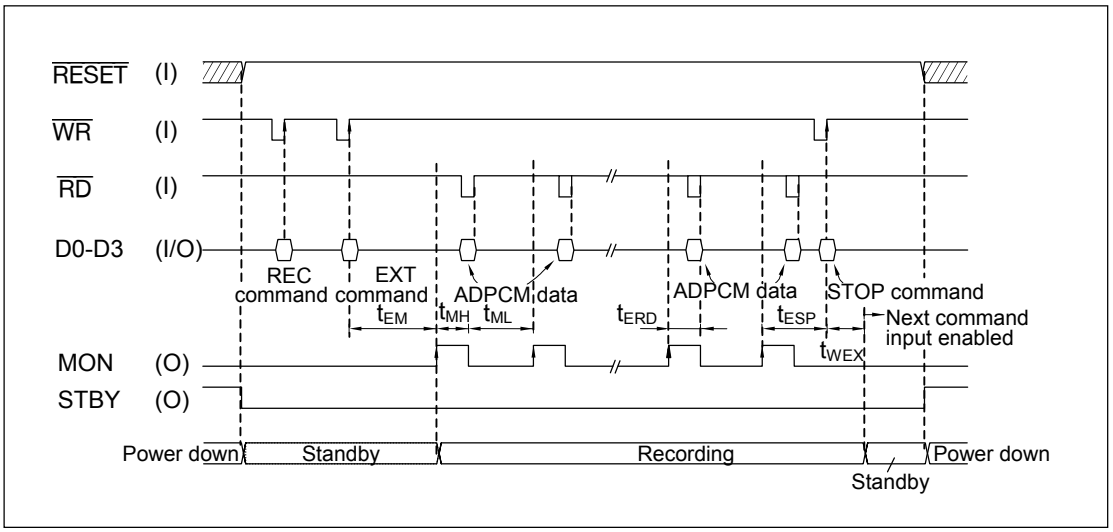
10. Timing of pause in record/playback using PAUSE command



11. Timing of data transfer by DTRW command



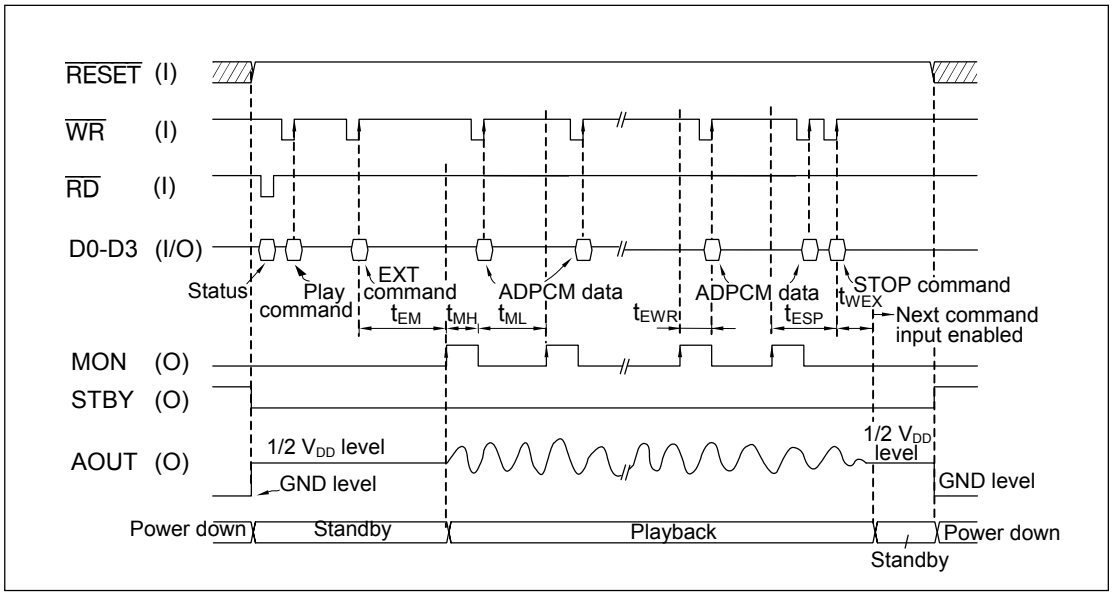
12. Timing of recording by EXT command



Notes: 1. When reading the ADPCM data, input the $\overline{RD}$ pulse to satisfy time t_{ERD} from rise of MON to rise of the $\overline{RD}$ pulse.

2. Input the STOP command when the MON pin is “H”, after reading the ADPCM data. At that time, it is required to satisfy time t_{ERD} from rise of MON to input of the STOP command.

13. Timing of playback by EXT command



Notes: 1. When writing the ADPCM data, input the $\overline{WR}$ pulse to satisfy time t_{EWR} from rise of MON to rise of the $\overline{WR}$ pulse.

2. Input the STOP command when the MON pin is “H”, after writing the ADPCM data. At that time, it is required to satisfy time t_{ESP} from rise of MON to input of the STOP command, and interval t_{WE1} between the $\overline{WR}$ pulse and the STOP command pulse.

3. Input the ADPCM data beginning with the top of a phrase every sampling period sequentially. If the ADPCM data is input beginning with the second or following part of a phrase or with data missing, normal (playback) waveforms cannot be regenerated.

FUNCTIONAL DESCRIPTION

Recording Time and Memory Capacity

Recording time depends on the memory capacity of the external serial registers, sampling frequency, and the ADPCM bit length, and is expressed as

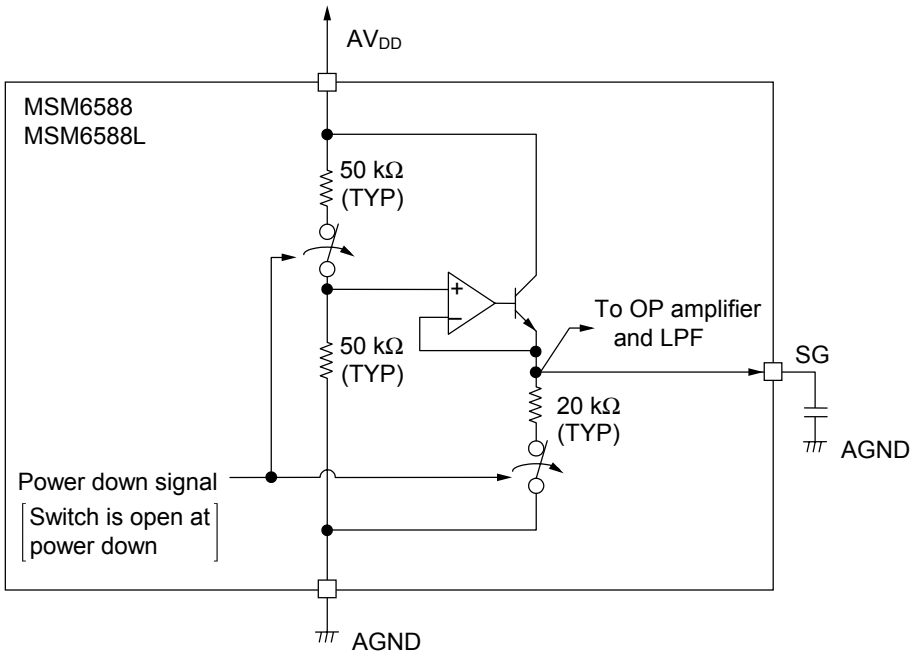
$$\text{Recording time} = \frac{1.024 \times \text{memory capacity (Kbit)}}{\text{sampling frequency (kHz)} \times \text{bit length}} \text{ (sec)}$$

For example, if the sampling frequency is 5.3 kHz with a 3-bit ADPCM and 4 serial registers, it is possible to record up to 262 seconds because

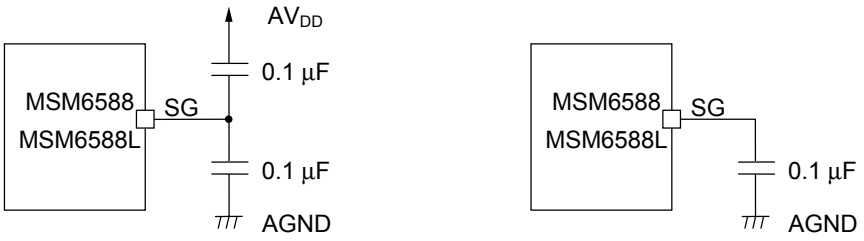
$$\text{Recording time} = \frac{1.024 \times 1024 \text{ (Kbit)} \times 4}{5.3 \text{ (kHz)} \times 3 \text{ (bit)}} = 262 \text{ (sec)}$$

Configuring SG pin

The internal equivalent circuit around the SG pin is shown below.



The SG signal is a reference voltage (signal ground) for internal OP amplifiers and LPF.
Install a capacitor as shown below in order to make the SG signal noiseless.
It is recommended to install an approx. 0.1 µF capacitor, which should be determined after evaluating the tone quality.

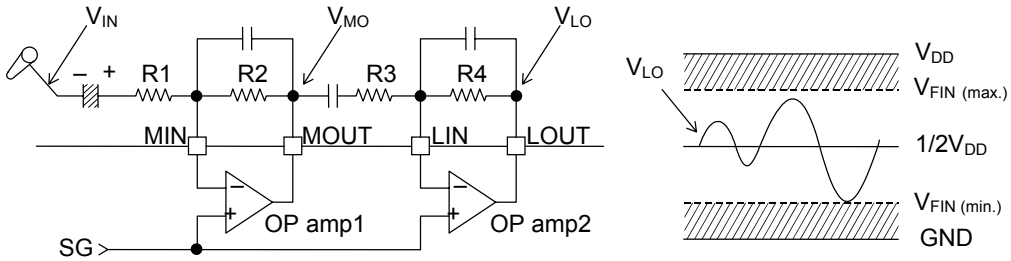


It takes several ten msec until the DC levels such as the SG level of the analog circuit is stabilized after the power-down mode is cancelled. The larger capacitance of a capacitor connected to SGC or SG requires the longer time for stabilizing.
After the power-down mode is cancelled, activate the recording or playback operation after the DC levels for the analog circuit has been stabilized.
When the device is in power-down mode, the output voltage of the SG pin becomes unstable. Therefore, SG must not be supplied to external circuits.
Otherwise, power supply current may be leaked via the internal SG circuit.

Analog Input Amplifier Circuit

This IC has two built-in operational amplifiers for amplifying the microphone output. Each OP amplifier is provided with the inverting input pin and output pin. The analog circuit reference voltage SG (signal ground) is connected internally to the non-inverting input of each OP amplifier.

For amplification, form an inverting amplifier circuit and adjust the amplification ratio by using external resistors as shown below.



$$V_{LO} = \frac{R4}{R3} \quad V_{MO} = \frac{R2 \bullet R4}{R1 \bullet R3} \; V_{IN} \; (V)$$

During recording, the output V_{LO} of OP amp 2 is connected to the input FIN of the LPF. Adjust the amplification ratio by using the external resistors so that the V_{LO} amplitude is within the FIN admissible input voltage (V_{FIN}) range.

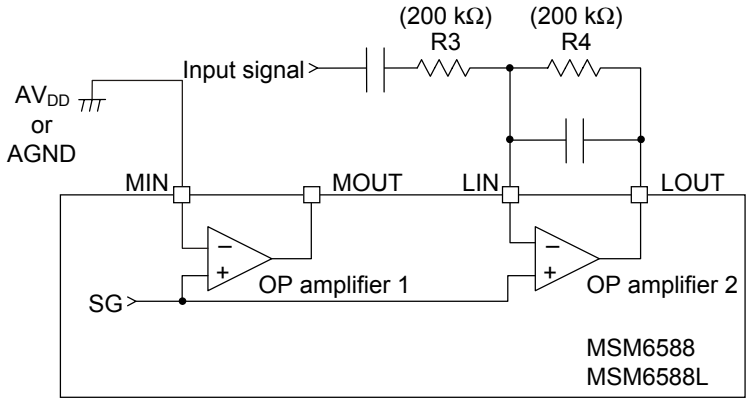
If V_{LO} exceeds the V_{FIN} range, the LPF output waveform will be distorted.

The table below shows an example of the FIN admissible input voltage range for the MSM6588 and the MSM6588L.

Parameter	Power supply voltage V_{DD}	FIN admissible input voltage range V_{FIN}		FIN admissible input voltage
		Min.	Max.	
MSM6588	5 V	1 V	4 V	3 V_{P-P}
MSM6588L	3 V	0.75 V	2.25 V	1.5 V_{P-P}

The value of the OP amp load resistance R_{OUTA} is 200 kΩ minimum. Therefore the values of the inverting amplifier circuit feedback resistors R2 and R4 should be 200 kΩ or more.

When OP amplifier 1 is not used and OP amplifier 2 is used, the MIN pin must be connected to AGND or AV_{DD}, and the MOUT pin must be open.
Even if amplification is unnecessary, OP amplifier 2 must be always used.
Below is an example of an analog input amplifier circuit when R3 and R4 each are 200 kΩ and the amplification factor is 1.



Connection of LPF Circuit Peripherals

Inside the IC, the AMON pin is connected to the output of the amplifying circuit in recording mode (LOUT pin) and output of the DA converter in playback mode. This means that the AMON pin is directly connected to the input pin (FIN pin) of the built-in LPF.
Both the FOUT pin and AOUT pin are output pins of the built-in LPF. The FOUT pin is connected to the input pin (ADIN pin) of the AD converter and the AOUT pin is connected to a speaker through the speaker amplifier.
The connection of the FOUT pin and the AOUT pin changes according to the output of LPF, SG level or GND level inside the LSI depending on the operation state which is summarized by the following:

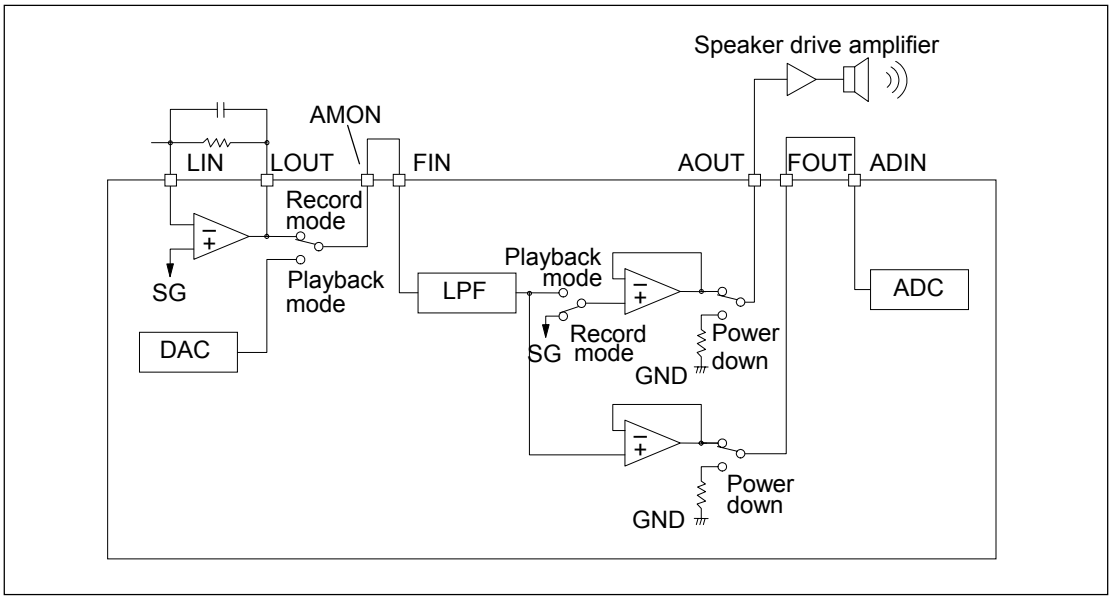
- Microcontroller interface mode and stand-alone mode when the PDMD pin = "H"

Analog pin	At power down ($\overline{\text{RESET}}$ pin = "L")	During operation ($\overline{\text{RESET}}$ pin = "H")	
		Recording mode	Playback mode
FOUT pin	GND level	LPF output (record wave form)	LPF output
AOUT pin	GND level	SG level	LPF output (playback wave form)

- Stand-alone mode when the PDMD pin = "L"

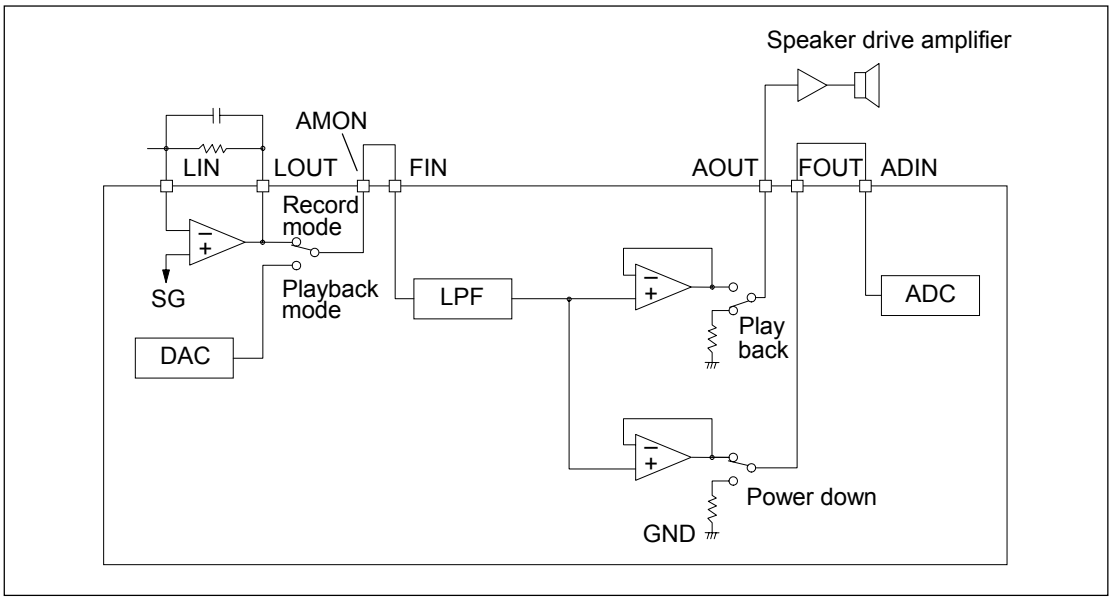
Analog pin	At power down	During operation	
		Recording mode	Playback mode
FOUT pin	GND level	LPF output (record wave form)	LPF output
AOUT pin	GND level	GND level	LPF output (playback wave form)

- Microcontroller interface mode and stand-alone mode when the PDMD pin = “H”



Note: Switches in the figure denote the state during record operation.

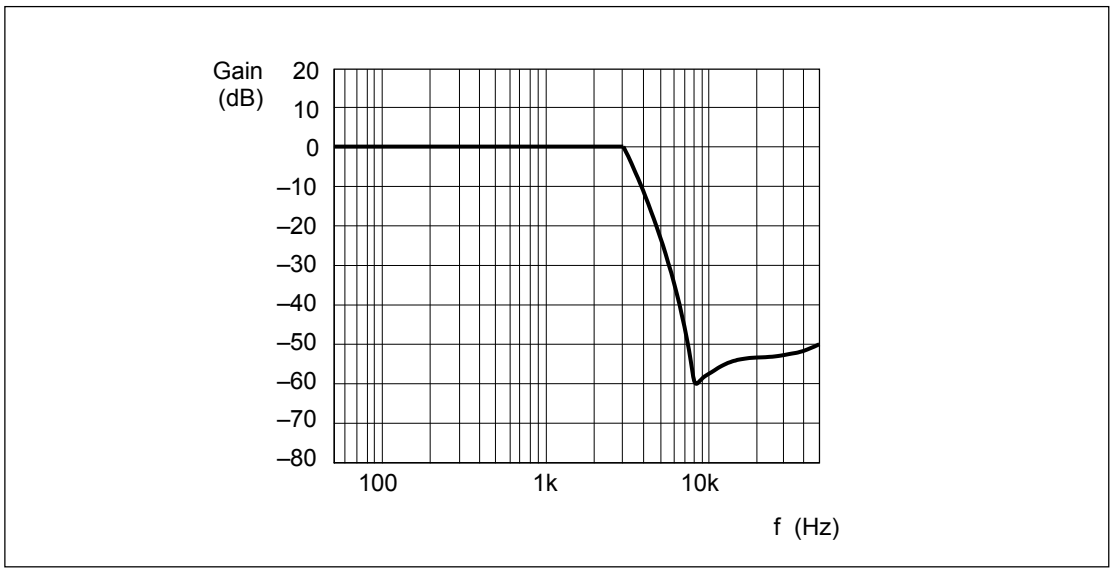
- Stand-alone mode when the PDMD pin = “L”



Note: Switches in the figure denote the state during record operation.

LPF Characteristics

This IC has a built-in fourth order LPF using switched capacitor filter technology.
The filter characteristics are –40 dB/oct. Both the cut-off frequency and frequency characteristics change in proportion to the sampling frequency (f_{samp}).
The cut-off frequency is preset to 0.4 times the sampling frequency. The following graph depicts the frequency characteristics of LPF when f_{samp} = 8 kHz.

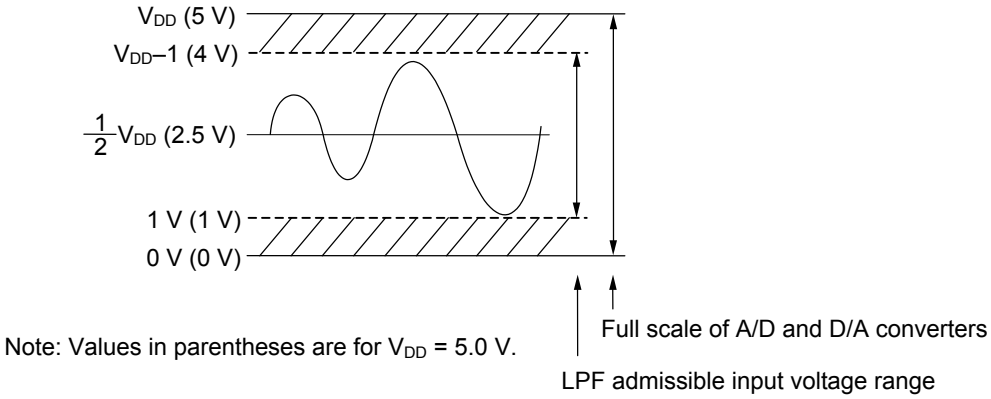


LPF Frequency Characteristics (f_{samp} = 8.0 kHz)

Full Scale of A/D and D/A Converters

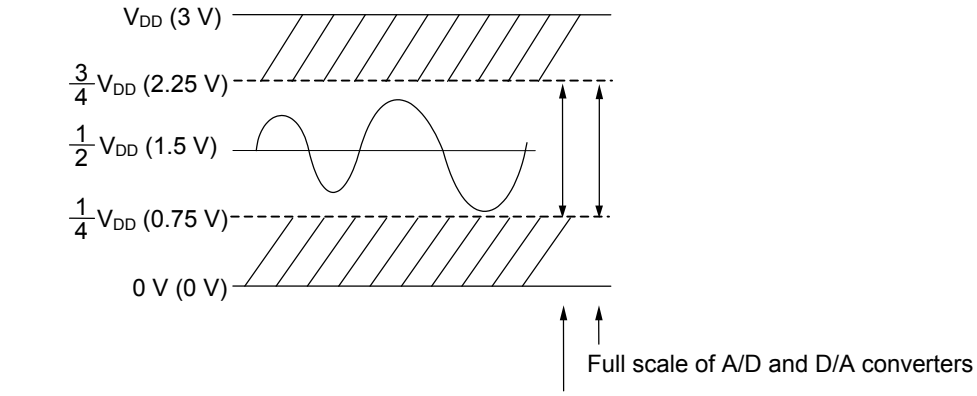
Parameter	Full scale of A/D and D/A converters		
	Min. (V)	Max. (V)	Amplitude (V_{p-p})
MSM6588	0	V_{DD}	V_{DD}
MSM6588L	$\frac{1}{4} \times V_{DD}$	$\frac{3}{4} \times V_{DD}$	$\frac{1}{2} \times V_{DD}$

1. When the MSM6588 is used



Note: Values in parentheses are for V_{DD} = 5.0 V.

2. When the MSM6588L is used

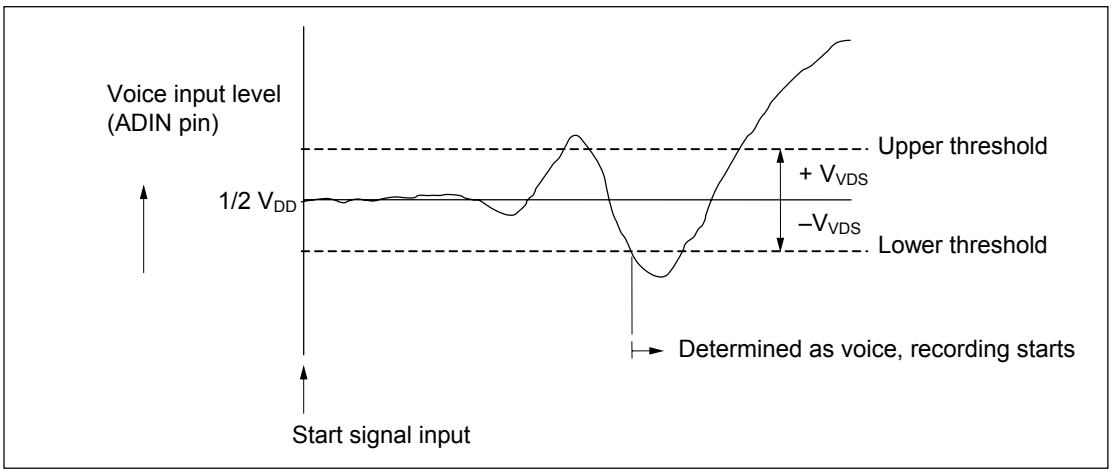


Note: Values in parentheses are for V_{DD} = 3.0 V.

Voice Triggered Starting

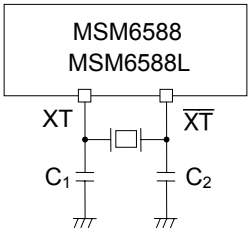
This IC has a voice triggered starting function that starts recording when the amplitude of voice input exceeds a preset threshold.
The voice triggered starting function is controlled by the VDS pin in stand-alone mode and by the VDS command in microcontroller interface mode. The voice standby state can be released by a STOP pulse or the STOP command.
During recording/playback using the EXT command in microcontroller interface mode, voice triggered starting cannot be used.

Stand-alone mode		VDS pin	L	—	H	—
Microcontroller interface mode		VD1	0	0	1	1
		VD0	0	1	0	1
Voice detection level V_{VDS}	MSM6588 (5 V version) Values inside ( ) are for V_{DD} = 5.12 V		Voice triggered starting disabled	$\pm V_{DD}/64$ (±80 mV)	$\pm V_{DD}/32$ (±160 mV)	$\pm V_{DD}/16$ (±320 mV)
	MSM6588L (3 V version) Values inside ( ) are for V_{DD} = 3.072 V		Voice triggered starting disabled	$\pm V_{DD}/128$ (±24 mV)	$\pm V_{DD}/64$ (±48 mV)	$\pm V_{DD}/32$ (±96 mV)



How to Connect an Oscillator

Connect a ceramic oscillator or a crystal oscillator to XT and $\overline{XT}$ pins as shown below.
The optimal load capacities when connecting ceramic oscillators from MURATA MFG., KYOCERA CORPORATION, and TDK CORPORATION are shown below for reference.



1. MSM6588

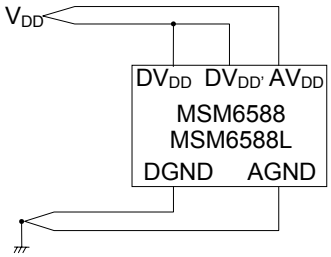
Ceramic oscillator			Optimal load capacity		Power supply voltage (V)	Operating temperature (°C)
Type		Freq. (MHz)	C1 (pF)	C2 (pF)		
MURATA MFG.	CSTLS4M00G53-B0 (with capacitor)	4.0	—	—	3.5 to 5.5	–40 to +85
	CSTCR4M00G53-R0 (with capacitor)					
	CSTLS6M00G53-B0 (with capacitor)	6.0				
	CSTCR6M00G53-R0 (with capacitor)					
	CSTLS8M00G53-B0 (with capacitor)	8.0				
	CSTCC8M00G53-R0 (with capacitor)					
KYOCERA CORP.	KBR-4.0MSA	4.0	33	33	3.5 to 5.5	–40 to +85
	KBR-4.0MWS KBR-4.0MKS (with capacitor)					
	PBRC4.00A					
	KBR-6.0MSA	6.0				
	KBR-6.0MWS KBR-6.0MKS (with capacitor)					
	PBRC6.00A					
	KBR-8.0M	8.0				
	KBR-8.0MWS (with capacitor)					
	PBRC8.00A					
TDK CORP.	FCR4.0MC5 (with capacitor)	4.0	—	—	3.5 to 5.5	–40 to +85

2. MSM6588L

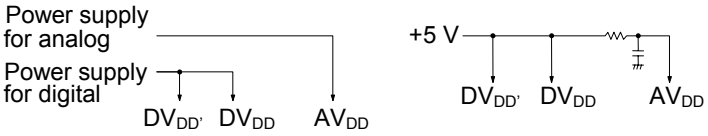
Ceramic oscillator			Optimal load capacity		Power supply voltage (V)	Operating temperature (°C)
Type		Freq. (MHz)	C1 (pF)	C2 (pF)		
MURATA MFG.	CSTLS4M00G53-B0 (with capacitor)	4.0	—	—	2.7 to 3.6	–40 to +85
	CSTCR4M00G53-R0 (with capacitor)					
	CSTLS6M00G53-B0 (with capacitor)	6.0				
	CSTCR6M00G53-R0 (with capacitor)					
	CSTLS8M00G53-B0 (with capacitor)	8.0				
	CSTCC8M00G53-R0 (with capacitor)					
KYOCERA CORP.	KBR-4.0MSB	4.0	33	33	2.7 to 3.6	–40 to +85
	KBR-4.0MKC (with capacitor)					
	PBRC4.00A					
	PBRC4.00B (with capacitor)					
	KBR-6.0MSB	6.00				
	KBR-6.0MKC (with capacitor)					
	PBRC6.00A					
	PBRC6.00B (with capacitor)					
	KBR-8.0M	8.0				
	PBRC8.00A					
	PBRC8.00B (with capacitor)					
TDK CORP.	FCR4.0M5	4.0	33	33	2.7 to 3.6	–40 to +85
	FCR4.0MC5 (with 30 pF capacitor)		—	—		
	FCR6.0M5	6.0	33	33		
	FCR6.0MC5 (with 30 pF capacitor)		—	—		
	FCR8.0M2S	8.0	33	33		

How to Connect Power Supply

This IC uses a single power supply which is divided into two routes on the wiring, one is to the analog section, and the other is to the logic section.



The following connections are not permitted.



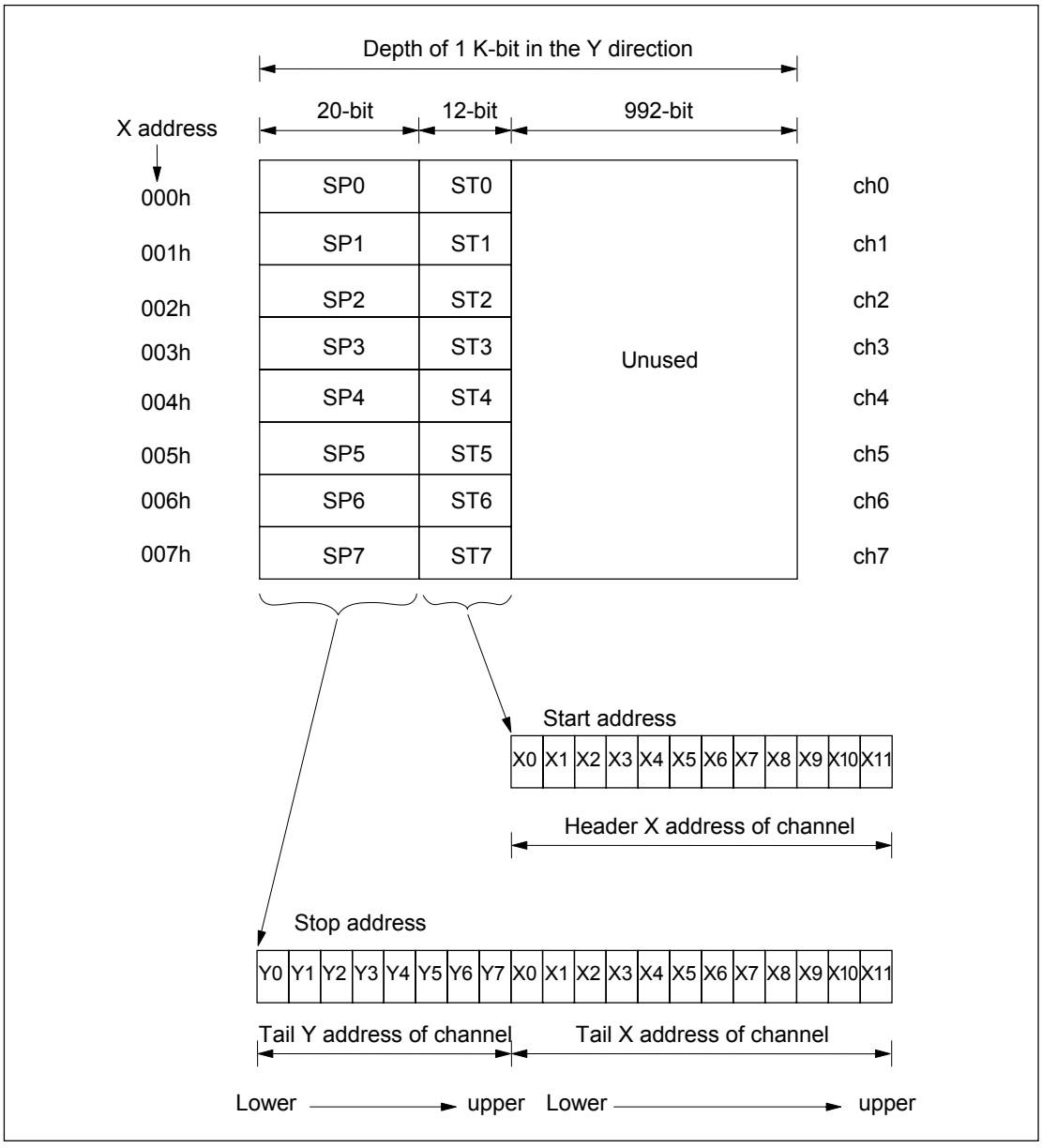
Data Configuration of External Serial Registers

The external serial registers are composed of (X address in the word direction) × (depth of 1K bit) and are divided into the channel index area and the voice (ADPCM) data area.
The maximum address of X address in the word direction can be summarized in the following table depending on the memory capacity of connected serial registers:

Memory capacity of connected serial registers (bit)	Maximum X address
256K	0FFh
512K	1FFh
1M	3FFh
2M	7FFh
3M	BFFh
4M	FFFh

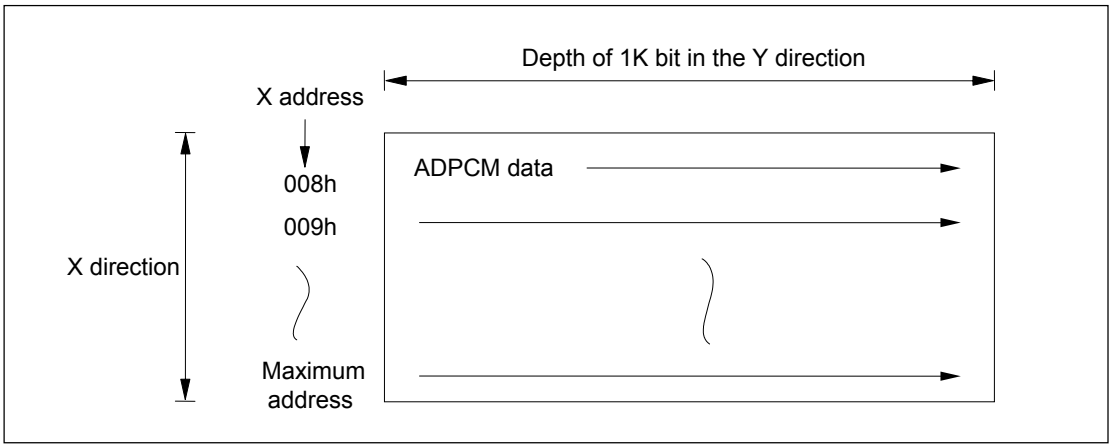
1. Channel index area

Addresses 000h-007h, are header addresses for the serial registers and are known as the channel index area which store the start and stop address of each channel.
The start address and stop address are expressed by 12-bit and by 20-bit, respectively. They store the header and tail addresses of the voice data for each channel.



2. Voice (ADPCM) data area

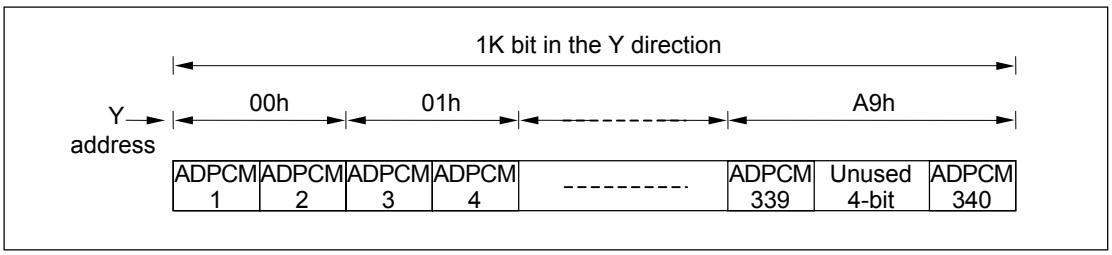
Addresses after 008h of the X address are the voice data area and store ADPCM data.



The storage method of ADPCM data per 1 address in the X-direction (1K bit) is different for 3-bit and 4-bit ADPCM. It is summarized as follows:

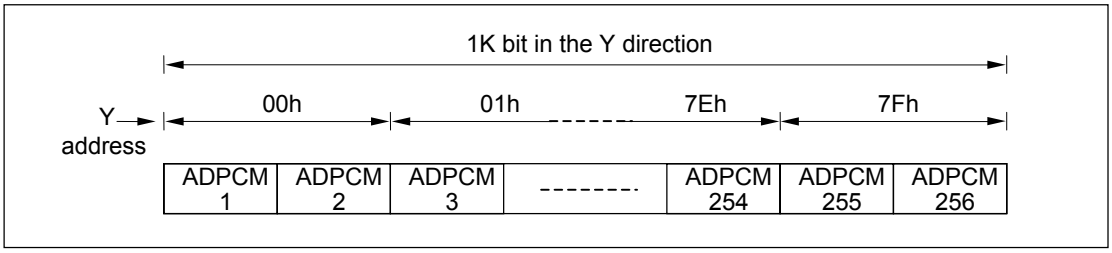
3-bit ADPCM

3-bit data × 340 samples = 1020-bit data are stored in the 1K bit memory area. The Y address is assigned one address per two samples and is controlled by 00h-A9h.



4-bit ADPCM

4-bit data × 256 samples = 1024-bit data are stored in the 1K bit memory area. The Y address is assigned one address per two samples and is controlled by 00h-7Fh.



Selection of Serial Registers

RSEL1 and RSEL2 are used to select the type and the number of serial registers connected externally.
The $\overline{CS4}$ (RSEL0) pin functions as a $\overline{CS4}$ output pin when RSEL1 = RSEL2 = "H" and as an RSEL0 input pin otherwise to select either 512K bit or 256K bit.

RSEL2	L		L	H	H
RSEL1	L		H	L	H
RSEL ($\overline{CS4}$)	L (I)	H (I)	— (I)	— (I)	$\overline{CS4}$ (O)
Number of serial registers	One 256K bit	One 512K bit	One 1M bit	Two 1M bit	Four 1M bit

Recording Control Modes

The recording control modes include fixed and flex mode during stand-alone operation and fixed, flex and direct mode during microcontroller interface operation. The recording control mode is specified by the CSEL1 and CSEL2 pin in stand-alone operation and by data input via commands (RCON, CSEL1 and CSEL2) during microcontroller interface operation.

RCON	CSEL2	CSEL1	Number of recording words	Control mode
L	—	—	8-word	Direct mode (only in microcontroller interface mode)
H	L	L	8-word	Fixed mode (When the number of the recorded words is wished to be selected in one word, select Flex mode.)
	L	H	4-word	
	H	L	2-word	
	H	H	8-word	Flex mode

1. Direct mode

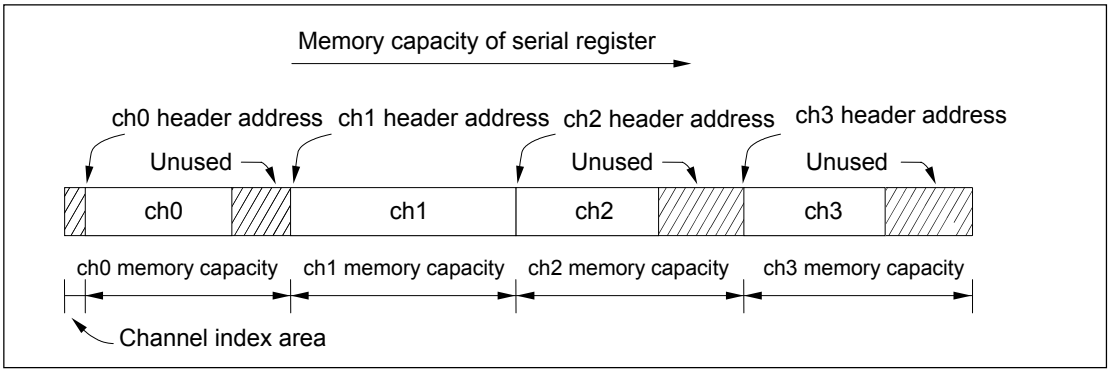
This mode can be used in microcontroller interface mode only.
The start and stop addresses of each channel are input to the channel index area directly from the microcontroller. This means that the assignment of memory capacity of each channel is controlled by the microcontroller.

2. Fixed mode

This mode can be used in both stand-alone mode and microcontroller interface mode.
The start and stop addresses of each channel can be set indirectly by the channel selection (CA1-CA3) and they are input to the channel index area.
The memory capacity of the external serial register equally divided by the number of recording words is assigned to each channel by CSEL1 and CSEL2.
(Hereafter, this will be called the channel memory capacity).

When recording, ADPCM data is written in from the header address of the selected channel memory capacity. When stopping recording by the STOP signal, the memory capacity after that is unused.

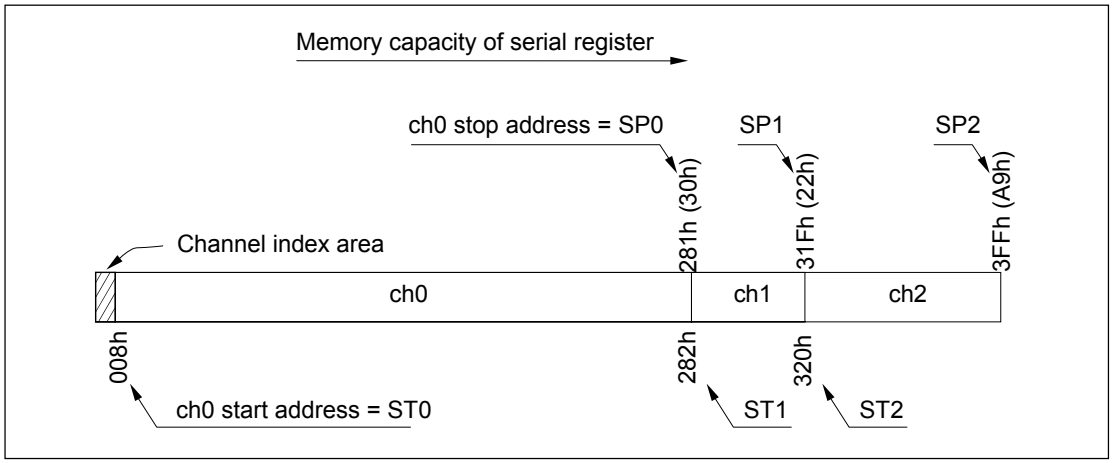
An example of selecting 4-word as the number of recording words



3. Flex mode

This mode can be used in both stand-alone mode and microcontroller interface mode.
The start and stop addresses of each channel are indirectly set by channel selection (CA1-CA3) and are input to the channel index area.
When recording at the initial state (no recording has been performed in any channels), it is necessary to record in the order of ch0 to ch7. When starting recording of ch0, ADPCM data is stored from the header of the voice data area and the recording is stopped when the STOP signal is input. When the STOP signal is not input, recording is stopped when the maximum address of the serial register reached.
When ch1 is selected subsequently, the recordable memory area starts from the address incremented by 1 from the stop address of ch0 through the maximum address. Similarly, the recording continues to ch2, ch3.... The start address of ch_n is the one incremented by 1 from the stop address of ch_{n-1}.

An example of recording 3 words onto 1M bit serial register



Channel Usage

A channel can be specified by CA1, CA2 and CA3. In stand-alone mode, CA1-CA3 pins are used while in microcontroller interface mode, command data is input with (CA1-CA3).

1. Selection of a channel in direct mode and flex mode

The number of recording words is 8 and is specified by CA1-CA3 as follows:

CA3	CA2	CA1	Channel
L	L	L	ch0
L	L	H	ch1
L	H	L	ch2
L	H	H	ch3
H	L	L	ch4
H	L	H	ch5
H	H	L	ch6
H	H	H	ch7

2. Channel selection in fixed mode

The relationship between the number of recorded words (CSEL1, CSEL2) and channels (CA1-CA3) is shown in the following table.

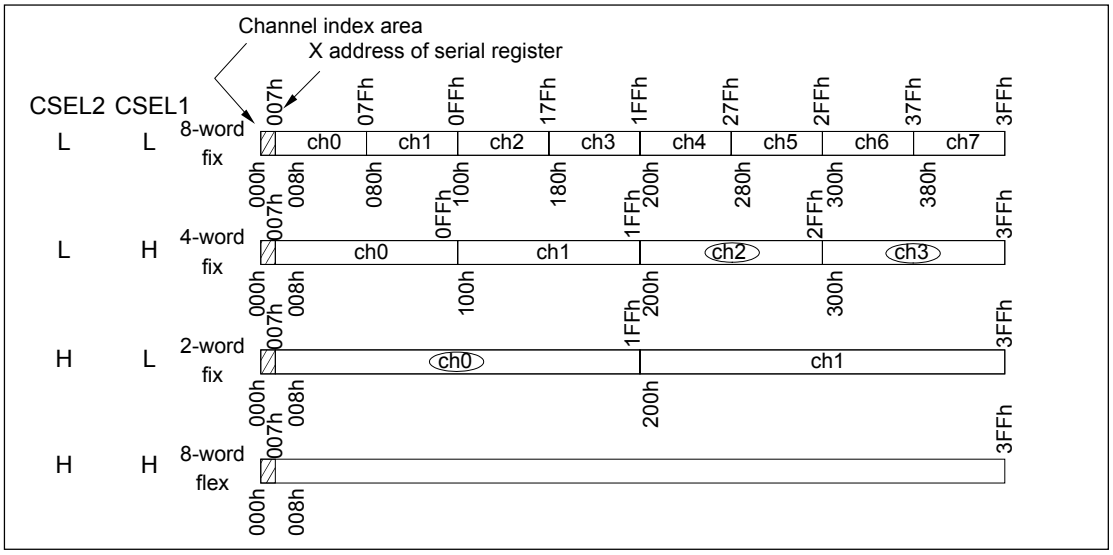
CSEL2	CSEL1	Number of recorded words	CA3	CA2	CA1	Channel
L	L	8-word	L	L	L	ch0
			L	L	H	ch1
			L	H	L	ch2
			L	H	H	ch3
			H	L	L	ch4
			H	L	H	ch5
			H	H	L	ch6
			H	H	H	ch7
L	H	4-word	L	L	—	ch0
			L	H	—	ch1
			H	L	—	ch2
			H	H	—	ch3
H	L	2-word	L	—	—	ch0
			H	—	—	ch1

The relationship between the external serial registers, the number of recorded words and the channel memory capacity is shown in the following table.

CSEL1	CSEL2	Number of recorded words	Channel memory capacity				
			256K bit serial register	512K bit serial register	1 M bit serial register	2M bit serial register	4M bit serial register
L	L	8-word	32K bits (1 second)	64K bits (2 seconds)	128K bits (4 seconds)	256K bits (8 seconds)	512K bits (16 seconds)
L	H	4-word	64K bits (2 seconds)	128K bits (4 seconds)	256K bits (8 seconds)	512K bits (16 seconds)	1M bits (32 seconds)
H	L	2-word	128K bits (4 seconds)	256K bits (8 seconds)	512K bits (16 seconds)	1 M bits (32 seconds)	2M bits (64 seconds)

Note: Numbers in ( ) are recording time of each channel when the bit rate is 32 kbps.

Assignment to channel and channel memory capacity when connecting a 1M bit serial register



By combining CSEL1, CSEL2, CA1, CA2 and CA3, it is possible to assign (the encircled channels) ch0 = 16 seconds, ch2 = 8 seconds and ch3 = 8 seconds (f_{samp} = 8 kHz, 4-bit ADPCM).

Operation in Stand-alone Mode

1. Power down function

Transition to power down mode is selected by the PDMD pin and is summarized as follows:

PDMD pin	Power down operation
L	The IC automatically enters the power down state except during recording/playback.
H	The IC powers down by input of a "L" level to the $\overline{\text{RESET}}$ pin. When the $\overline{\text{RESET}}$ pin = "H" level, the IC is in stand-by mode and the analog circuit is active. When using the built-in LPF with external circuit, select this mode.

During power down, the IC stops oscillating to minimize power consumption and the circuit enters the initialized state.
When using an external clock, input the GND level to the XT pin to reduce power consumption.

2. Master clock frequency and sampling frequency

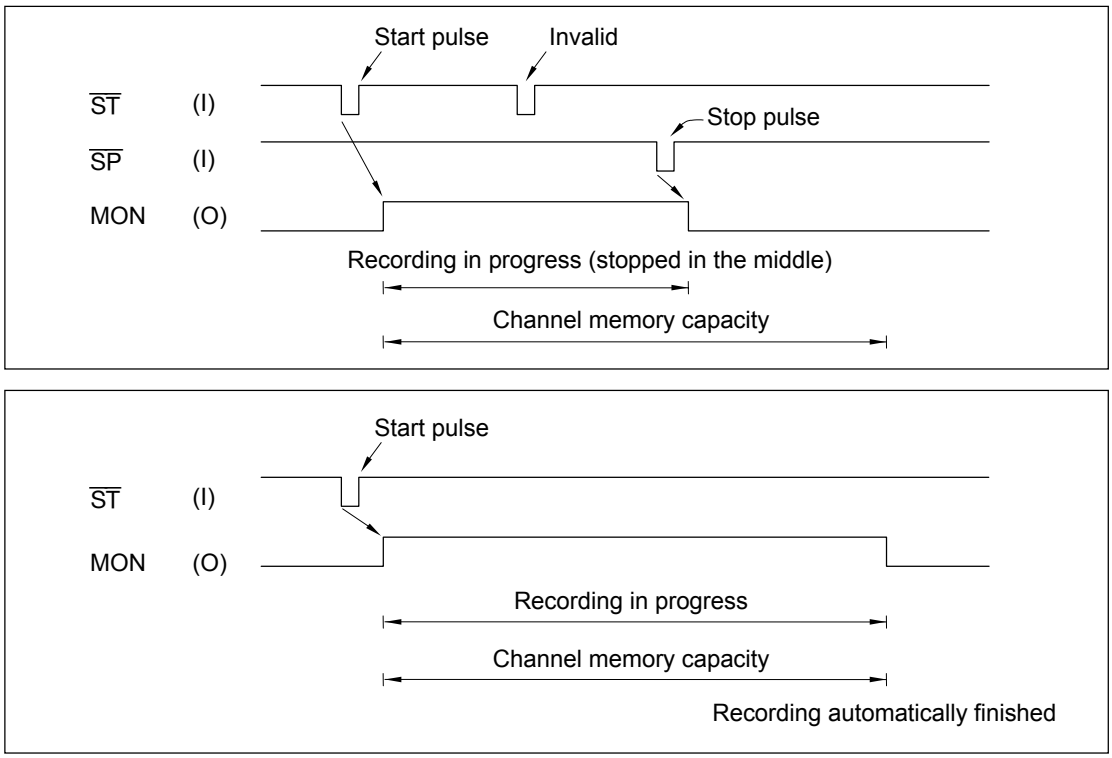
The relationship between the master clock frequency (f_{OSC}) and the sampling frequency (f_{samp}) is summarized in the following table by the SAM pin.

SAM	L	H
f_{samp}	$\frac{f_{OSC}}{768}$ (5.3 kHz)	$\frac{f_{OSC}}{512}$ (8.0 kHz)

Note: Numbers inside ( ) are for master clock frequency f_{OSC} = 4.096 MHz.

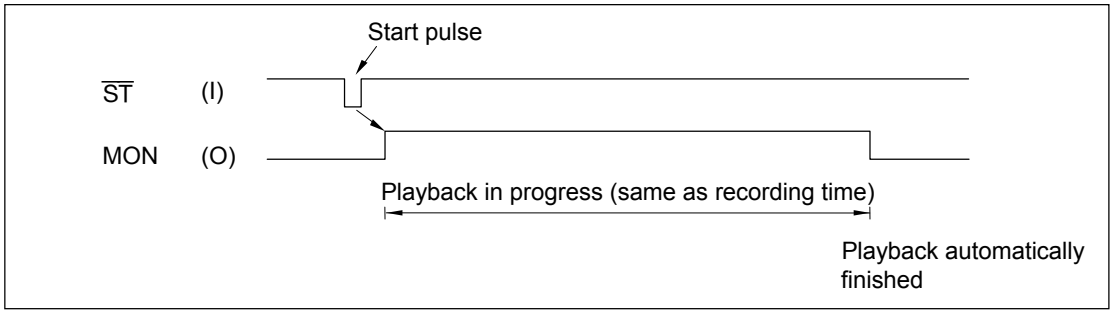
3. Method of recording

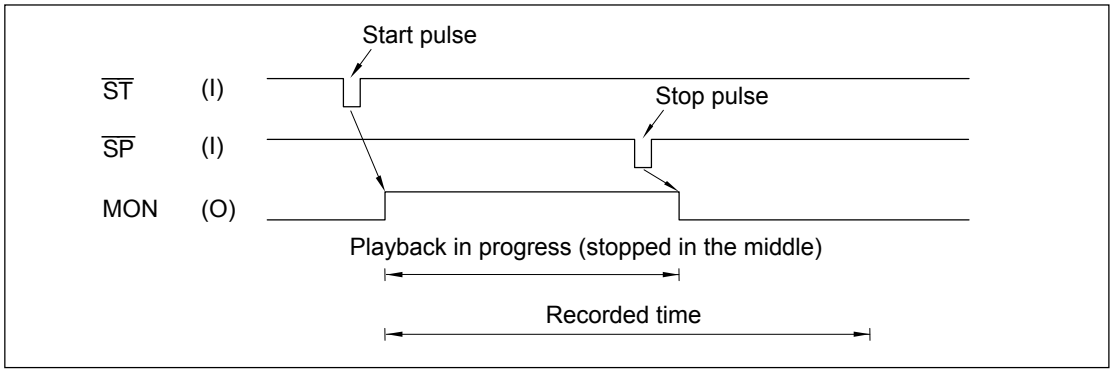
(1) Select the sampling frequency by the SAM pin.
(2) Specify whether the voice triggered starting is used by the VDS pin.
(3) Select the number of words by the CSEL1 and CSEL2 pins and the channel by the CA1, CA2, and CA3 pins.
(4) Input the "H" level to the REC/$\overline{\text{PLAY}}$ pin to set recording mode.
(5) Input a "L" pulse to the $\overline{\text{ST}}$ pin to start recording. To finish recording in the middle, input a $\overline{\text{SP}}$ pulse. The time between these two pulses is recording time.
When recording is started by input of a "L" pulse to the $\overline{\text{ST}}$ pin and continues to the end of the channel memory capacity, the recording is automatically finished at that point.
The MON pin outputs a "H" level during recording.



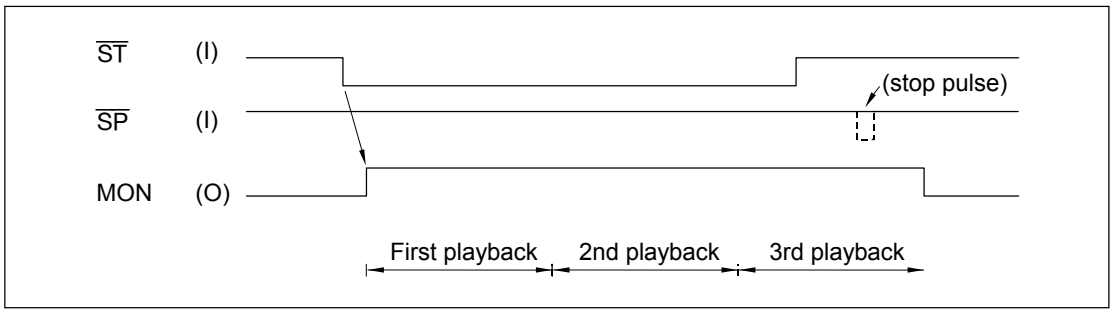
4. Method of playback

(1) Select the sampling frequency by the SAM pin.
(2) Select the number of words by the CSEL1 and CSEL2 pins and the channel by the CA1, CA2 and CA3 pins.
(3) Input a "L" level to the REC/$\overline{\text{PLAY}}$ pin to set playback mode.
(4) Input a "L" level pulse to the $\overline{\text{ST}}$ pin to start playback. When played back for the duration of recorded time, the playback ends automatically.
To stop the playback in the middle, input a "L" level pulse to the $\overline{\text{SP}}$ pin.
The MON pin outputs a "H" level during playback.
Do not start playback in channels not recorded because the playback data and time are undefined. However, playback under these conditions can be halted by a $\overline{\text{SP}}$ pulse.



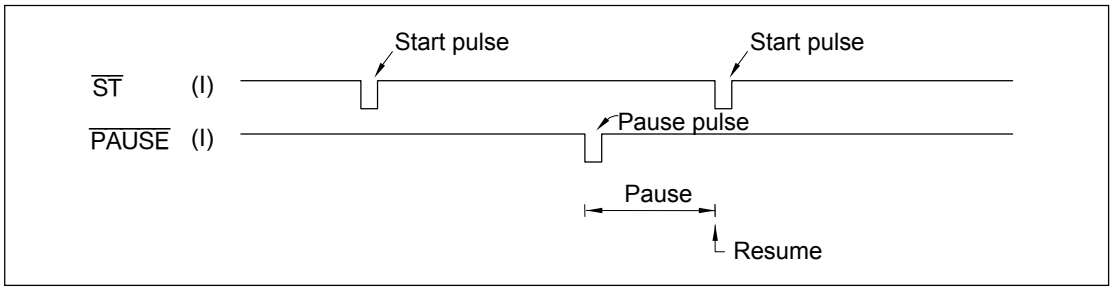


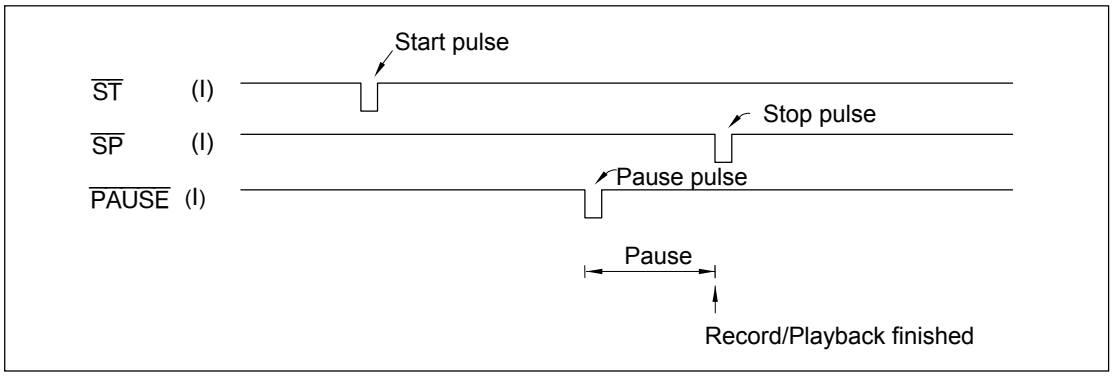
By maintaining the $\overline{\text{ST}}$ pin at "L" level, repeated playback is possible.
Repeated playback is executed only when only one serial register is connected.



5. Method of pause in record/playback

By input of a “L” level pulse to the $\overline{\text{PAUSE}}$ pin during record/playback, input a “L” level pulse to the $\overline{\text{ST}}$ pin. The recording/playback is finished when a “L” level pulse is input to the $\overline{\text{SP}}$ pin.

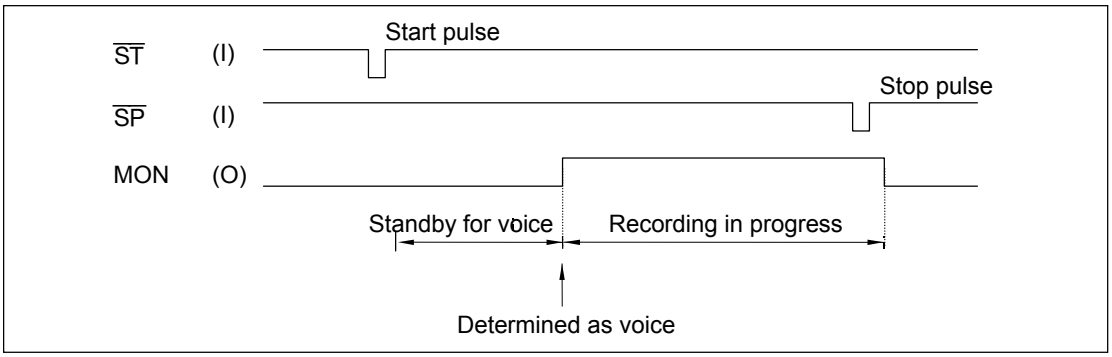




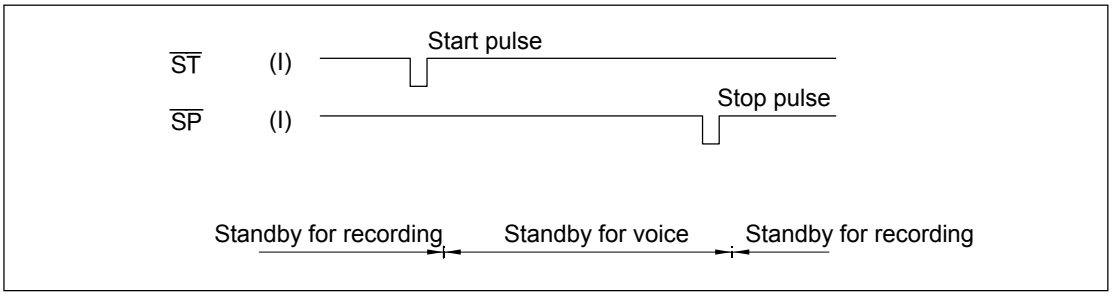
After resuming record/playback, the voice triggered starting circuit does not operate and the recording is resumed when a START pulse is input.

6. Operation in voice triggered starting

By input of a “H” level to the VDS pin, recording by voice triggered starting can be performed. Using the voice triggered starting, the memory capacity can be utilized effectively by eliminating any data prior to voice detection. However, it does not remove silence data during recording.
Input of a $\overline{ST}$ pulse initiates standby for voice and recording is started when voice is detected. The MON pin outputs a “H” level.



When a STOP pulse is input during standby for voice, the standby for voice is finished and the IC enters standby for recording.



7. Method of re-recording

7.1 Fixed mode

In this mode, because the memory area that each channel can use is already assigned, re-recording can by performed without interfering with the contents of other channels. Re-recording can be performed from the beginning similar to a new recording, regardless of the previous recording time.

7.2 Flex mode

In this mode, recording for each channel is started from the address incremented by +1 from the address of preceding channel, ch_{n-1} (if ch0, the header address of the voice data area) and the recording continues until the input of a $\overline{SP}$ pulse. If a $\overline{SP}$ pulse is not input, the recording is continued until the maximum address of the external serial register. This indicates that if the duration of recording is longer than the previously recorded time, it interferes with the contents of proceeding channels.

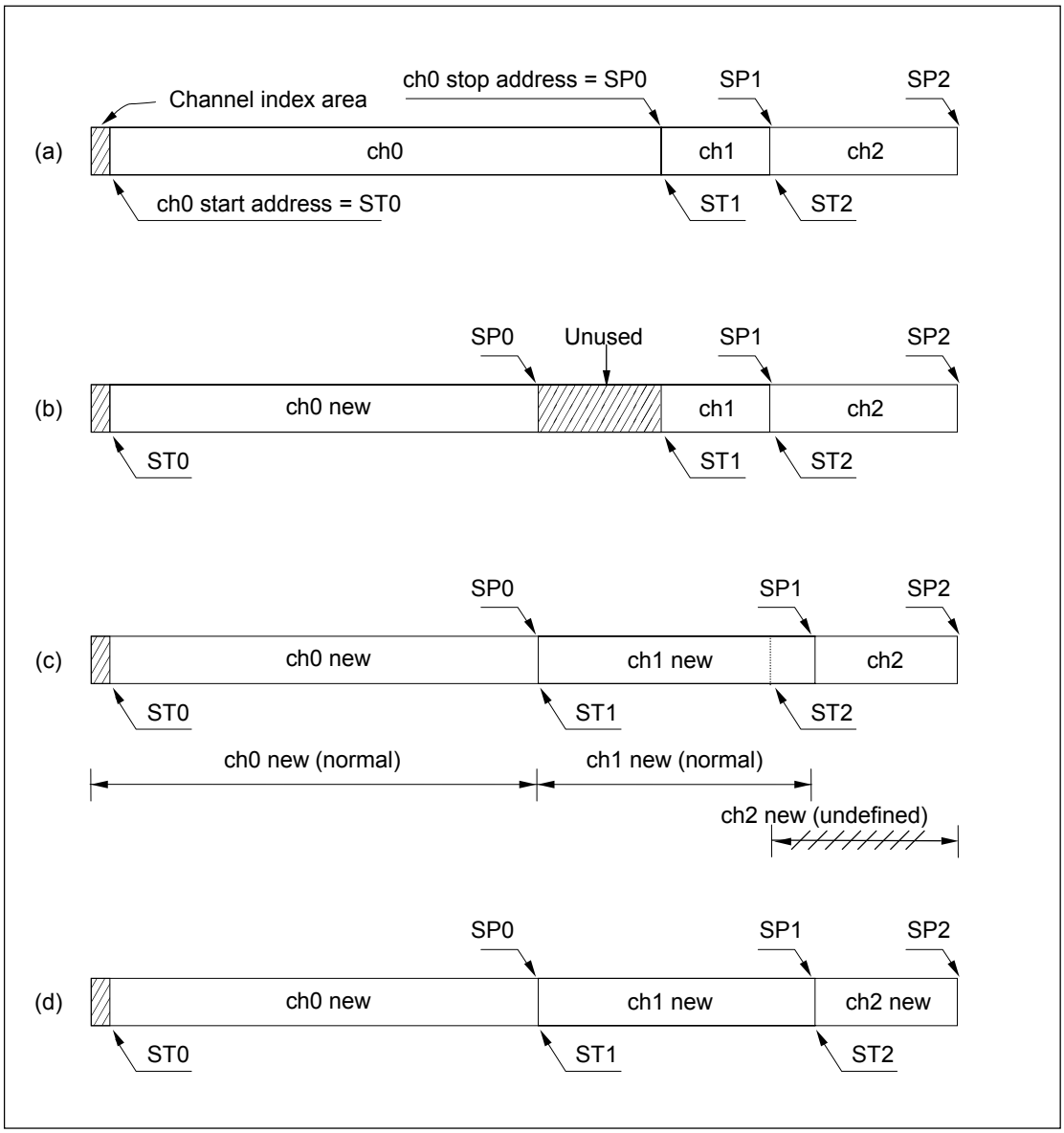
The following shows an example in which the first recording is performed as in Figure (a) and after that each channel is re-recorded.

If the duration of re-recording of ch0 is shorter than the initially recorded time, all the channels function properly as shown in Figure (b).

If the duration of re-recording of ch1 is longer than the initially recorded time and reaches the range of ch2, ch0, and ch1 function properly but the playback data of ch2 becomes undefined as ch2 is played back from the middle of ch1 data.

By re-recording ch2 as shown if Figure (d), ch0-ch2 function properly.

Memory capacity of external serial register



8. Pull-up resistor

In stand-alone mode, a pull-up resistor is connected internally to the $\overline{ST}$, $\overline{SP}$ and $\overline{PAUSE}$ pins. However, the resistor is disconnected during a “L” level input to the $\overline{RESET}$ pin.

Operation in Microcontroller Interface Mode

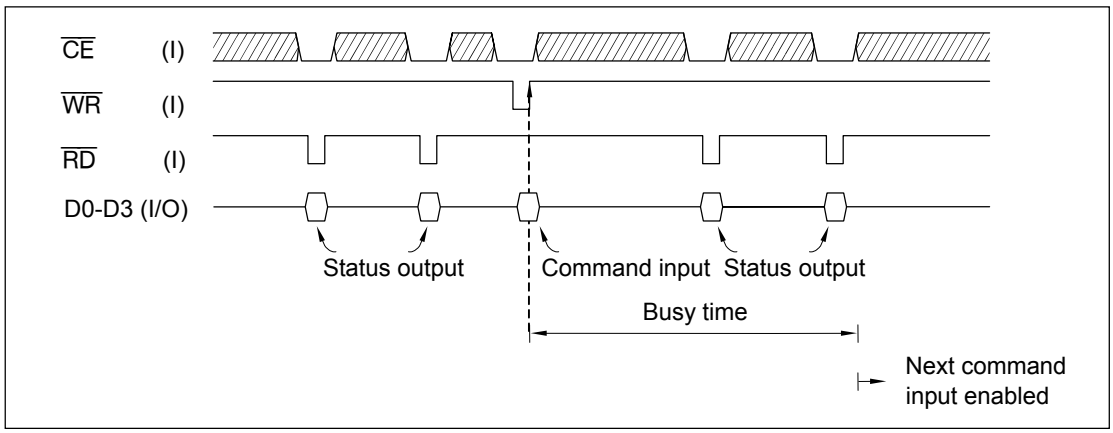
There are 13 data bus commands, D0 to D3 and $\overline{WR}$, $\overline{RD}$ and $\overline{CE}$ which control the MSM6588/6588L in this mode. It has an internal status register so that the state of the LSI can be monitored.

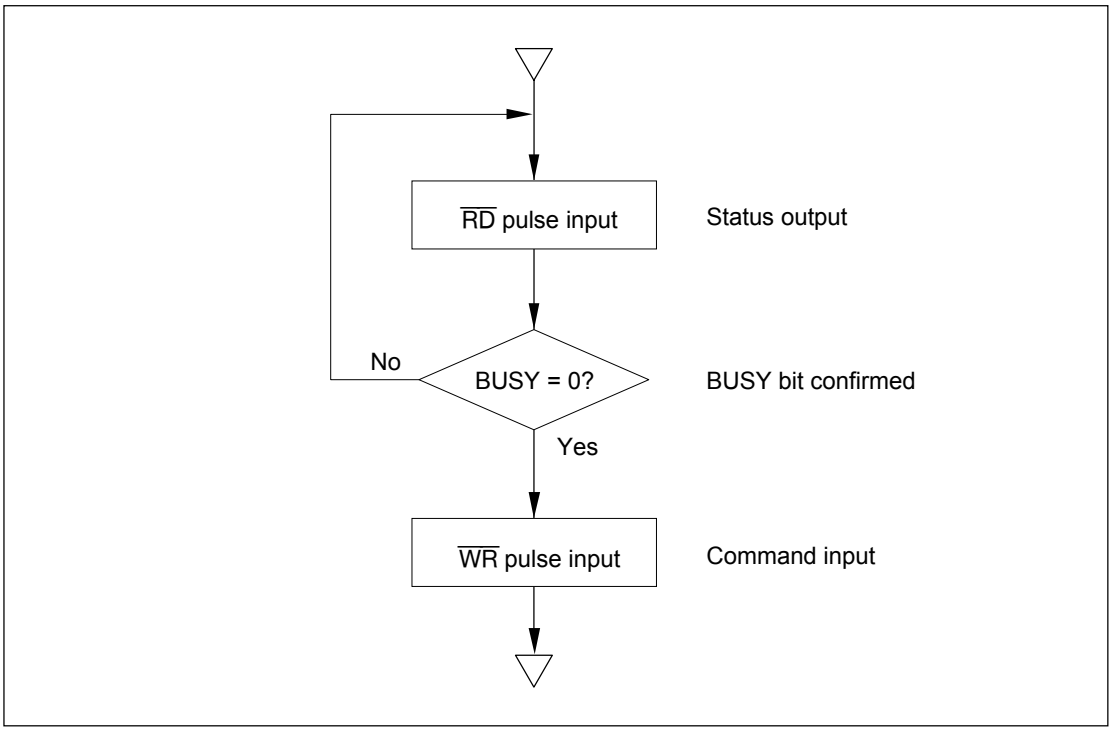
1. Command input method

Input of commands and data can be performed by input of a "L" level ($\overline{WR}$ pulse) during command data input on the D0 to D3-pin.
Input of a "L" level ($\overline{RD}$ pulse), outputs status or data to the D0 to D3-pin.
The $\overline{CE}$ pin controls enable/disable of the $\overline{WR}$ and $\overline{RD}$ pulses. Input of a "L" level enables $\overline{WR}$ and $\overline{RD}$ pulses, while a "H" level disables $\overline{WR}$ and $\overline{RD}$ pulses and D0 to D3 become high-impedance. When using the D0 to D3-pin with the MSM6588/6588L alone, the $\overline{CE}$ pin can be fixed at the "L" level.

1.1 Input method of 1 nibble command

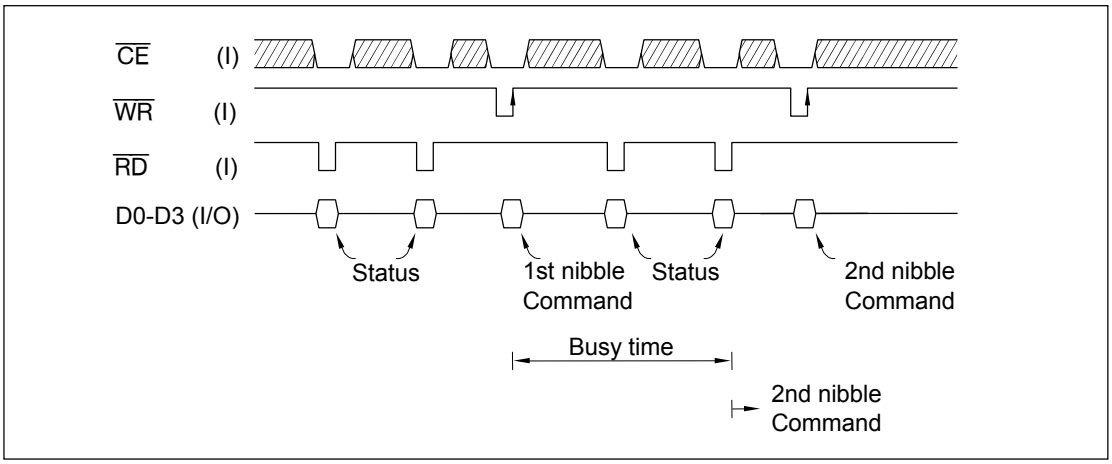
(1) Input a $\overline{RD}$ pulse to fetch the contents of the status register and make sure that the BUSY bit is 0. When it is 1, repeat input of $\overline{RD}$ pulses until it becomes 0.
(2) Send a command to the D0 to D3-pin to input a $\overline{WR}$ pulse.
(3) Confirm that it is not BUSY state as in (1) during input of the next command. Alternatively, wait for the duration of the BUSY time.

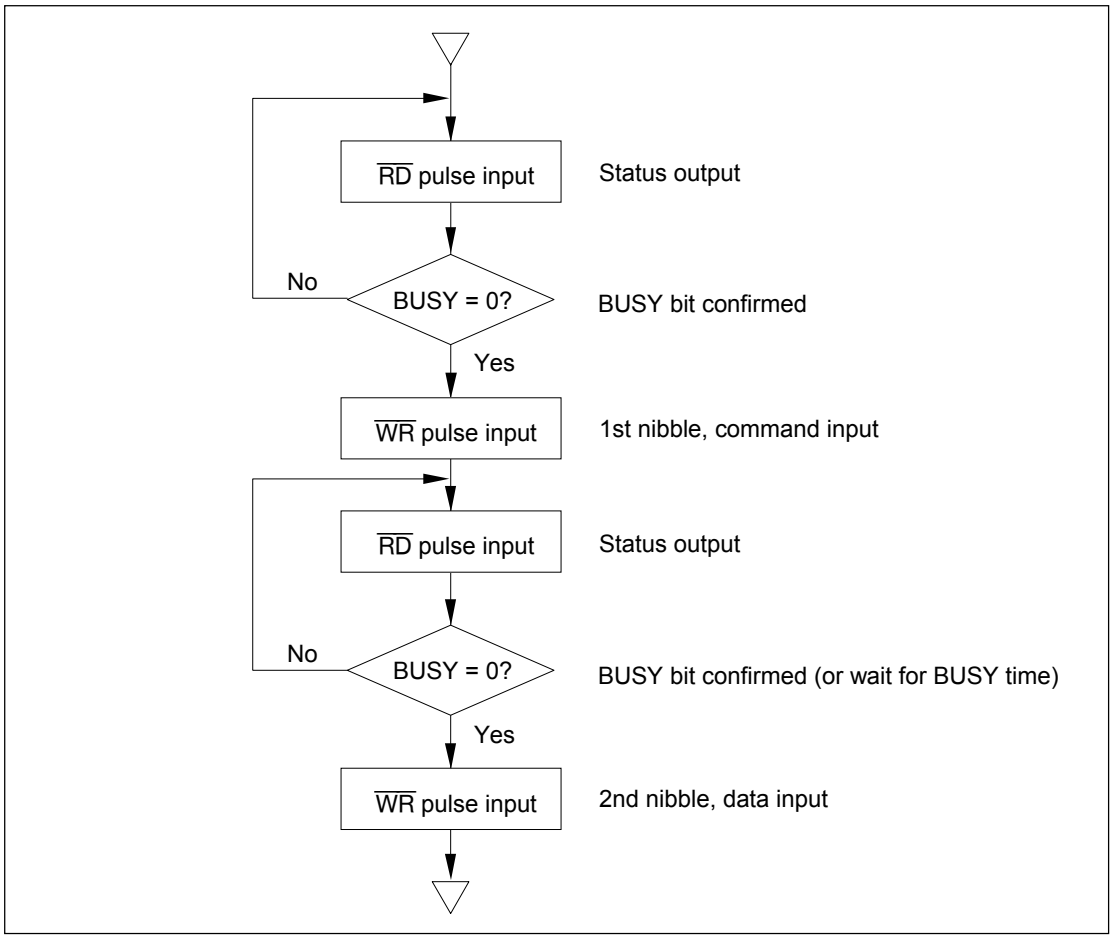




1.2 Input method of 2 nibble command

(1) Input a $\overline{RD}$ pulse to confirm the BUSY bit.
(2) Send a command to the D0 to D3-pin to input an $\overline{WR}$ pulse.
(3) Input a $\overline{RD}$ pulse and wait until the BUSY bit becomes 0. Alternatively, wait for the duration of the BUSY time.
(4) Set data to the D0 to D3-pin to input a $\overline{WR}$ pulse.




RD pulse input
Status output
No
BUSY = 0?
BUSY bit confirmed
Yes
WR pulse input
1st nibble, command input
RD pulse input
Status output
No
BUSY = 0?
BUSY bit confirmed (or wait for BUSY time)
Yes
WR pulse input
2nd nibble, data input

2. Explanation of commands

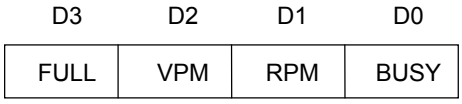
Command	Code				Function of commands
	D3	D2	D1	D0	
NOP	0	0	0	0	(NON OPERATION) no function
PAUSE	0	0	0	1	(PAUSE) Suspends record/playback temporarily.
PLAY	0	0	1	0	(PLAYBACK) Sets playback mode.
REC	0	0	1	1	(RECORD) Sets recording mode.
START	0	1	0	0	(START) Starts record/playback.
STOP	0	1	0	1	(STOP) Stops record/playback. In record mode, the contents of the address counter are stored in the channel index area as the stop address.
SAMP	0	1	1	0	(SAMPLING FREQUENCY) Specifies the sampling frequency and control mode with the following (1) nibble.
CHAN	0	1	1	1	(CHANNEL) Specifies the channel and control mode with the following (1) nibble.
ADRWR	1	0	0	0	(ADDRESS WRITE) In direct mode, stores the start address and the stop address to the channel index area with the following (8) nibbles.
ADRRD	1	0	0	1	(ADDRESS READ) Reads out the start address and the stop address stored in the channel index area by reading of the following (8) nibbles. During this operation, the contents of the status register cannot be read.
DTRW	1	0	1	0	(DATA READ WRITE) Transfers data to the external serial registers through the data bus with preset timing.
EXT	1	0	1	1	(EXTERNAL) Performs record/playback by input and output of ADPCM data through the data bus by preset timing. Use this command when using SRAM or a hard disk as storage media of voice data. Does not control the external serial registers nor addresses.
VDS	1	1	0	0	(VOICE DETECT SELECT) Selects the voice triggered starting condition and the bit length of ADPCM with the following (1) nibble.

Command List

Command	1st nibble command				2nd nibble command				Note
					D3	D2	D1	D0	
NOP	0	0	0	0	—				1 nibble command
PAUSE	0	0	0	1	—				1 nibble command
P LAY	0	0	1	0	—				1 nibble command
REC	0	0	1	1	—				1 nibble command
START	0	1	0	0	—				1 nibble command
STOP	0	1	0	1	—				1 nibble command
SAMP	0	1	1	0	CSEL2	CSEL1	SA1	SA0	2 nibble command CSELn…control mode SAn…sampling freq
CHAN	0	1	1	1	RCON	CA3	CA2	CA1	2 nibble command RCON…control mode CAn…channel
ADRWR	1	0	0	0	Inputs address data (2nd-9th nibble)				9 nibble command
ADRRD	1	0	0	1	Outputs address data (2nd-9th nibble)				9 nibble command
DTRW	1	0	1	0	—				Transfers data by preset timing
EXT	1	0	1	1	—				Records/plays back by preset timing
VDS	1	1	0	0	—	BIT	VD1	VD0	2 nibble command BIT…ADPCM bit length VDn…Voice triggered starting condition

3. Explanation of status register

The status register is a 4-bit register and outputs the current state to the D0 to D3 pin by input of a “L” level to the $\overline{RD}$ pin.
However, the contents of the status register cannot be read during the execution of ADRRD or during record/playback by the EXT command.



Status register

(1) BUSY
“H” level of this bit indicates that the $\overline{RESET}$ operation is in progress or a command is being processed. Do not issue commands at this time.
(2) RPM
This bit becomes “H” level during recording or playback. Do not issue commands except the STOP command, PAUSE command and START command after release of pause.
(3) VPM
This bit becomes “H” level when 1) standby for voice after voice triggered recording is started and 2) suspending recording/playback by the PAUSE command.
(4) FULL
This status is used for recording in a flex mode. This bit is set to a “H” level when recording is through to the end of the channel capacity which is maximum address of the serial register connected to MSM6588/6588L. It is reset when either a REC command, PLAY command or START command is input. After recording in flex mode, start recording of the next channel after confirming the FULL bit.

BUSY Condition		BUSY Status Bit	Duration of BUSY
After releasing $\overline{\text{RESET}}$		Enable	125 μs (Note 3)
After input of 1nibble command		Enable	16 μs
After input of 2 nibble command		Enable	16 μs
After input of data of 2 nibble command		Enable	16 μs
After input of the ADRWR command		Enable	270 μs
After input of address data of the ADRWR command		Enable	50 μs
After input of the ADRRD command		Disable	270 μs
After output address data of the ADRRD command		Disable	50 μs
During execution of the DTRW command	After input of the DTRW command	Enable	16 μs
	After input of lower 4-bit of address	Enable	16 μs
	After input of middle 4-bit of address	Enable	16 μs
	After input of upper 4-bit of address	Enable	270 μs
	After input of the REC command	Enable (Note 2)	16 μs
	After input of write-in data	Enable (Note 2)	50 μs
	After input of the PLAY command	Disable	50 μs
	After input of the STOP command	Enable (Note 2)	50 μs

Notes: 1. The duration of BUSY is proportional to the period of the sampling frequency (f_{samp}).
2. When enabling only the data write access after input of the DTRW command, the BUSY state can be confirmed by the BUSY bit.
3. The oscillation stable time is added to the duration of BUSY after releasing $\overline{\text{RESET}}$.
The oscillation stable time is several tens of milliseconds for crystal oscillators and is several hundreds of microseconds for ceramic oscillators.

4. Selection of sampling frequency (SAMP command)

Data that follows the SAMP command will select the sampling frequency.
The relationship between the master clock oscillation frequency (f_{OSC}) and the sampling frequency (f_{samp}) is shown in the following table using data bits SA1 and SA0.

SA1	SA0	Sampling frequency (f_{samp})
0	0	f_{OSC}/1024 (4.0 kHz)
0	1	f_{OSC}/768 (5.3 kHz)
1	0	f_{OSC}/640 (6.4 kHz)
1	1	f_{OSC}/512 (8.0 kHz)

Note: Numbers in ( ) are for master clock frequency f_{OSC} = 4.096 MHz.

5. Recording control modes (SAMP and CHAN commands)

In microcontroller interface mode, there are three record control modes. They are direct, fixed, and flex mode. Control mode selection is performed by data bit RCON of the CHAN command and data bits CSEL1 and CSEL2 of the SAMP command.

RCON	CSEL2	CSEL1	Number of record words	Control mode
0	—	—	8-word	Direct mode
1	0	0	8-word	Fixed mode
	0	1	4-word	
	1	0	2-word	
	1	1	8-word	Flex mode

(1) Direct mode
The start and stop addresses of each channel are input directly to the channel index area using the ADRWR command from a microcontroller. This means that the assignment of memory capacity for each channel is controlled by the microcontroller.

(2) Fixed mode
The start and stop addresses of each channel are input indirectly to the channel index area by channel selection from a microcontroller. Memory capacity of each channel is assigned by equally dividing the memory capacity of the external serial register by the number of recording words.

(3) Flex mode
The start and stop addresses of each channel are input indirectly to the channel index area by channel selection from a micro-controller. There is no assignment of memory capacity of each channel so that the recording time for each channel can be set arbitrarily.
Refer to the Recording Control Modes on each mode description. In the meantime, since the method of re-recording for the fixed and flex modes is the same as that of the stand-alone mode, refer to Item 7, Method of re-recording for the stand-alone mode.

6. Selection of channel (CHAN command)

6.1 Channel selection in direct mode and in flex mode

CA3	CA2	CA1	Channel
0	0	0	ch0
0	0	1	ch1
0	1	0	ch2
0	1	1	ch3
1	0	0	ch4
1	0	1	ch5
1	1	0	ch6
1	1	1	ch7

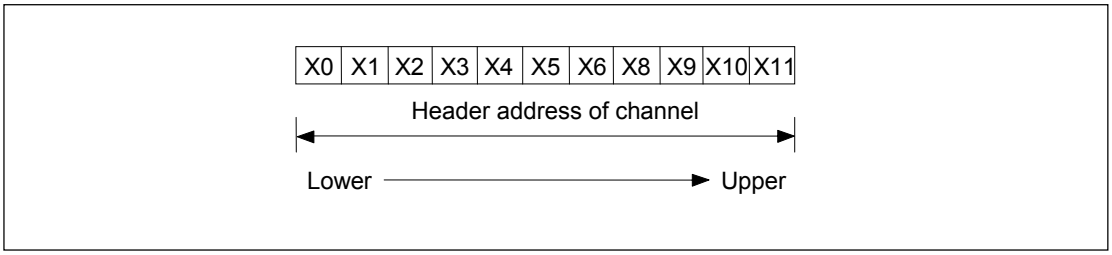
6.2 Channel selection in fixed mode

CSEL2	CSEL1	Number of recorded words	CA3	CA2	CA1	Channel
0	0	8-word	0	0	0	ch0
			0	0	1	ch1
			0	1	0	ch2
			0	1	1	ch3
			1	0	0	ch4
			1	0	1	ch5
			1	1	0	ch6
			1	1	1	ch7
0	1	4-word	0	0	—	ch0
			0	1	—	ch1
			1	0	—	ch2
			1	1	—	ch3
1	0	2-word	0	—	—	ch0
			1	—	—	ch1

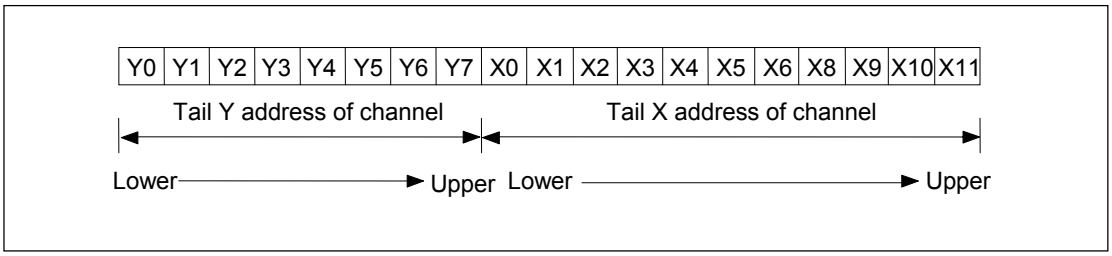
7. Input/output of start and stop address (ADRWR and ADRRD commands)

When recording in direct mode, the start and stop addresses of each channel are directly input to the channel index area by the ADRWR command.
The start address consists of 12 bits and the stop address consists of 20 bits. They denote the header and tail addresses of the channel, respectively.

Start address STn



Stop address SPn



The X addresses of the voice data area are 008h-FFFh (when connecting the serial register for 4M bit).
The tail Y address changes depending on the ADPCM bit length, the range that can be specified is 00h-A9h (for 3-bit ADPCM) and 00h-7Fh (for 4-bit ADPCM). For ordinary recording, A9h or 7Fh (tail address) should be input as the tail Y address.
The ADPCM and ADRRD commands input the start and stop address after issuing the commands with the following 8 nibble data.

	D3	D2	D1	D0	Contents
1st nibble	1	0	0	0	ADRWR command
2nd nibble	Y3	Y2	Y1	Y0	Stop address (Y address)
3rd nibble	Y7	Y6	Y5	Y4	
4th nibble	X3	X2	X1	X0	Stop address (X address)
5th nibble	X7	X6	X5	X4	
6th nibble	X11	X10	X9	X8	
7th nibble	X3	X2	X1	X0	Start address (X address)
8th nibble	X7	X6	X5	X4	
9th nibble	X11	X10	X9	X8	

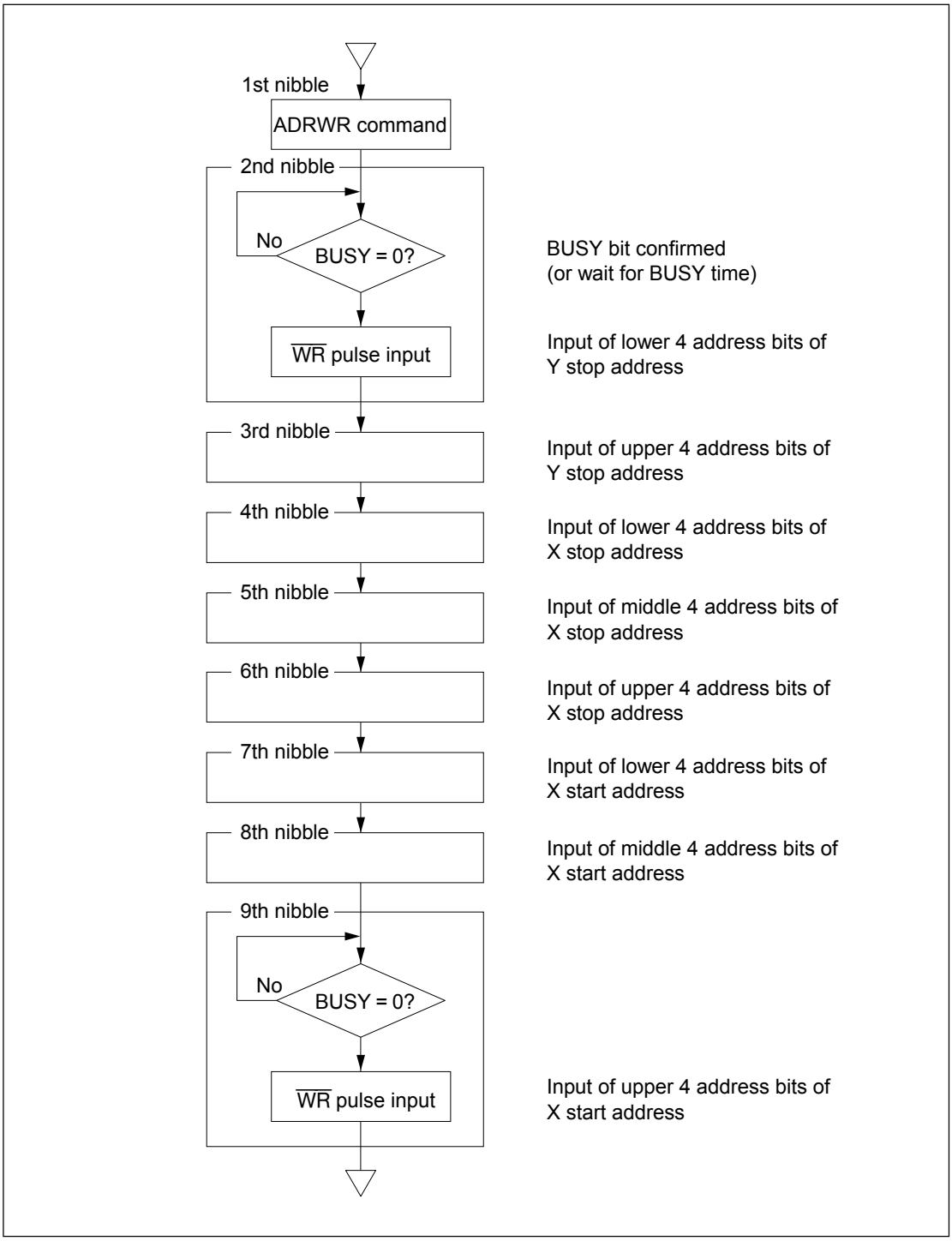
7.1 Input method of address data by the ADRWR command

(1) After confirming the BUSY bit, input the ADRWR command.
(2) After confirming the BUSY bit or waiting for the BUSY time period, input the lower 4 bits (Y3, Y2, Y1, Y0) of the Y stop address. This operation is to be repeated for 8 times to input the stop and start address.

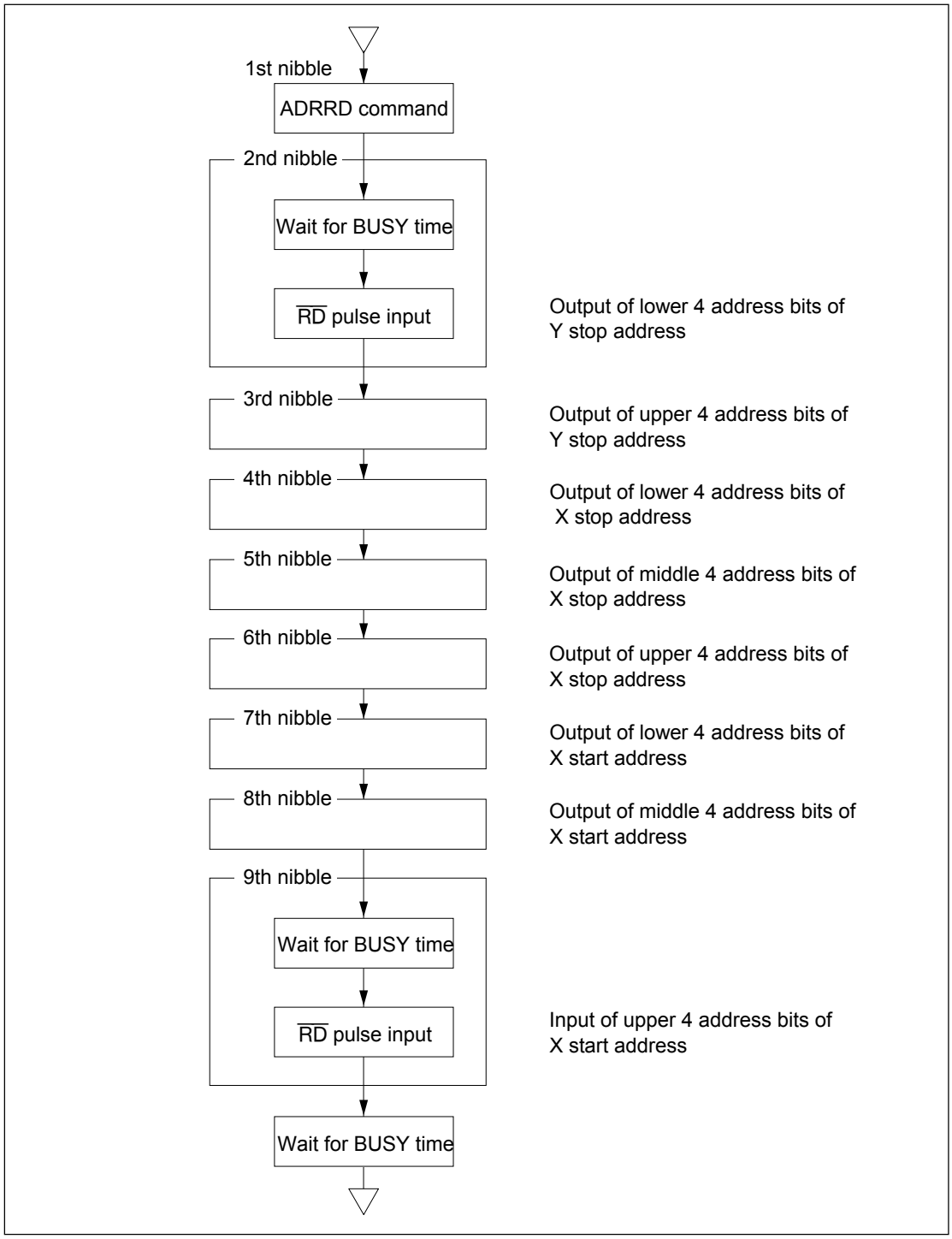
7.2 Output method of address data by the ADRRD command

(1) After confirming the BUSY bit, input the ADRRD command.
(2) Wait for the BUSY time period and input a $\overline{RD}$ pulse to output the address data from the data bus. This operation is to be repeated for 8 times to get the stop and start address to the microcontroller.
(3) After input of the ninth nibble $\overline{RD}$ pulse, the next command is enabled after waiting for the BUSY time period. During the execution of the ADRRD command, the contents of the status register cannot be confirmed. It is necessary to wait for the BUSY time period between each $\overline{RD}$ pulse.

ADRWR Command Flow Chart



ADRRD Command Flow Chart



8. Specifying ADPCM bit length (VDS command)

The ADPCM bit length is specified by the VDS command data (bit).

BIT	ADPOM bit length
0	3-bit
1	4-bit

9. Specifying voice triggered starting mode (VDS command)

Specify whether voice triggered starting is used and the voice detection level by the VDS command data bits (VD0 and VD1).

VD1	VD0	Voice detection level V_{VDS}	
		MSM6588 (5 V version)	MSM6588L (3 V version)
0	0	Voice triggered starting disabled	Voice triggered starting disabled
0	1	$\pm V_{DD}/64$ (±80 mV) *	$\pm V_{DD}/128$ (±24 mV) **
1	0	$\pm V_{DD}/32$ (±160 mV) *	$\pm V_{DD}/64$ (±48 mV) **
1	1	$\pm V_{DD}/16$ (±320 mV) *	$\pm V_{DD}/32$ (±96 mV) **

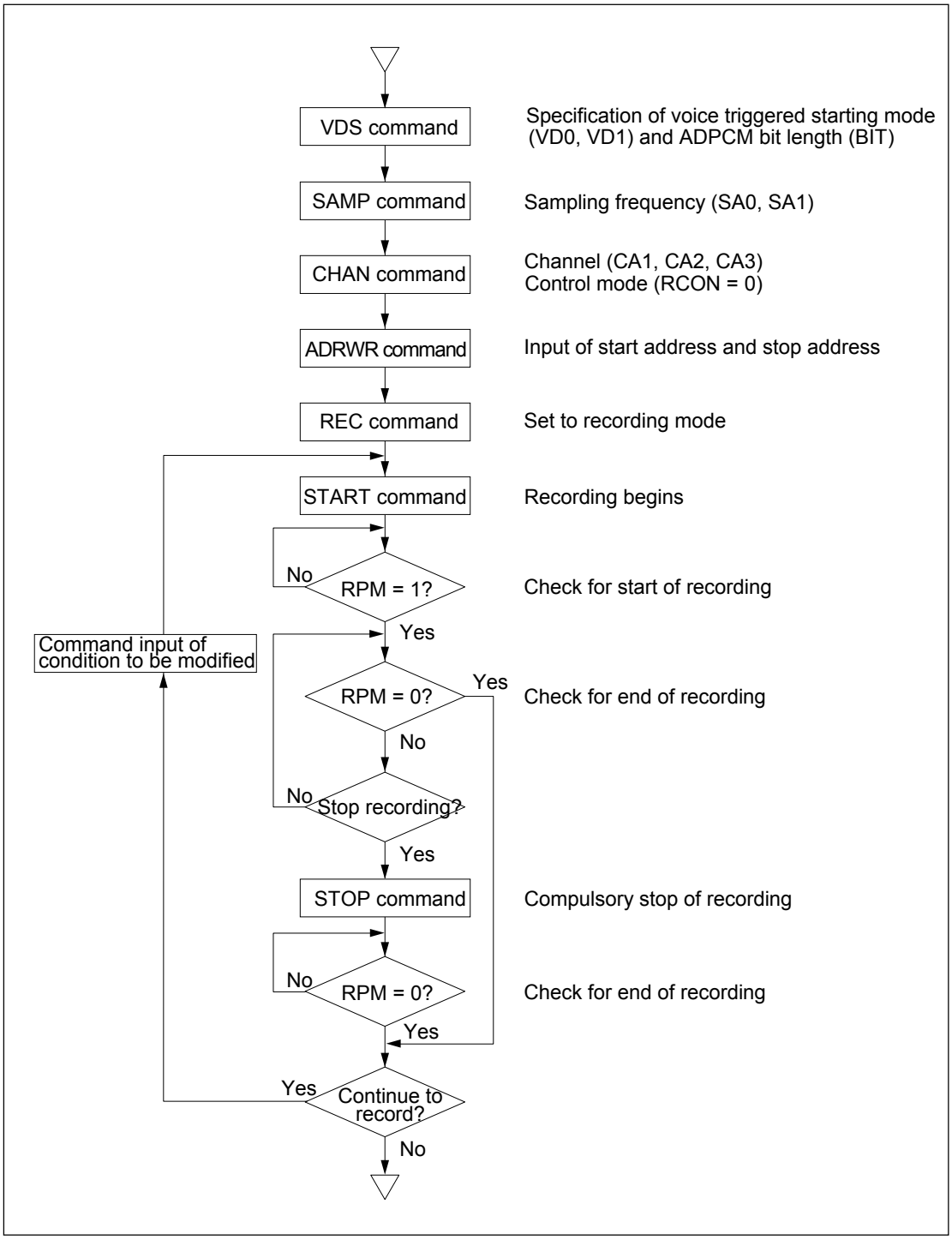
* Values in parentheses are for V_{DD} = 5.12 V.
** Values in parentheses are for V_{DD} = 3.072 V.

10. Recording method

10.1 Recording in direct mode

(1) Input the VDS command. Specify whether voice triggered starting is used and voice detection level using VD1 and VD0, set the ADPCM bit length by use of the BIT data.
(2) Input the SAMP command. Specify the sampling frequency by SA0 and SA1 data. In direct mode, CSEL1 and CSEL2 data are ignored.
(3) Input the CHAN command. Specify the channel by CA1, CA2 and CA3 data. By setting RCON data to 0, the control mode is set to the direct mode.
(4) Input the start address and stop address with the ADRWR command to specify the memory area to record into. The address data is stored in the channel index area.
(5) Input the REC command to set recording mode.
(6) Input the START command to begin recording. At this time, the IC fetches the start address and the stop address of the specified channel from the channel index area and starts recording after storing them to the address counter and the stop address register.
(7) When the contents of the address counter and the stop address register corresponds, the recording is finished. The end of recording is confirmed by the RPM bit of the status register.
(8) If the recording needs to be suspended temporarily, input the STOP command. The contents of the address counter become the new stop address and are automatically stored in the channel index area.
When finishing recording by the STOP command, input the next command after confirming that the recording operation is finished using the RPM bit.
(9) If recording is to be continued, specify the condition to be modified by (1)-(4).

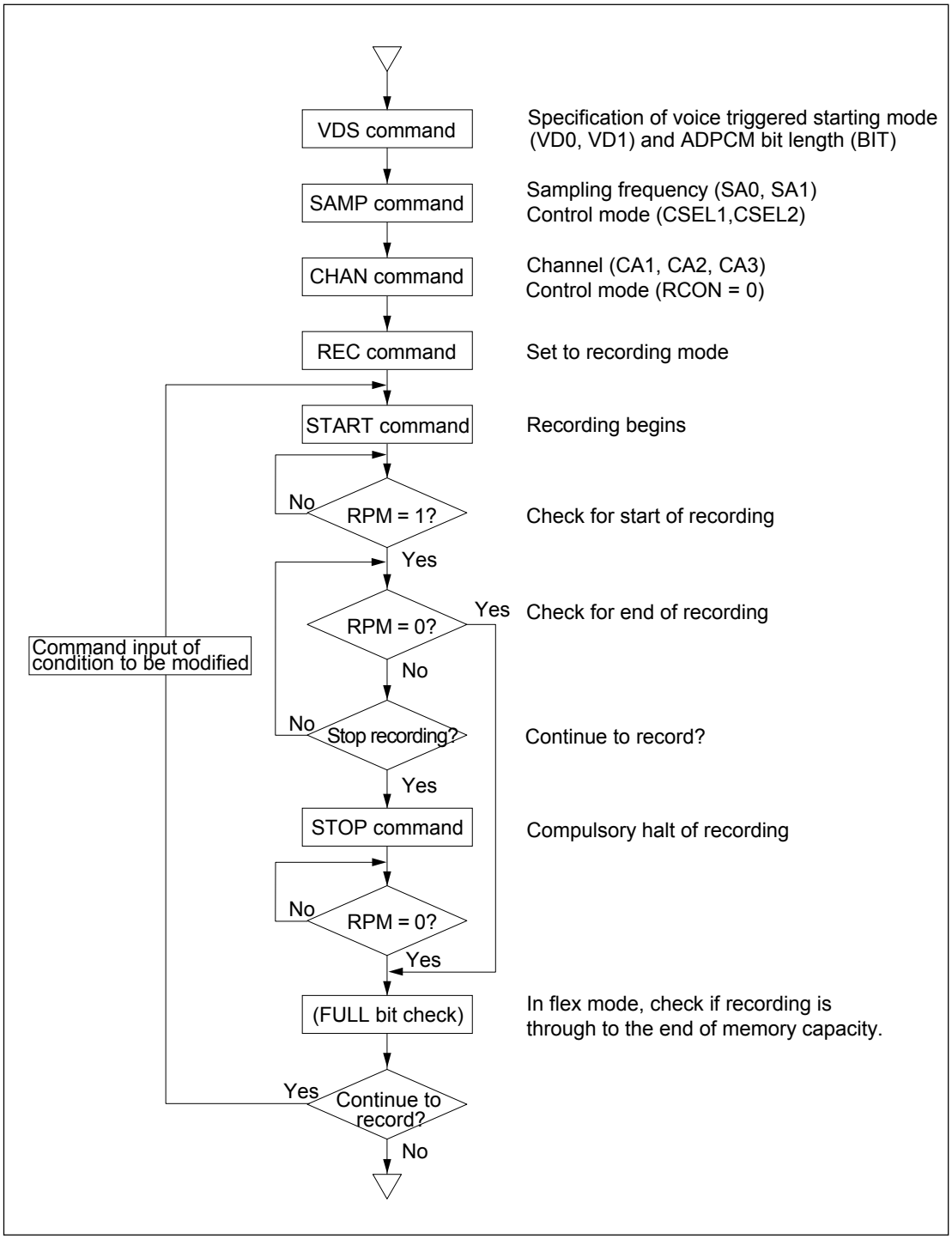
Flowchart of Recording in Direct Mode



10.2 Recording method in the fixed and flex modes

(1) Input the VDS command. Specify whether voice triggered starting is used and voice detection level with data bits VD0 and VD1. Specify the ADPCM bit length with the VDS command data (BIT).
(2) Input the SAMP command. Specify the sampling frequency with SA0 and SA1 data and control mode with CSEL1 and CSEL2 data.
(3) Input the CHAN command. Specify the channel with CA1, CA2 and CA3 data. The control mode selection data (RCON) is set to 1.
(4) Input the REC command to set the recording mode.
(5) Start recording by input of the START command.
In fixed mode, recording is begun after storing the start and stop address generated inside the IC to the address counter and the stop address register respectively, and to the channel index area.
In flex mode, the start address is incremented by +1 from the address of preceding channel (ch_{n-1}) fetched from the channel index area.
The stop address is the last address of external serial register. Recording is begun after storing each address to the address counter, the stop address register and the channel index area.
(6) When the contents of the address counter and the stop address register corresponds, recording is finished. The end of recording is confirmed by the RPM bit of the status register.
(7) If recording is to be suspended temporarily, input the STOP command. The contents of the address counter become the new stop address and are automatically stored in the channel index area.
After finishing recording using the STOP command, input the next command after confirming that the recording operation is finished using the RPM bit.
(8) In flex mode, make sure that the recording is finished to the end of the memory capacity by checking the FULL bit of the status register. If recording is completed to the end of memory, it is not possible to the next channel (ch_{n+1}).
(9) If recording is to be continued, specify the condition to be modified by (1)-(3).

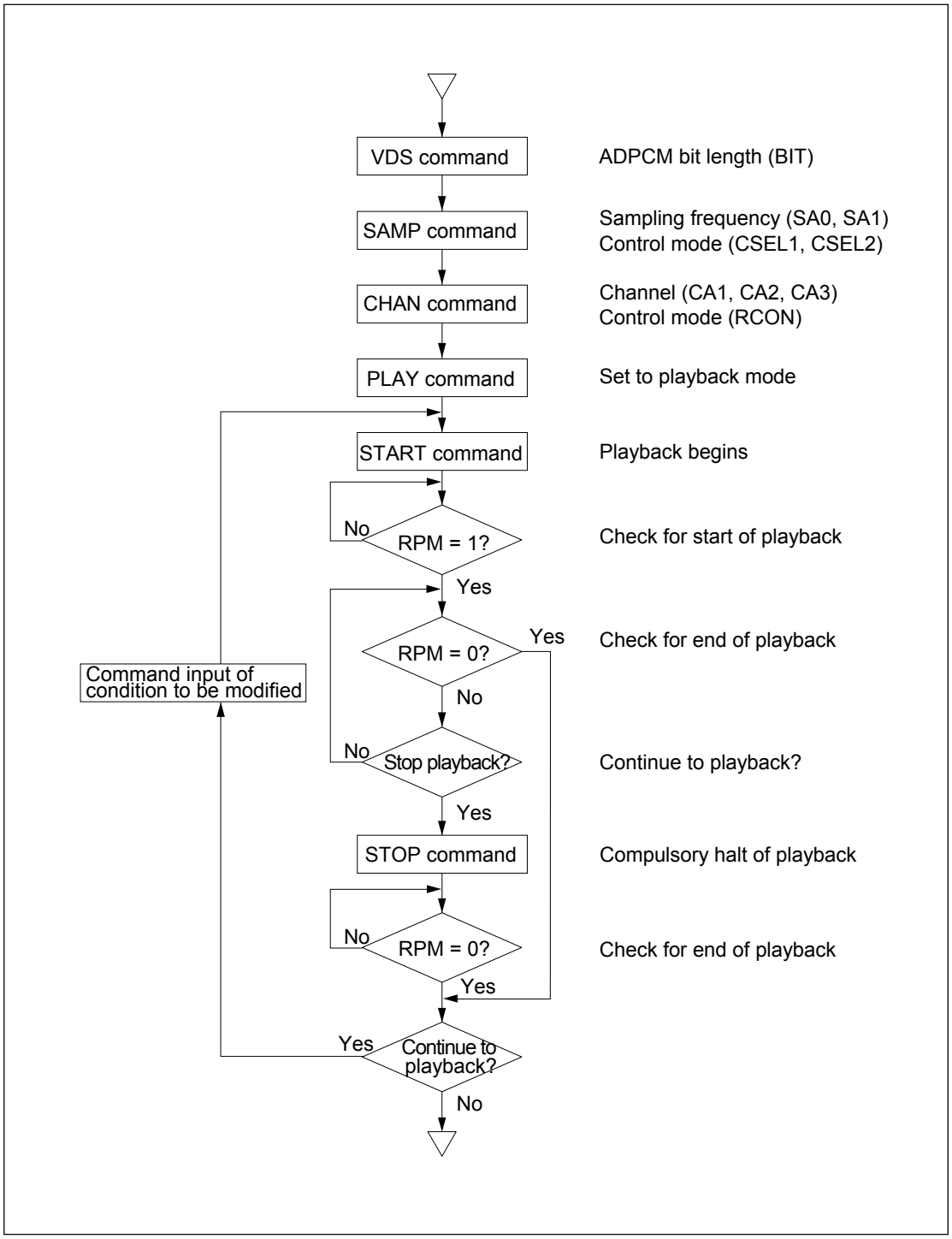
Flowchart of Recording in Fixed and Flex Modes



11. Playback method

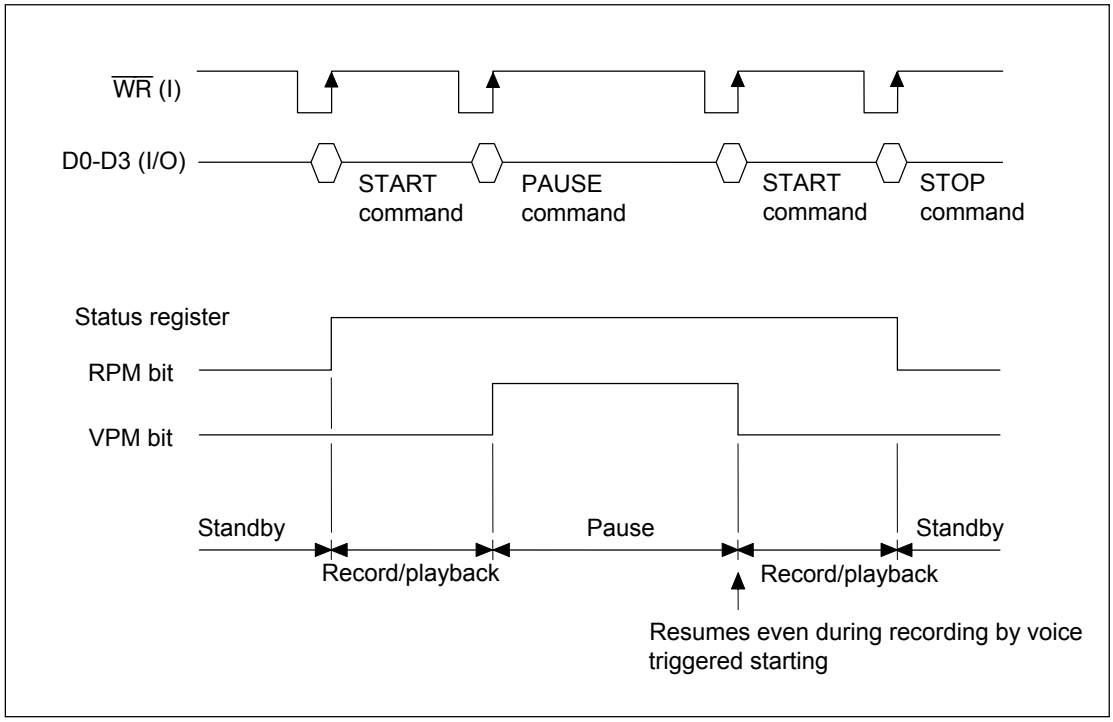
(1) Input the VDS command. Specify the ADPCM bit length using the VDS command data (BIT). VD0 and VD1 data for voice detection are invalid in playback mode.
(2) Input the SAMP command. Specify the sampling frequency using SA0 and SA1 data and the control mode using CSEL1 and CSEL2 data.
(3) Input the CHAN command. Specify the channel using CA1, CA2 and CA3 and specify the control mode during recording using the RCON data bit. Channel selection during playback can be specified randomly in either control mode.
(4) Input the PLAY command to set playback mode.
(5) Start playback by input of the START command.
The IC fetches the start and stop addresses of the specified channel from the channel index area and stores each to the address counter and the stop address register to begin playback.
(6) When the contents of the address counter and the stop address register corresponds, playback is finished. The end of playback is confirmed by the RPM bit of the status register.
(7) If playback is to be suspended temporarily, input the STOP command. After finishing playback using the STOP command, input the next command after confirming that the recording operation is finished using the RPM bit.
(8) If recording is to be continued, specify the condition to be modified by (1)-(3).

Flowchart of Playback

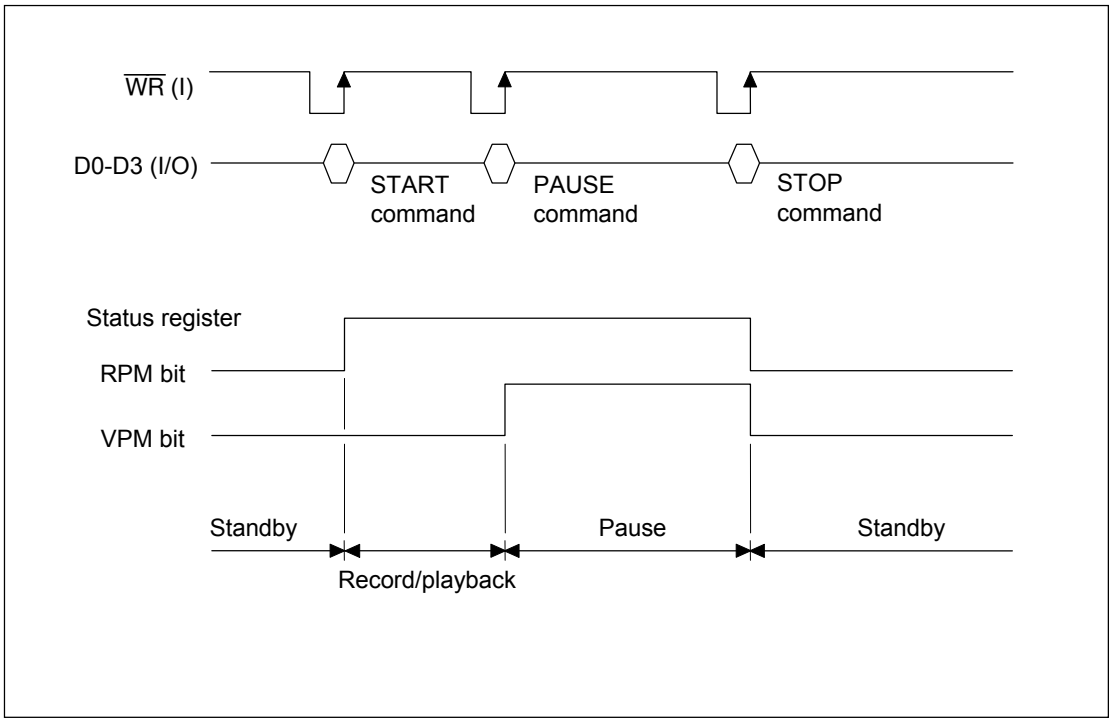


12. Pause method (temporary suspension) with the (PAUSE command)

Record/playback is suspended temporarily by input of the PAUSE command and is resumed by input of the START command. During pause, the VPM bit of the status register is 1 and the RPM bit is 1.
Even when recording is done with voice triggered starting activated, input of the START command during pause resumes recording even in no-voice detected state.
During standby for record/playback, pause, and standby for voice, the PAUSE command is invalid.

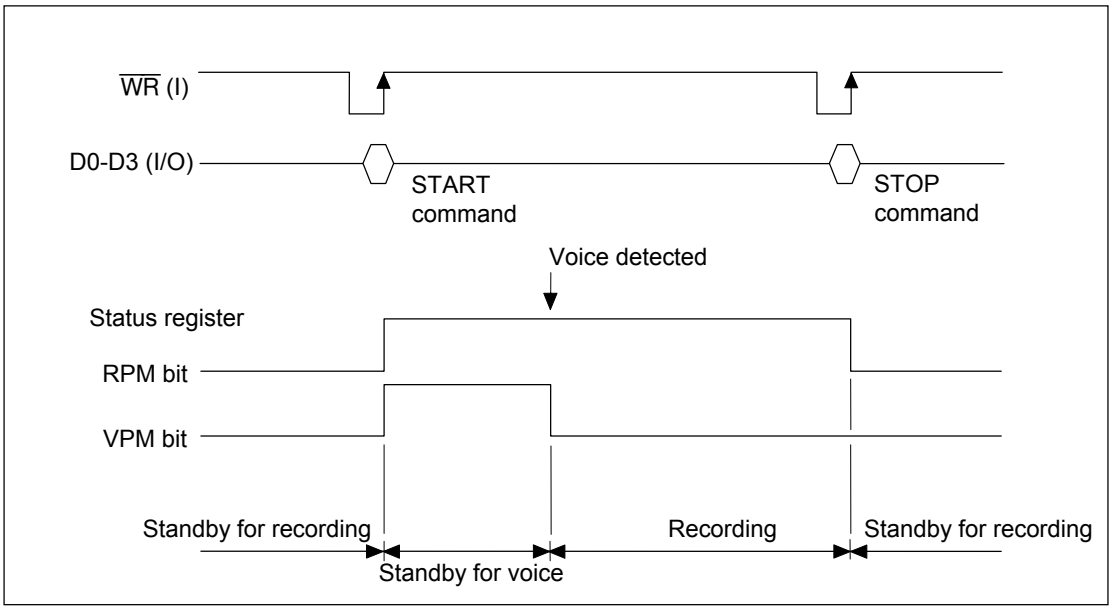


Input of the STOP command during pause causes record/playback to be finished and the IC enters standby mode.

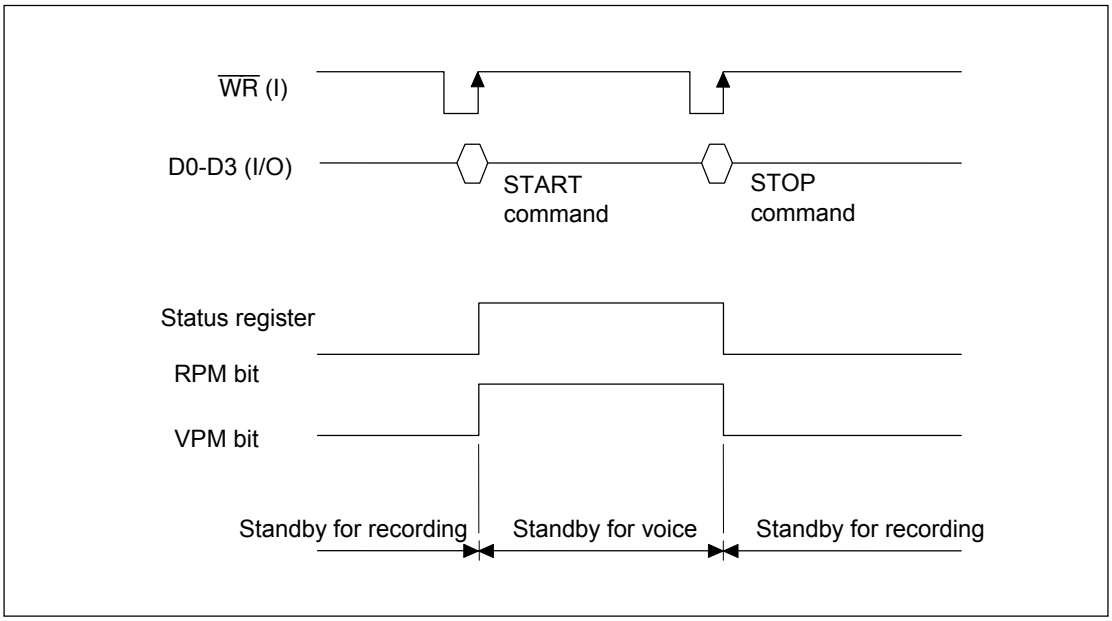


13. Operation in voice triggered starting (VDS command)

By setting the VD0 and VD1 data bits of the VDS command, recording through voice triggered starting is enabled. Using voice triggered starting, it is possible to eliminate the silence data prior to the detection of voice data thus utilizing the memory capacity efficiently. However, elimination of silence data, once voice triggered recording has begun, does not occur. During standby for voice, the VPM bit of the status register is held at 1 and is reset back to 0 when recording starts after voice is detected. The RPM bit becomes 1 after recording starts.



Input of a STOP command during standby for voice causes the IC to first finish standby for voice and then enter standby for recording.



14. Address control operation

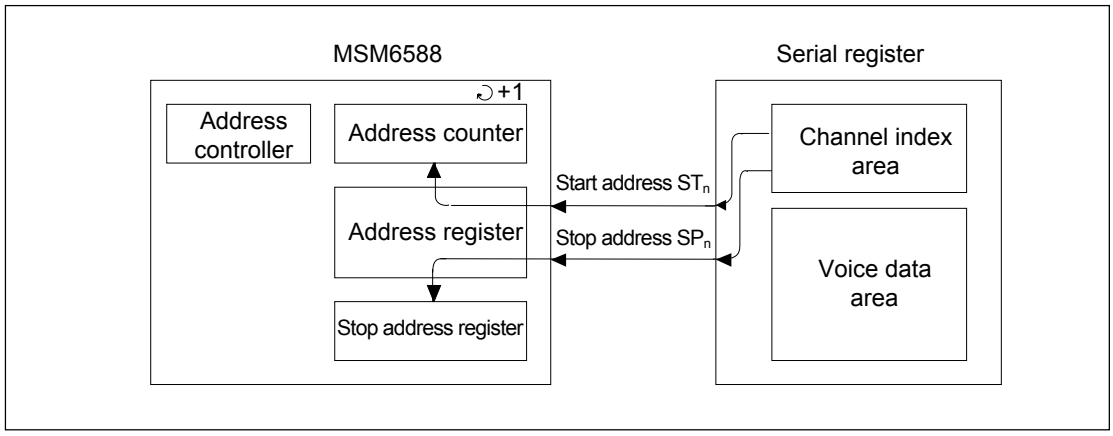
Address control operation during record/playback is performed via the channel index area.
Transfer of data with the channel index area differs depending on the control mode during recording.

14.1 Address control operation during recording

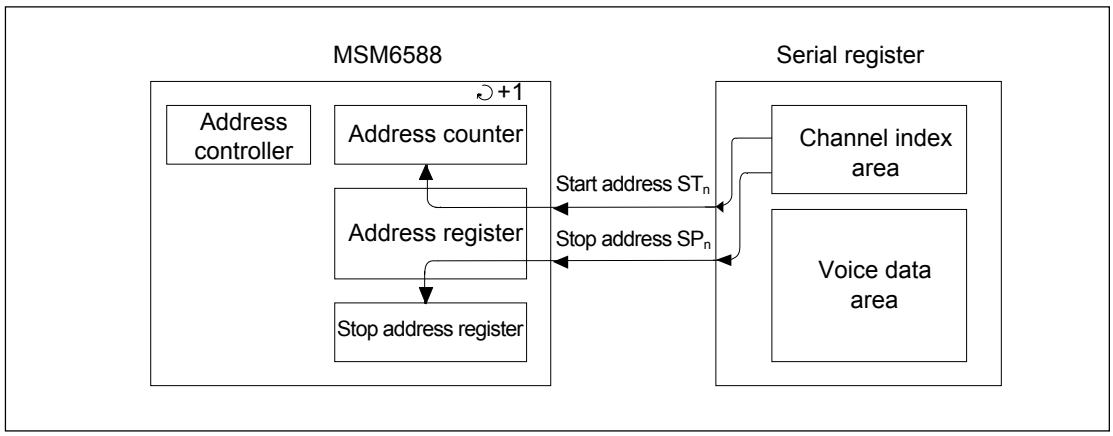
14.1.1 Direct mode recording

(1) Address data is directly written to the channel index area by the ADRWR command.
(2) With the input of a START command, the start and stop addresses are read from the channel index area. They are then set to the address counter and the stop address register via the address register.
After this address control operation, recording is begun and the address counter counts up.
(3) When recording is stopped by the STOP command, the contents of the address counter at that time are stored in the channel index area as the new stop address.

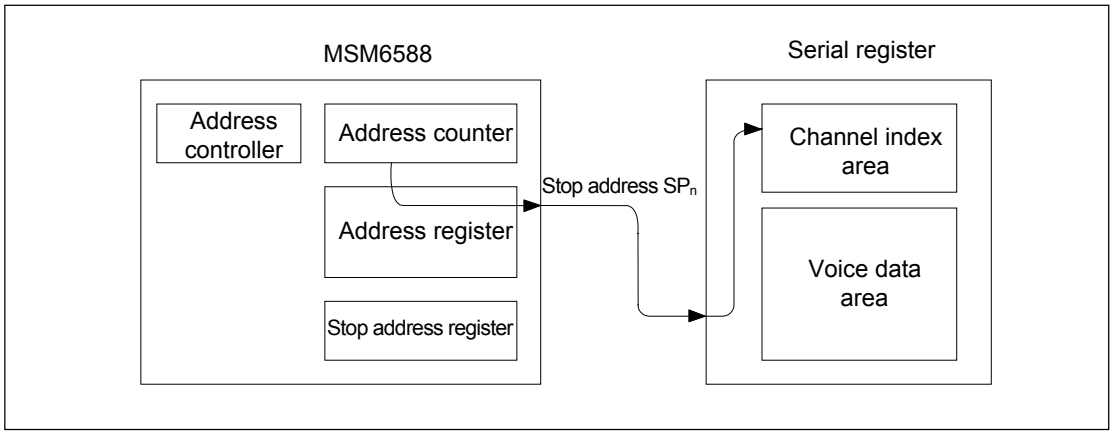
1) ADRWR Command Input



2) START Command Input (recording begins)



3) STOP Command (recording stops)

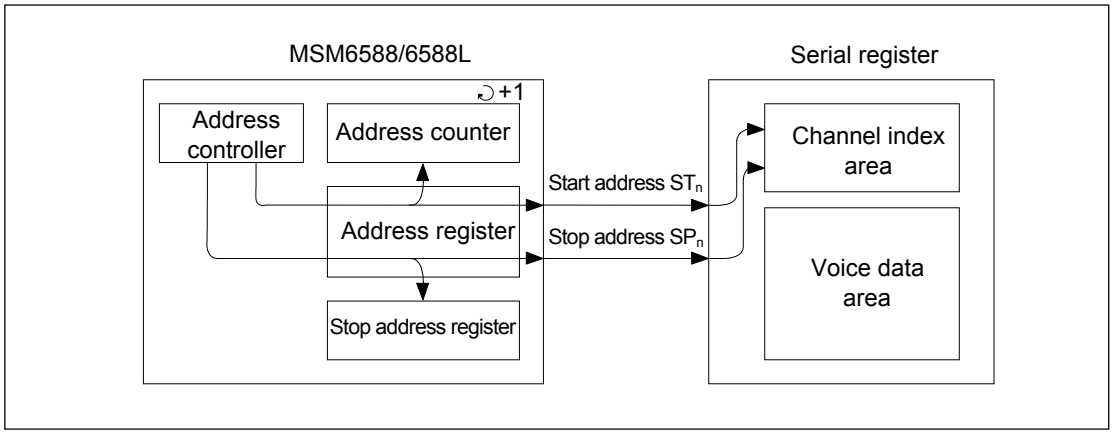


14.1.2 Fixed mode recording

(1) With the input of a START command, the start and stop address generated in the address controller is set to the address counter and the stop address register via the address register, respectively. The address data is stored in the channel index area.
After this address control operation, recording is begun and the address counter counts up.

(2) When the recording is stopped by the STOP command, the contents of the start address counter at that time are stored in the channel index area as the new stop address.

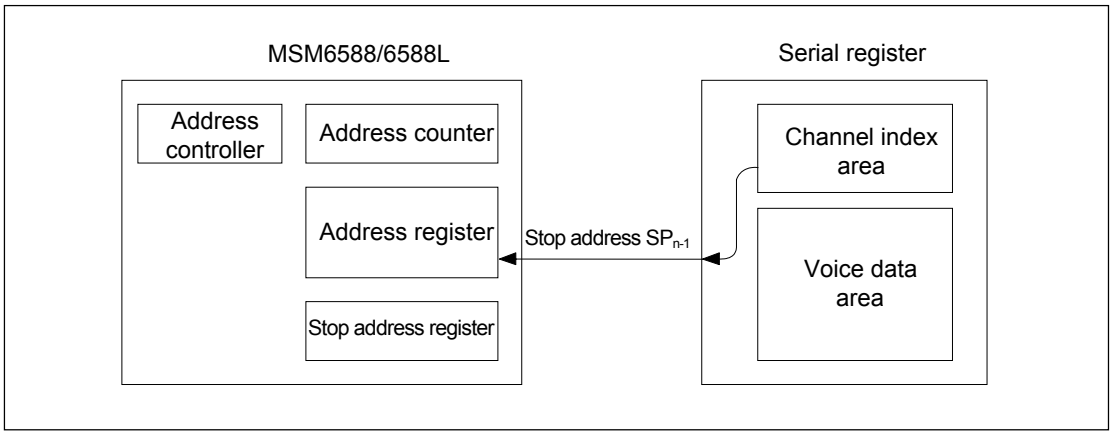
1) START Command Input (recording begins)



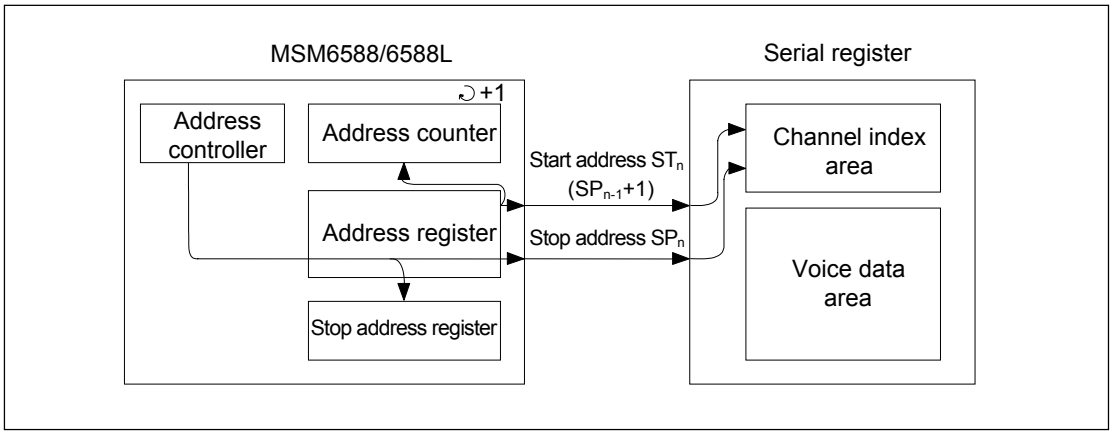
14.1.3 Flex mode recording

(1) With the input of a START command, the stop address of the preceding channel (SP_{n-1}) is read out from the channel index area.
(2) Next, address data incremented by 1 from the contents of the stop address are stored in the address counter and the channel index area as the start address ($ST_n = SP_{n-1}+1$).
The stop address generated in the address controller (the maximum address of the serial register) is set in the stop address register and is stored in the channel index area.
After this operation, recording is begun and the address counter counts up.
(3) When recording is finished by the STOP command, the contents of the address counter at that time are stored in the channel index area as the new stop address.

1) START Command Input



2) Start of Recording

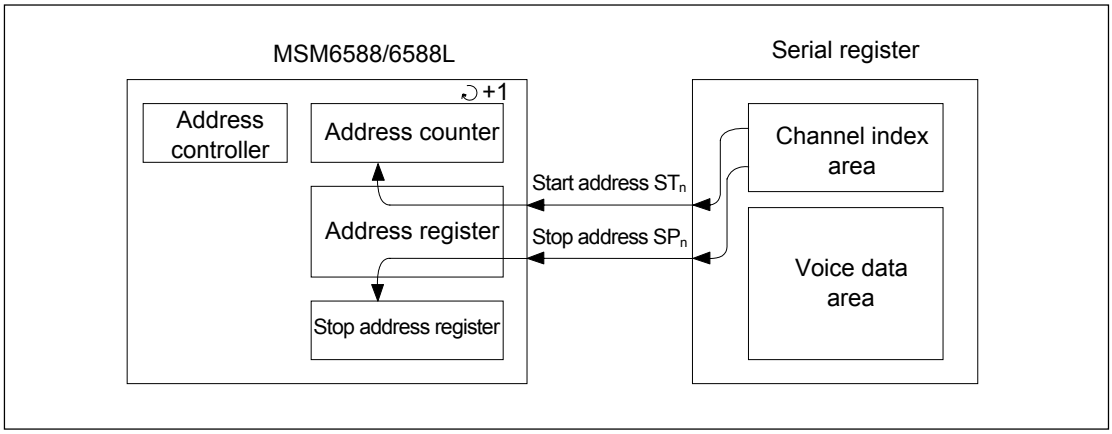


14.2 Address control operation during playback

During play back, the IC performs playback using the address and stop addresses stored in the channel index area regardless of the control mode.

(1) With the input of a START command, the IC first reads the start and stop address from the channel index area. They are then set to the address counter and the stop address register, respectively, through the address register.
After this address control operation, playback begins and the address counter counts up.
(2) When a STOP command is input, playback is stopped. No address control operation is performed at this time.

1) START Command Input (playback starts)



15. Multi-channel record/playback method

It is possible to record/playback on multiple channels by preparing memory corresponding to the channel index area that stores the start and stop addresses of each channel inside a microcontroller or equivalent external circuit. Recording/playback of multiple channels is performed in the direct mode and the channel index area can be used as temporary address data storage. In the case of playback for the fixed message stored into the serial voice ROM, the address data of each word can be similarly stored into a ROM in a microcontroller. The following shows the procedure.

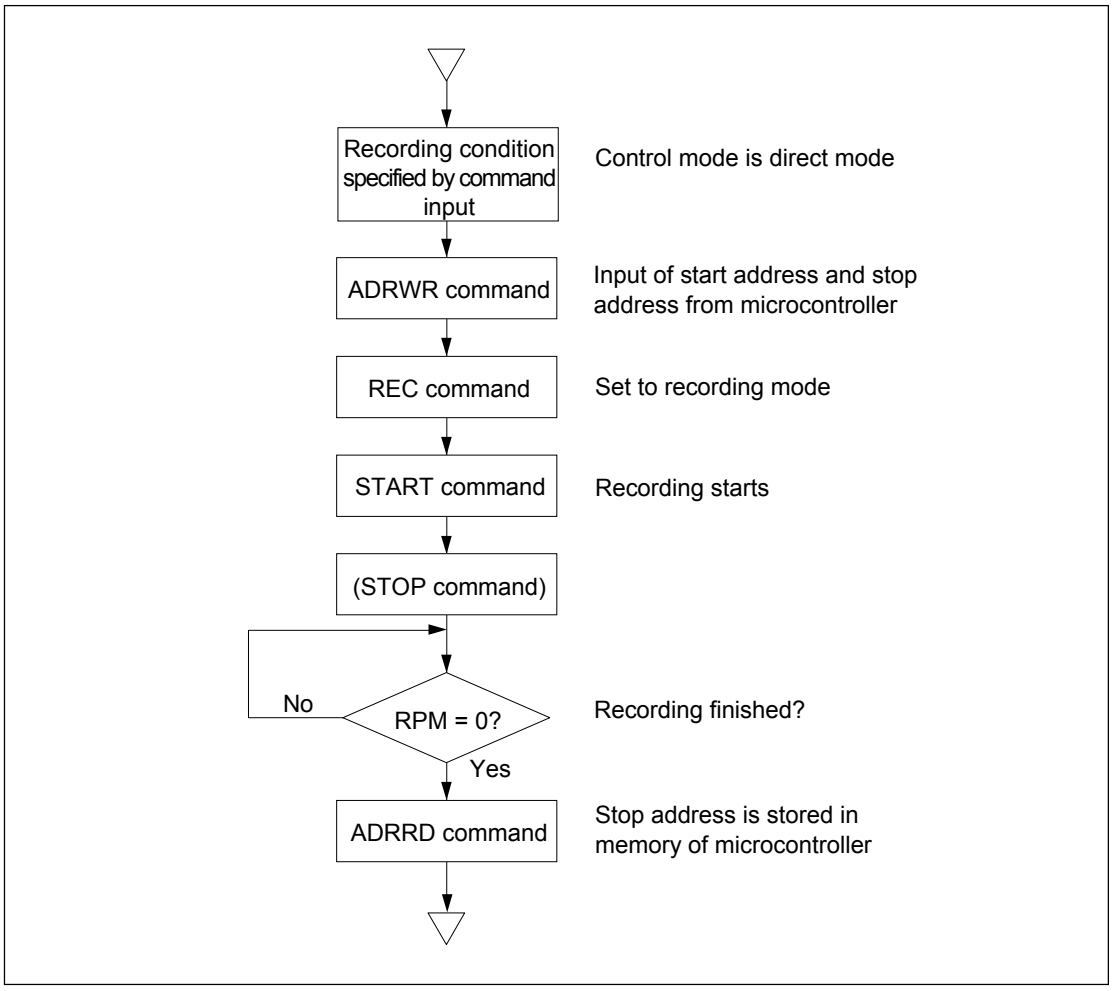
15.1 Multi-channel recording method

(1) Recording conditions are specified by a command input similar to the recording method in direct method. Channels can be specific (e.g. ch0).
(2) The stop and start addresses can be written into the channel index area by the ADRWR command.
(3) Recording is started.
(4) After recording is performed, the stop address which is stored in the channel index area by the ADRRD command is read out.
(5) The stop address is stored in microcontroller memory.

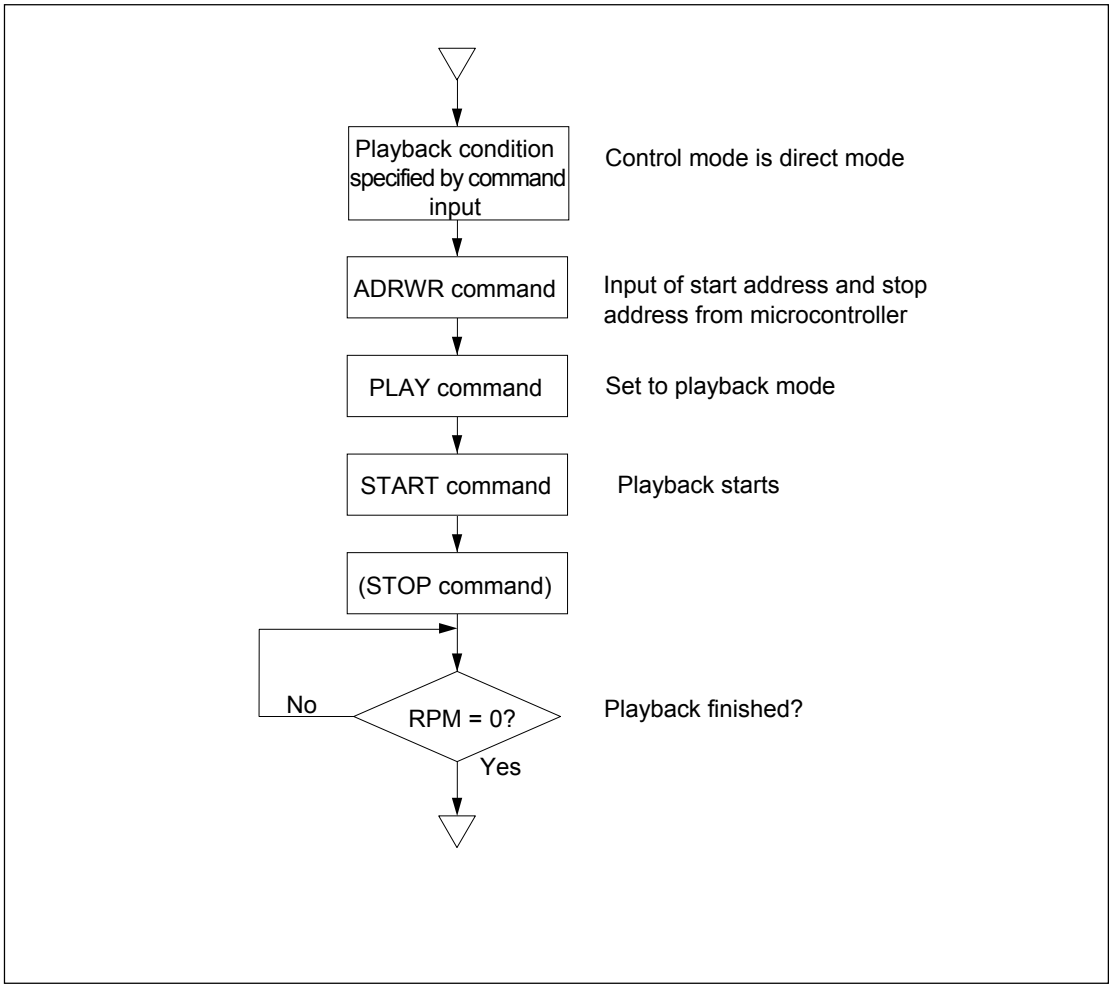
15.2 Multi-channel playback method

(1) Playback conditions are specified by a command input.
(2) The stop and start addresses that are stored in microcontroller memory are written in the channel index area by the ADRWR command.
(3) Playback is started.

Flowchart to Multi-channel Recording



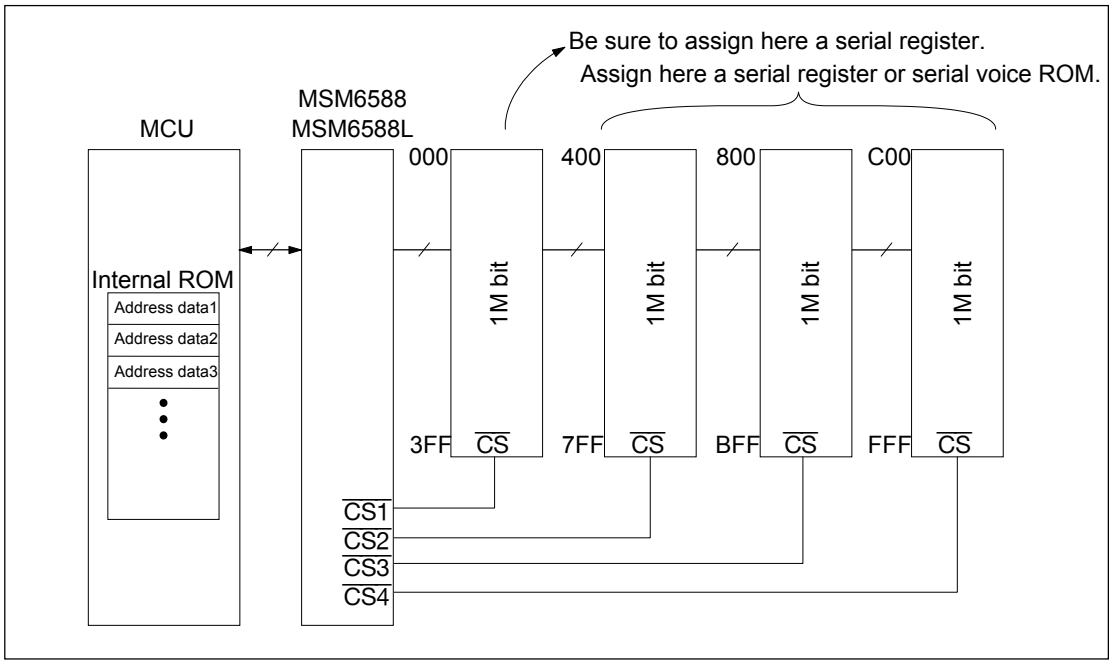
Flowchart to Multi-channel Playback



16. Playback method by means of a serial voice ROM

The following describes how to play a fixed message by connecting a serial voice ROM to the MSM6588/6588L.

16.1 Circuit and memory configurations

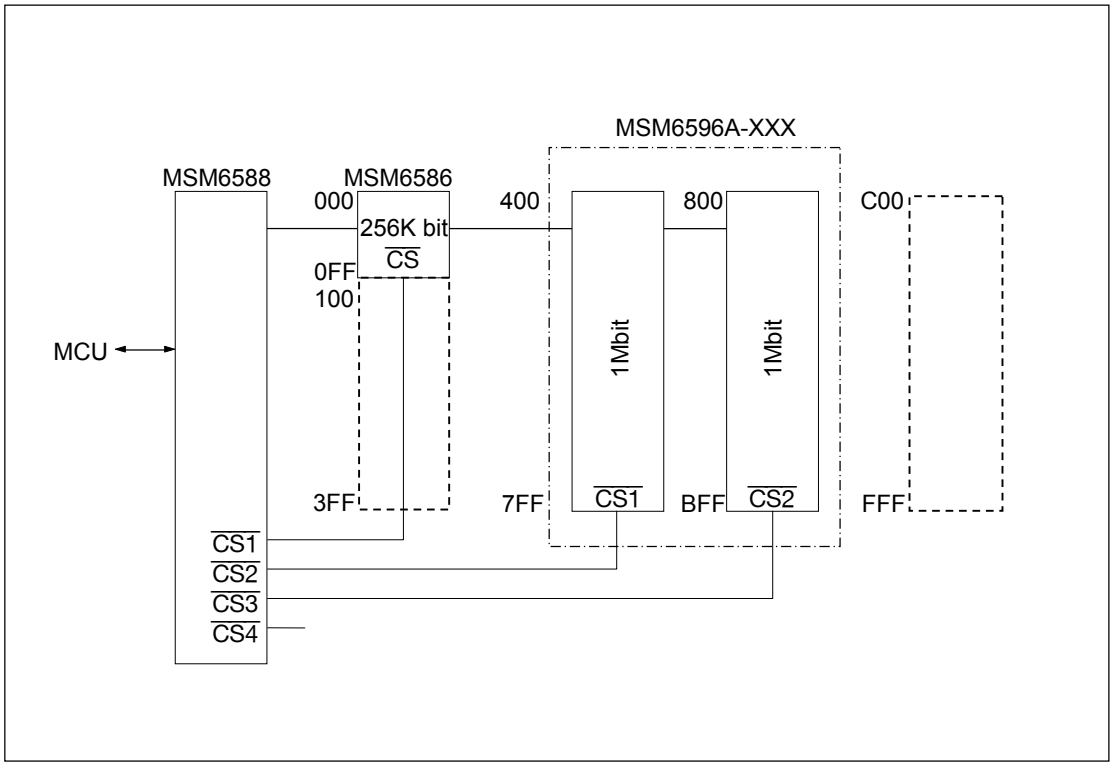


	Address space (X address)	Serial register	Serial voice ROM
$\overline{CS1}$	000h-3FFh	Assignable	Unassignable
$\overline{CS2}$	400h-7FFh	Assignable	Assignable
$\overline{CS3}$	800h-BFFh	Assignable	Assignable
$\overline{CS4}$	C00h-FFFh	Assignable	Assignable

A serial register or serial voice ROM is assigned in the unit of 1 Mbit ($\overline{CSn}$).

Note: Be sure to connect a serial register to $\overline{CS1}$.
It is impossible to connect only a serial voice ROM and use it for playback only.

The following circuit configuration shows the case where 256K bit and 2M bit are used for playback and for a fixed playback, respectively.
For playback (variable message): 256K bit serial register MSM6586
For fixed message: 2M bit serial voice ROM MSM6596A-XXX



$\overline{CS1}$	000h-0FFh	Serial register for variable message
	100h-3FFh	Unused (no addressing)
$\overline{CS2}$	400h-7FFh	Serial voice ROM for fixed message
$\overline{CS3}$	800h-BFFh	
$\overline{CS4}$	C00h-FFFh	Unused (no addressing)

Serial register
- 256K bit MSM6586
- 512K bit MSM6587
- 1M bit MSM6389C

Serial voice ROM
- 1M bit MSM6595A-XXX
- 2M bit MSM6596A-XXX
- 3M bit MSM6597A-XXX

16.2 How to control playback when a serial voice ROM is used.

(1) ROM for saving address data

A start address and stop address for each word must be previously saved in the microcontroller's ROM when a serial voice ROM is used for playback.
The address data is 32 bits per word.

	Upper X-address	Lower Y-address	
Start address	12 bits	—	32 bits
Stop address	12 bits	8 bits	per word

MCU's ROM size = 32 bits × number of voice words

(2) Address data

Address data described in the address correspondence table are saved in the microcontroller's ROM. The following offset addresses are added to $\overline{CS2}$ through $\overline{CS4}$, to which a serial voice ROM is assigned.

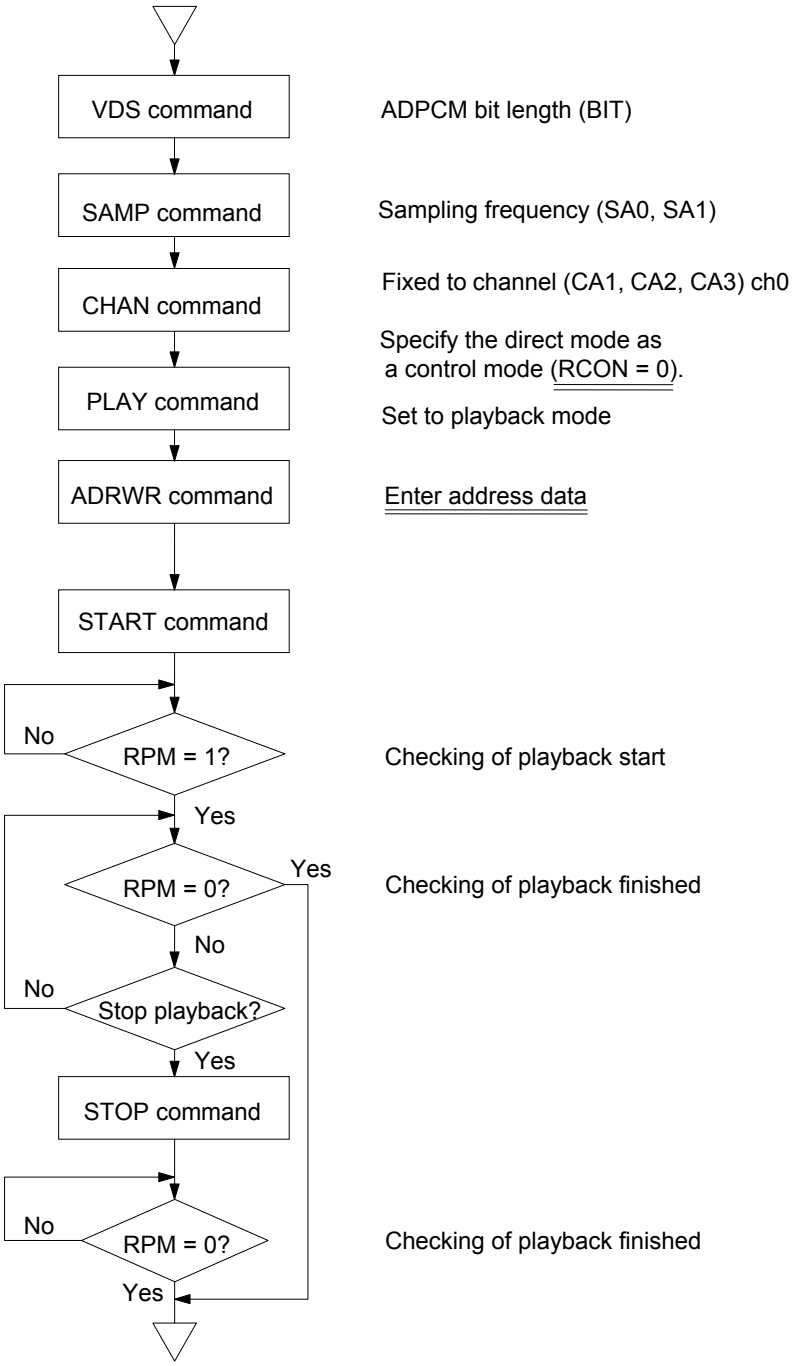
Assigned to	Offset address
$\overline{CS2}$	+400h
$\overline{CS3}$	+800h
$\overline{CS4}$	+C00h

For example, in the previous circuit, when MSM6596-600 is assigned to $\overline{CS2}$ and $\overline{CS3}$, and "GOZEN" that means "morning" is voiced, the address is shown below.

	Start X		Stop X		Stop Y	
No.1 00 GOZEN	0		10		5D	
	↓	+400h	↓	+400H	↓	no addition
Address to be specified→	400h		410h		5Dh	

(3) Flowchart to Serial Voice ROM

The serial voice ROM playback differs in its playback method from the serial register playback because after specifying the channel the serial voice ROM playback requires to enter the address data that are saved in the microcontroller's ROM, using the ADRWR command.
The channel index area is used temporarily.
Therefore, for example, ch0 is used only for serial voice ROM playback.

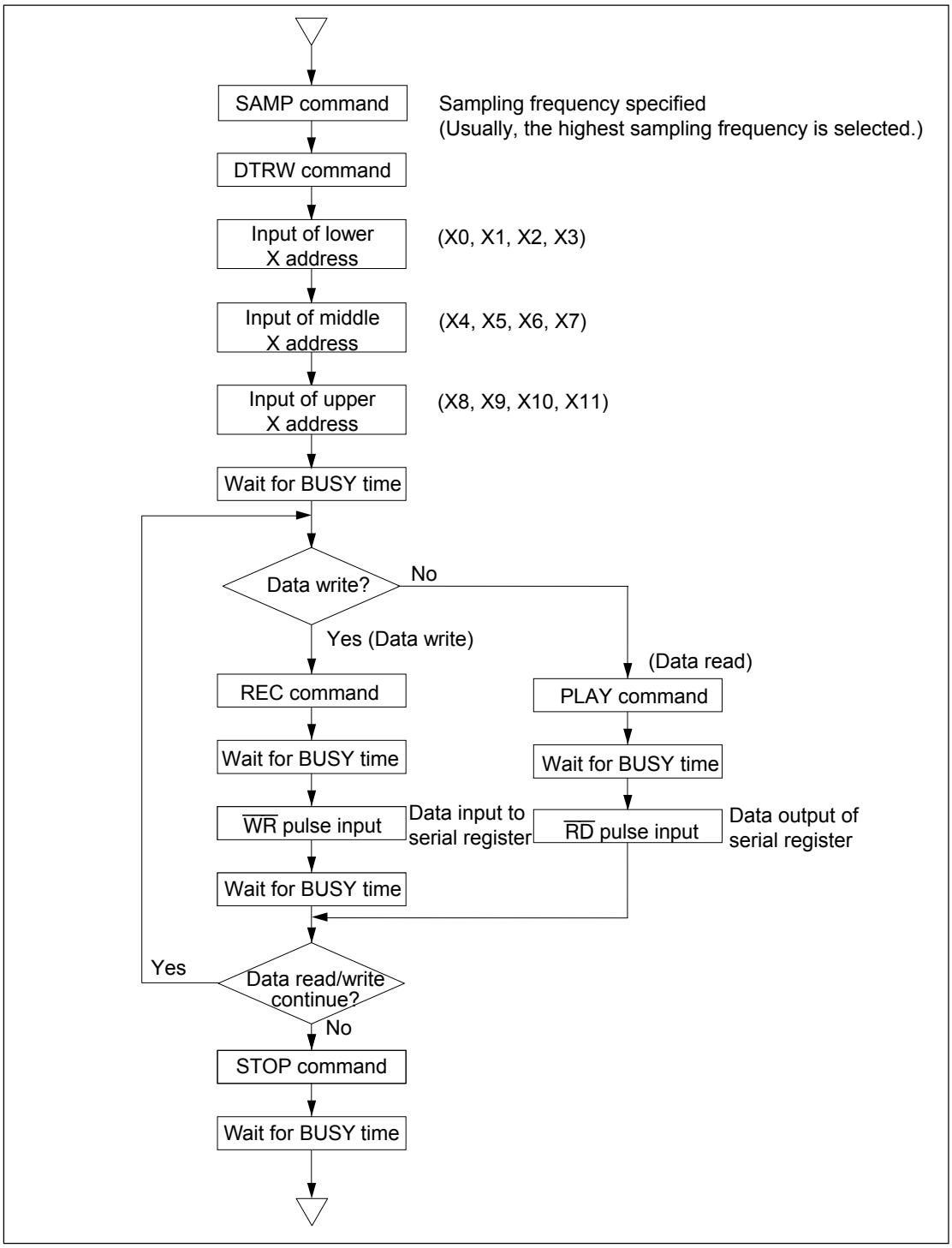


17. Data transfer method with external serial registers (DTRW command)

Data transfer can be performed with external serial registers using the DTRW command.
After input of the DTRW command, the X address of the serial register for read/write is specified. Data in 4-bit nibbles are transferred from the header of the X address specified. Although the serial registers are composed of the X address times 1K bit (Y direction), the address can be specified only in the X direction and no random address specification can be made that selects the middle of the Y direction.
A single DTRW command input can do read/write operations continuously if they are in the range of the same serial register. When the operation extends to other serial registers, it is necessary to suspend the operation temporarily and re-specify the address by input of the DTRW command.
The following is the DTRW command input procedure.

(1) The sampling frequency is specified by input of the SAMP command. Because the access time of data transfer by the DTRW command is proportional to the period of the sampling frequency, the highest frequency is usually selected.
(2) Input the DTRW command.
(3) Specify the header X address of the serial register with 3 WR pulses.
(4) Wait for BUSY time. Alternatively, the BUSY bit of the status register can be used to confirm this.
(5) For writing data, input the data to be written with a WR pulse after input of the REC command. It is necessary to wait for BUSY time between each WR pulse.
When performing data/write by a single DTRW command, the BUSY state can be checked by the BUSY bit of the status register but if data read is also performed, confirmation by the BUSY bit cannot be performed.
(6) For data read, 4-bit of data are output from the data bus by input of a RD pulse, after waiting for the BUSY time, after the input of the PLAY command.
For data read, confirmation of BUSY state by the BUSY bit is invalid.
(7) If data read/write is to be continued, specify data transfer by read/write mode using the PLAY/REC commands.
(8) If data read/write is to be terminated, input the STOP command. Wait for BUSY time and start input of the next command. If data read is performed, confirmation by the BUSY bit is invalid.

Flowchart of data transfer by the DTRW command



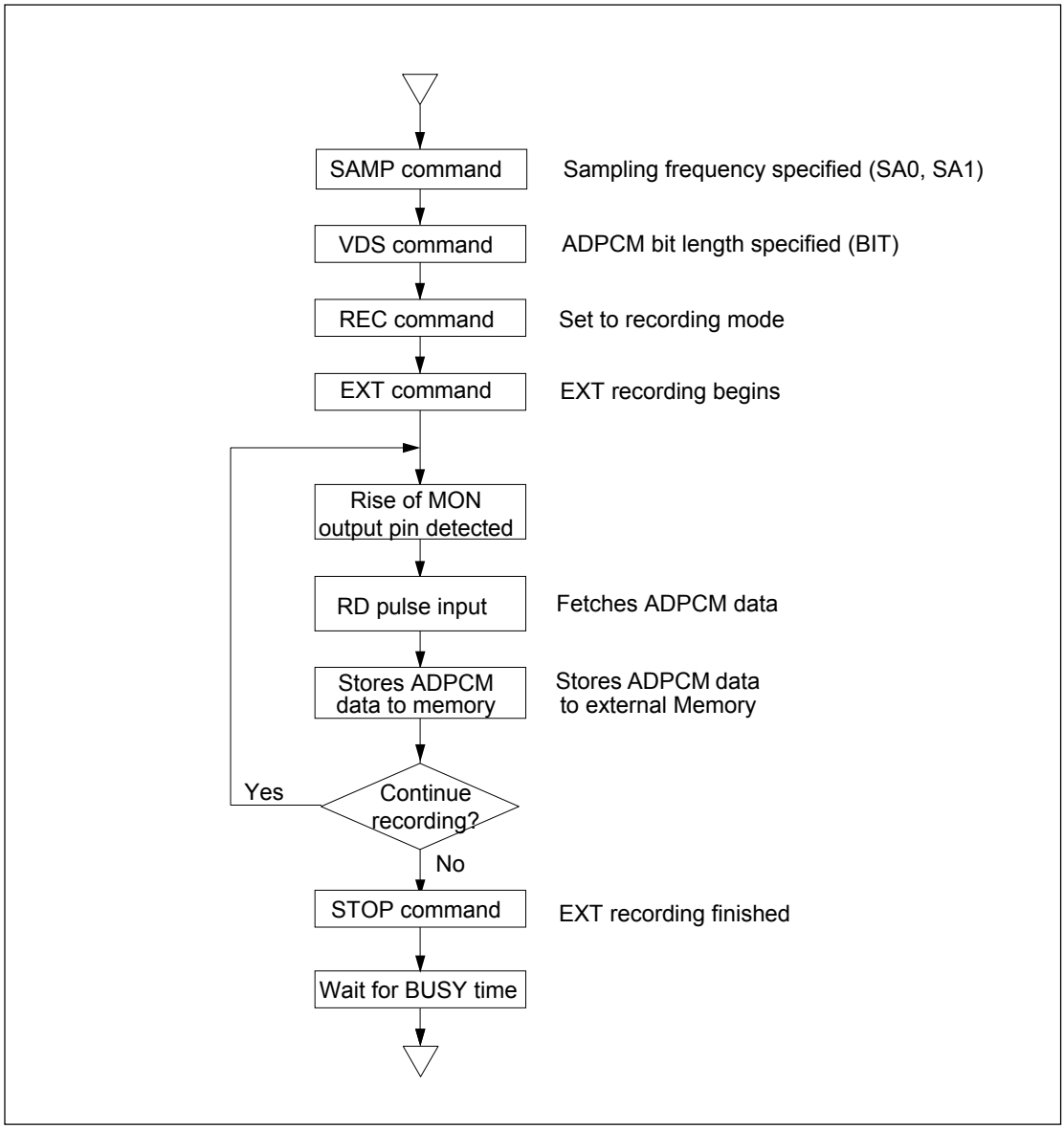
18. Method of record/playback by input/output of voice data from the data bus (EXT command)

When SRAM or a harddisk is used to store voice data instead of the serial registers, use the EXT command to do record/playback.
During record/playback using the EXT command, voice data (ADPCM data) is directly input/output from the data bus at the sampling frequency. There is no address control nor external serial register control at this time, therefore, it is necessary to use the microcontroller to control recording time and addresses.
Pause, voice-triggered starting function and selection of channels cannot be made during record/playback. Valid commands are PLAY, REC, STOP, SAMP, VDS and EXT only.

18.1 EXT command recording method

(1) The sampling frequency is specified by SA0 and SA1 data of the SAMP command.
(2) The ADPCM bit length is specified by BIT data of the VDS command.
(3) Input the REC command to set the recording mode.
(4) Input the EXT command to start recording. The sampling frequency clock is output from the MON pin.
(5) When the MON output pin becomes "H" level, input a $\overline{RD}$ pulse to fetch ADPCM data from the data bus. At that time, input the $\overline{RD}$ pulse to satisfy time t_{ERD} from rise of MON to rise of the $\overline{RD}$ pulse. The upper 3 bits (D3 to D1 pin) are valid for 3-bit ADPCM.
(6) Store ADPCM data to external memory.
(7) Repeat steps (5) and (6) to continue recording.
(8) To stop recording input a STOP command. Recording can be continued for an indefinite period of time until the STOP command is input.
When the MON pin becomes "H" level, input the $\overline{RD}$ pulse to fetch the ADPCM data, and input the STOP command to satisfy time t_{ESP} from rise of MON to input of the STOP command.
(9) As the status register cannot be checked during recording with the EXT command, it is necessary to wait for BUSY time after input of the STOP command to start input of the next command.

Flowchart of recording with the EXT command

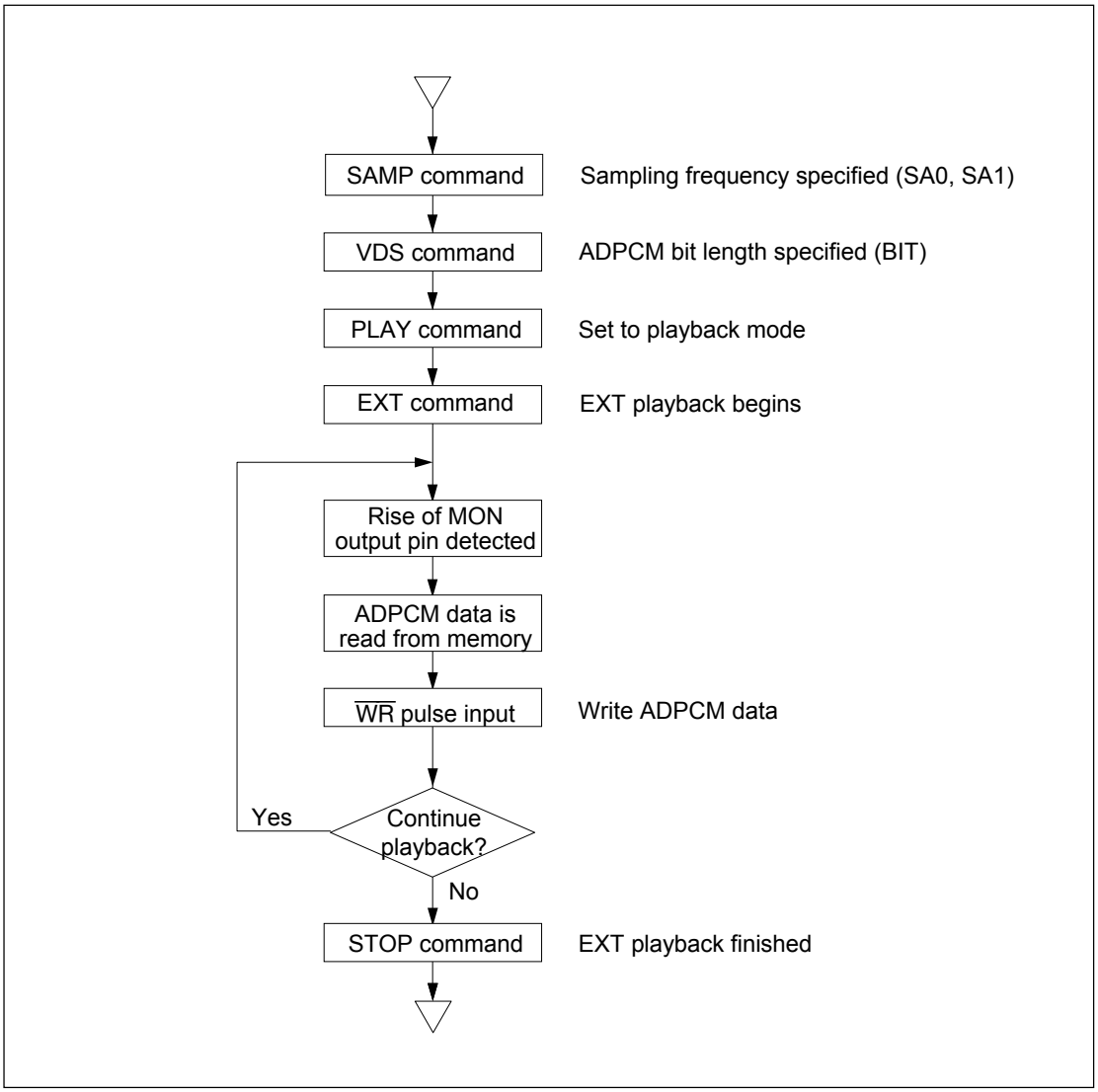


18.2 EXT command playback method

(1) Specify the sampling frequency by SA0 and SA1 data of the SAMP command.
(2) Specify the ADPCM bit length of recording by BIT data of the VDS command.
(3) Input the PLAY command to set playback mode.
(4) Input the EXT command to start playback. The sampling frequency clock is output from the MON pin.
(5) When the MON pin becomes "H", fetch ADPCM data from external memory.
(6) Input a $\overline{WR}$ pulse to get ADPCM data from the data bus. At that time, input the $\overline{WR}$ pulse to satisfy time t_{EWR} from rise of MON to rise of the $\overline{WR}$ pulse. In 3-bit ADPCM, the upper 3 bits (D3 to D1 pin) are valid and data in the lower 1 bit (D0 pin) is invalid.
(7) Repeat steps (5) and (6) to continue playback.
(8) Input the STOP command to end playback.
When the MON pin becomes "H", input the $\overline{WR}$ pulse, input the ADPCM data, and input the STOP command to satisfy time t_{ESP} from rise of MON to input of the STOP command, and interval t_{WE1} between the $\overline{WR}$ pulse and the STOP command pulse.

Note: Input the ADPCM data beginning with the top of a phrase every sampling period sequentially. If the ADPCM data is input beginning with the second or following part of a phrase or with data missing, normal (playback) waveforms cannot be regenerated.

Flowchart of playback by the EXT command



19. Reset and power down function

By input of a "L" level to the $\overline{\text{RESET}}$ pin, the IC stops oscillation to minimize power consumption and is set to the power down state. The control circuit is simultaneously initialized. Data specified by 2 nibble commands such as the sampling frequency, ADPCM bit length, and data in the serial registers is not affected.
However, when a $\overline{\text{RESET}}$ pulse is input in the middle of record/playback, internal data and voice data become undefined and operation stops.
The following shows the state of the IC at power down.

(1) Oscillation is stopped and all the operations in the internal circuit are halted, the control circuit is initialized.
(2) Power consumption is minimized. When using an external clock, input the GND level to the XT pin at power down so that no current is flowing to the oscillation circuit.
(3) The D0 to D3-pin on the data bus are in the high-impedance state regardless of the $\overline{\text{RD}}$ and $\overline{\text{CE}}$ pins.
(4) Power consumption of the external serial registers is minimized by setting the $\overline{\text{CS1}}$ to $\overline{\text{CS4}}$ pin to a "H" level output.
(5) The state of the output pins are as follows:
$\overline{\text{SAD}}$, $\overline{\text{SAS}}$, $\overline{\text{TAS}}$, $\overline{\text{CS1}}$ to $\overline{\text{CS4}}$, $\overline{\text{WE}}$, $\overline{\text{RWCK}}$, STBY pins.....“H” level output
MON pin.....“L” level output
DI/O pin.....High-impedance
AOUT, FOUT pins.....GND level output

APPLICATION CIRCUITS

Figure 1 shows an application circuit when the MSM6588/6588L is used in stand-alone mode and four 1M bit serial registers are used.
Figure 2 shows an application circuit when the MSM6588/6588L is used in microcontroller interface mode with two 1M bit serial registers and one 2M bit serial voice ROM.
Figure 3 shows an example of application circuit when record/playback is made using the EXT command for MSM6588/6588L.

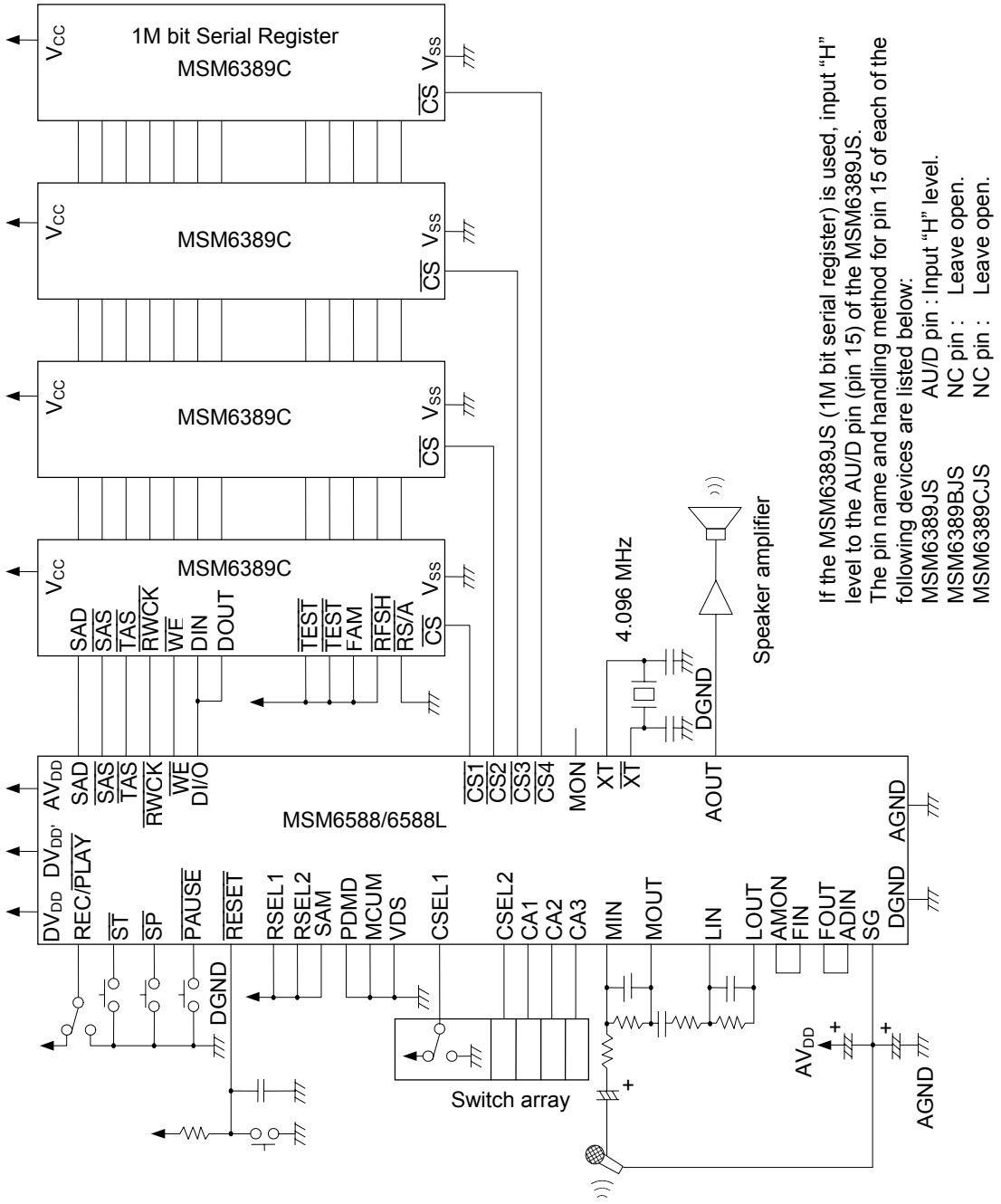


Figure 1 Example of Application Circuit in Stand-alone Mode with 1M bit Serial Registers

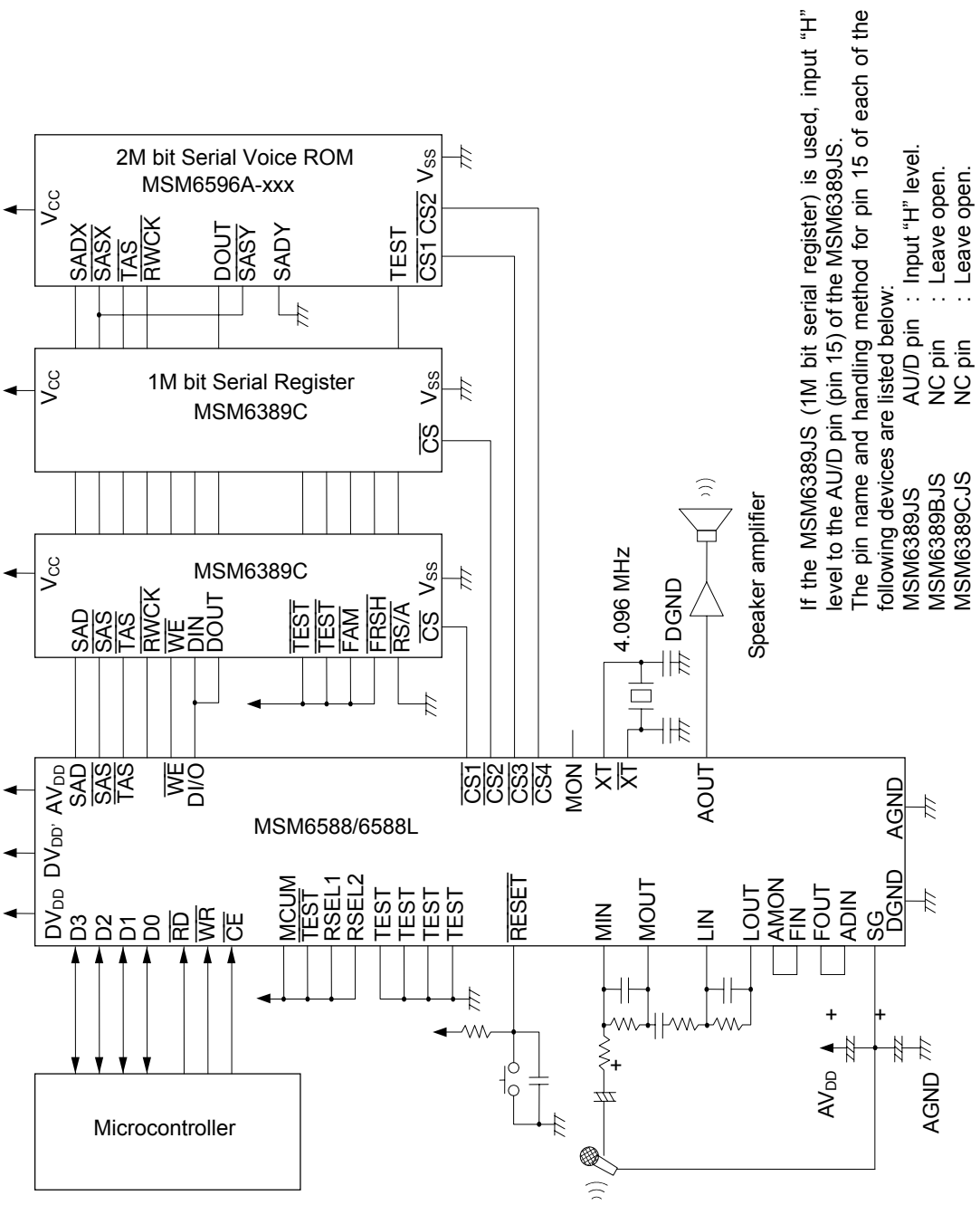


Figure 2 Example of Application Circuit in Microcontroller Interface Mode with 1M bit Serial Registers and 2M bit Serial Voice ROM

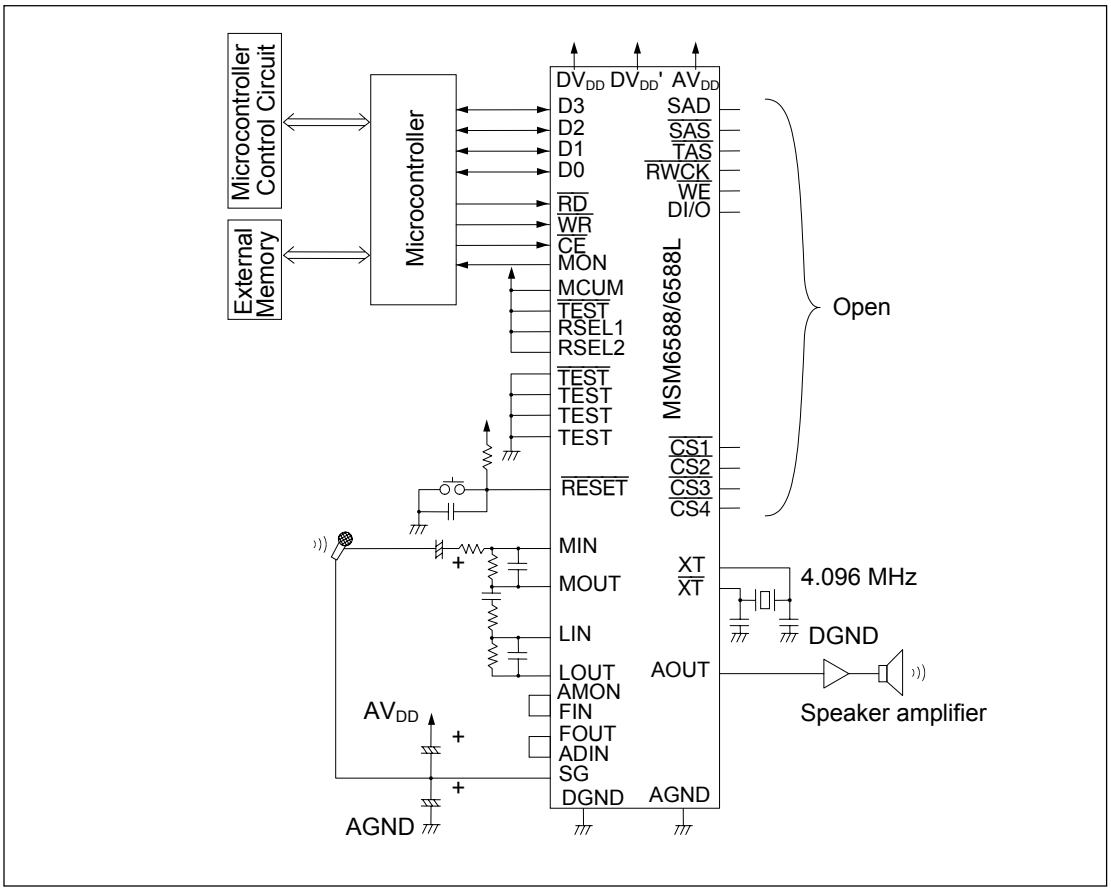
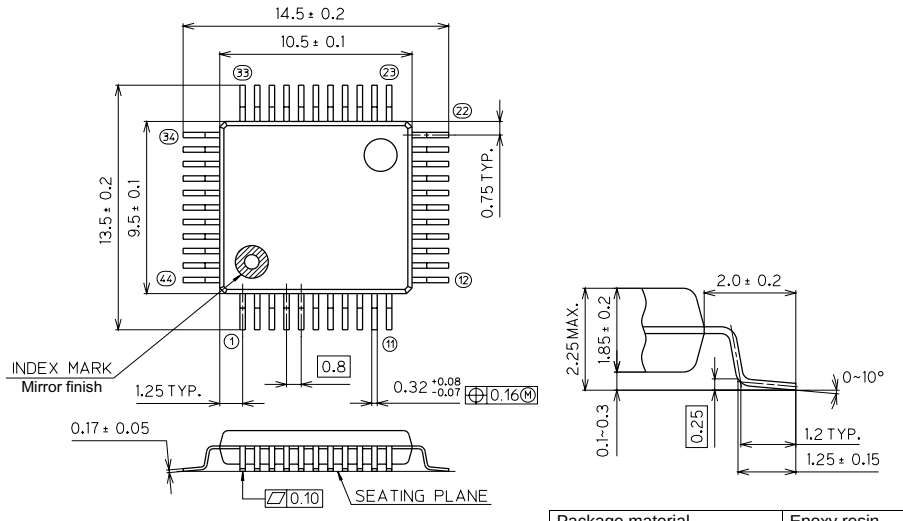


Figure 3 Example of Application Circuit When Record/Playback is Made Using EXT Command

PACKAGE DIMENSIONS

(Unit: mm)

QFP44-P-910-0.80-2K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.41 TYP.
Rev. No./Last Revised	4/Nov. 28, 1996

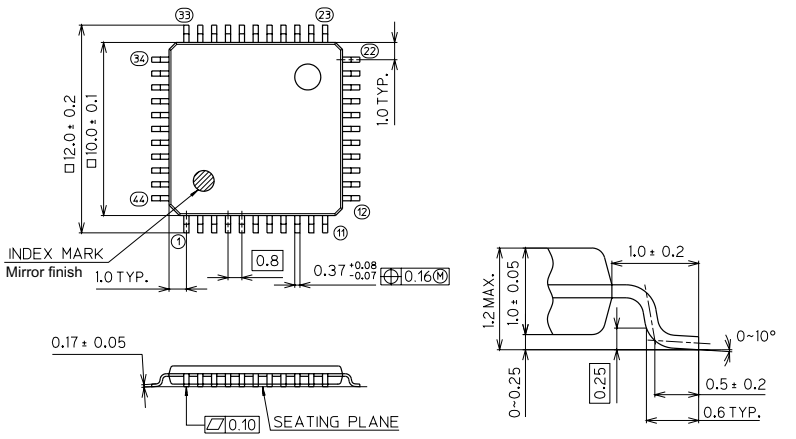
Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit: mm)

TQFP44-P-1010-0.80-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.28 TYP.
Rev. No./Last Revised	5/Oct. 28, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
E2D0025-39-23	Feb. 1999	—	—	Third edition
FEDL6588-6588L-04	Jan. 25, 2002	44	44	Changed contents of the tables for ceramic oscillators
		45	45	
		17	17	Changed the minimum values of t_{CR} and t_{CW} from 30 to 0, respectively.
		22	22	

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2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

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