54F/74F350

4-Bit Shifter
With 3-State Outputs

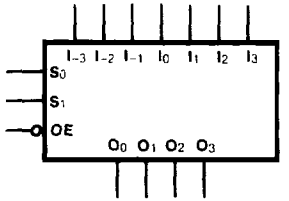
Description

The 'F350 is a specialized multiplexer that accepts a 4-bit word and shifts it 0, 1, 2 or 3 places, as determined by two Select (S_0, S_1) inputs. For expansion to longer words, three linking inputs are provided for lower-order bits; thus two packages can shift an 8-bit word, four packages a 16-bit word, etc. Shifting by more than three places is accomplished by paralleling the 3-state outputs of different packages and using the Output Enable ($\overline{OE}$) inputs as a third Select level. With appropriate interconnections, the 'F350 can perform zero-backfill, sign-extend or end-around (barrel) shift functions.

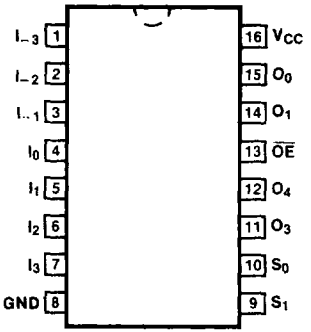
- **Linking Inputs for Word Expansion**
- **3-State Outputs for Extending Shift Range**

Ordering Code: See Section 5

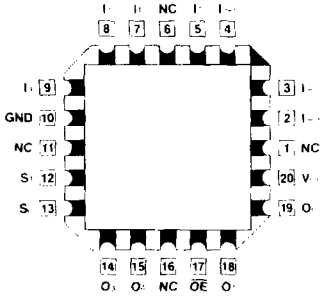
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
S_0, S_1	Select Inputs	0.5/0.75
I_{-3}-I_3	Data Inputs	0.5/0.75
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.75
O_0-O_3	3-State Outputs	75/15 (12.5)

Functional Description

The 'F350 is operationally equivalent to a 4-input multiplexer with the inputs connected so that the select code causes successive one-bit shifts of the data word. This internal connection makes it possible to perform shifts of 0, 1, 2 or 3 places on words of any length.

A 7-bit data word is introduced at the I_n inputs and is shifted according to the code applied to the select inputs S_0, S_1. Outputs O_0-O_3 are 3-state, controlled by an active LOW output enable ($\overline{OE}$). When $\overline{OE}$ is LOW, data outputs will follow selected data inputs; when HIGH, the data outputs will be forced to the high impedance state. This feature allows shifters to be cascaded on the same output lines or to a common bus. The shift function can be logical, with zeros pulled in at either or both ends of the shifting field; arithmetic, where the sign bit is repeated during a shift down; or end around, where the data word forms a continous loop.

Logic Equations

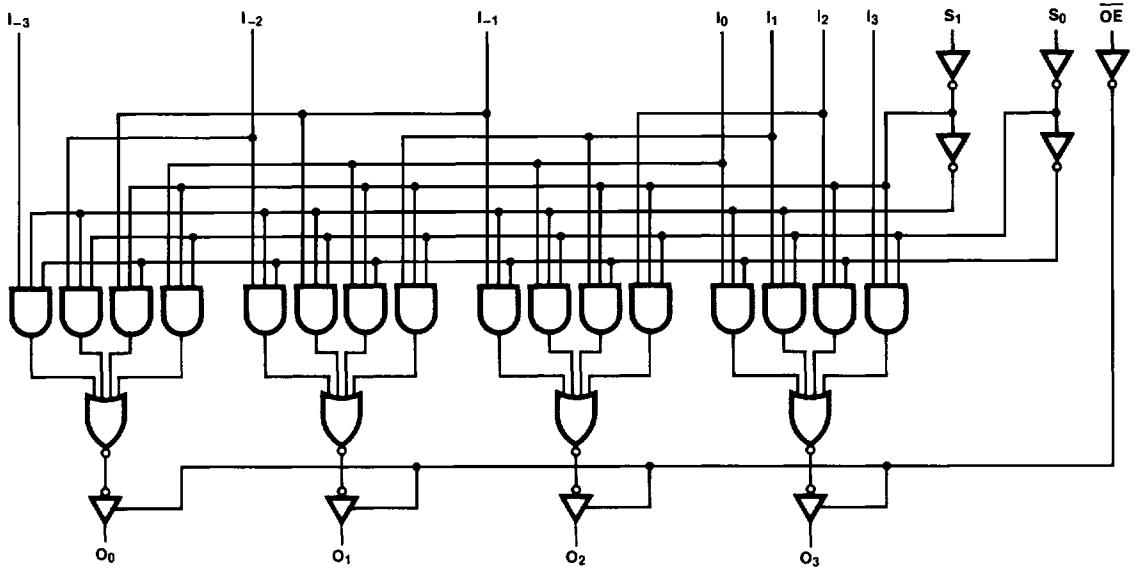
$$O_0 = \overline{S}_0\overline{S}_1 I_0 + S_0\overline{S}_1 I_{-1} + \overline{S}_0 S_1 I_{-2} + S_0 S_1 I_{-3}$$
$$O_1 = \overline{S}_0\overline{S}_1 I_1 + S_0\overline{S}_1 I_0 + \overline{S}_0 S_1 I_{-1} + S_0 S_1 I_{-2}$$
$$O_2 = \overline{S}_0\overline{S}_1 I_2 + S_0\overline{S}_1 I_1 + \overline{S}_0 S_1 I_0 + S_0 S_1 I_{-1}$$
$$O_3 = \overline{S}_0\overline{S}_1 I_3 + S_0\overline{S}_1 I_2 + \overline{S}_0 S_1 I_1 + S_0 S_1 I_0$$

Truth Table

Inputs			Outputs			
$\overline{OE}$	S_1	S_0	O_0	O_1	O_2	O_3
H	X	X	Z	Z	Z	Z
L	L	L	I_0	I_1	I_2	I_3
L	L	H	I_{-1}	I_0	I_1	I_2
L	H	L	I_{-2}	I_{-1}	I_0	I_1
L	H	H	I_{-3}	I_{-2}	I_{-1}	I_0

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

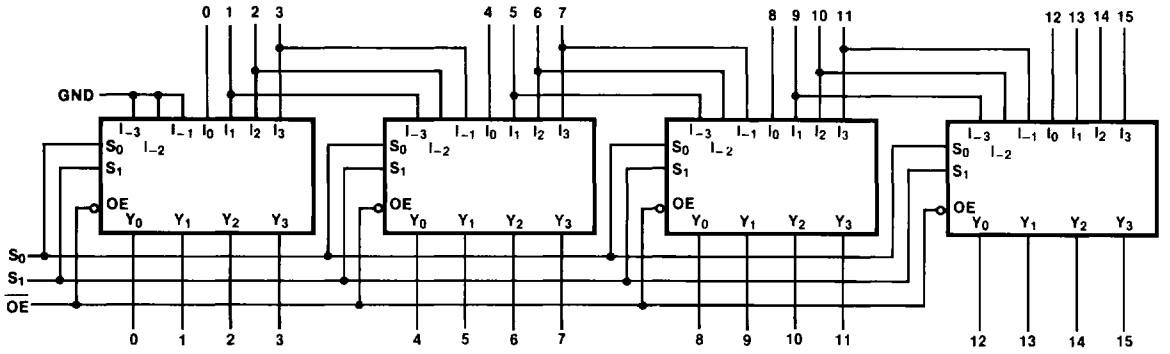
Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		22	35	mA	Outputs HIGH	V_{CC} = Max
I_{CCL}			27	41		Outputs LOW	
I_{CCZ}			26	42		Outputs OFF	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.0	4.5	6.0			3.0	7.0	ns	3-1
t_{PHL}	I_n to O_n	2.5	4.0	5.5			2.5	6.5		3-4
t_{PLH}	Propagation Delay	4.0	7.8	10.0			4.0	11.0	ns	3-1
t_{PHL}	S_n to O_n	3.0	6.5	8.5			3.0	9.5		3-10
t_{PZH}	Output Enable Time	2.5	5.0	7.0			2.5	8.0	ns	3-1, 3-12, 3-13
t_{PZL}		4.0	7.0	9.0			4.0	10.0		
t_{PHZ}	Output Disable Time	2.0	3.9	5.5			2.0	6.5		
t_{PLZ}		2.0	4.0	5.5			2.0	6.5		

Applications

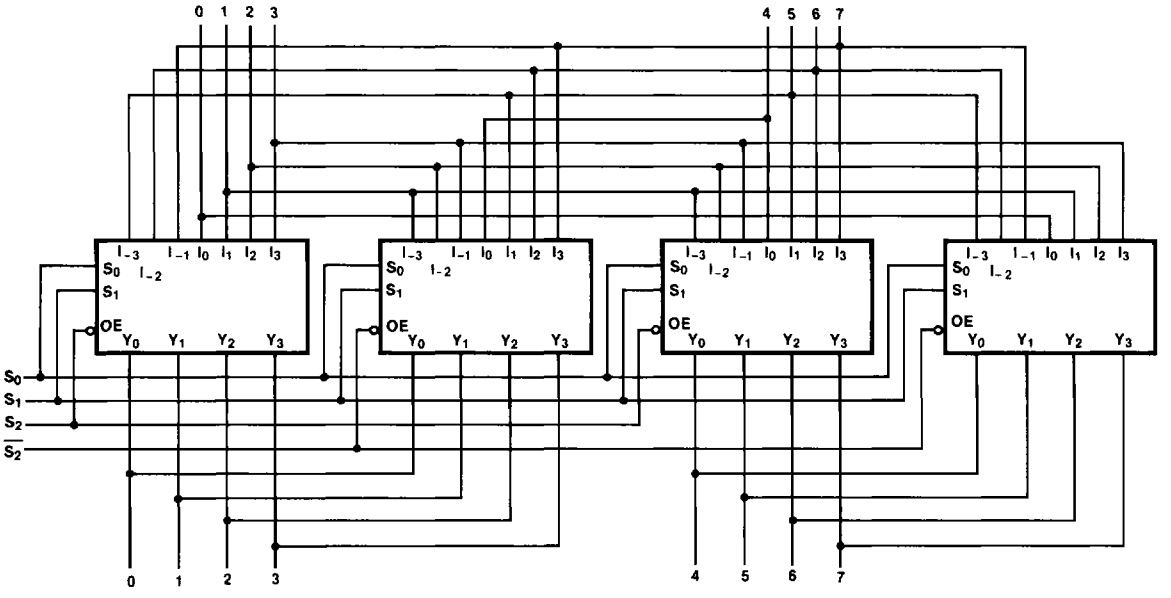
16-Bit Shift-Up 0 to 3 Places, Zero Backfill



Function Table

S_1	S_0	Shift Function
L	L	No Shift
L	H	Shift 1 Place
H	L	Shift 2 Places
H	H	Shift 3 Places

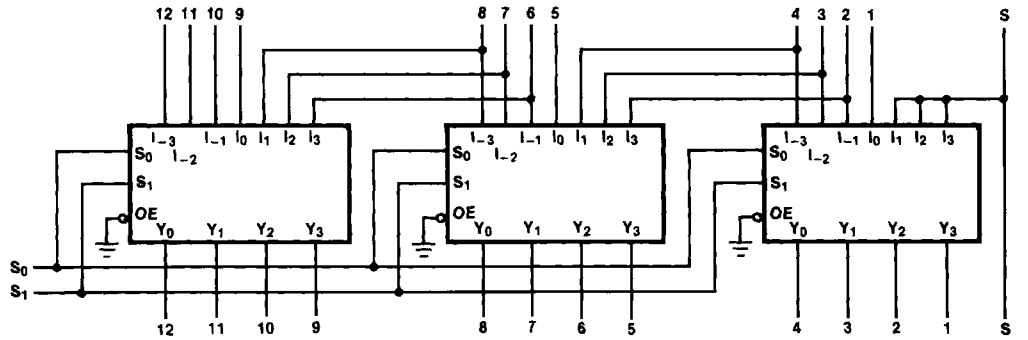
8-Bit End Around Shift 0 to 7 Places



Function Table

S_2	S_1	S_0	Shift Function
L	L	L	No Shift
L	L	H	Shift End Around 1
L	H	L	Shift End Around 2
L	H	H	Shift End Around 3
H	L	L	Shift End Around 4
H	L	H	Shift End Around 5
H	H	L	Shift End Around 6
H	H	H	Shift End Around 7

13-Bit Twos Complement Scaler



Function Table

S_1	S_0	Scale
L	L ÷ 8	1/8
L	H ÷ 4	1/4
H	L ÷ 2	1/2
H	H No Change	1