

2048x8 Registered PROM with Asynchronous Enable

53/63RA1681 53/63RA1681A

Features/Benefits

- Synchronous output enable
- Edge-triggered "D" registers
- Versatile 1:16 user programmable initialization words
- 8-bit-wide in 24-pin SKINNYDIP® for high board density
- Simplifies system timing
- Faster cycle times
- 16 mA I_{OL} output drive capability
- Reliable titanium-tungsten fuses (TiW), with programming yields typically greater than 98%

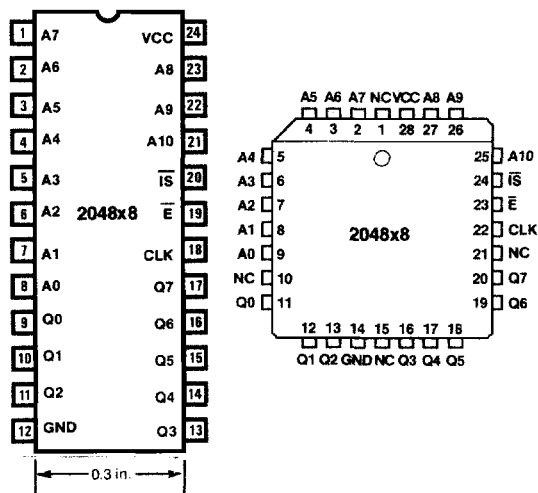
Applications

- Microprogram control store
- State sequencers
- Next address generation
- Mapping PROM

Description

The 53/63RA1681 and 53/63RA1681A are 2Kx8 PROMs with on-chip "D"-type registers. Output enable control through an asynchronous enable input and flexible start up sequencing through programmable initialization words.

Pin Configurations



Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7 V	12 V
Input voltage	-1.5 V to 7 V	7 V
Input current	-30 mA to +5 mA	
Off-state output voltage	-0.5 V to 5.5 V	12 V
Storage temperature	-65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	TYP†	MILITARY				COMMERCIAL				UNIT
			53RA1681A		53RA1681		63RA1681A		63RA1681		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Width of clock (high or low)	10	20		20		20		20		ns
$t_{s(A)}$	Setup time from address to clock	28	40		45		35		40		ns
$t_{s(\overline{IS})}$	Setup time from \overline{IS} to clock	20	30		35		25		30		ns
$t_{h(A)}$	Hold time address to clock	-5	0		0		0		0		ns
$t_{h(\overline{IS})}$	Hold time (\overline{IS})	-5	0		0		0		0		ns
V_{CC}	Supply voltage	5	4.5	5.5	4.5	5.5	4.75	5.25	4.75	5.25	V
T_A	Operating free-air temperature	25	-55	125	-55	125	0	75	0	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP†	MAX	UNIT		
V_{IL}	Low-level input voltage					0.8	V		
V_{IH}	High-level input voltage			2.0			V		
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}$	$I_I = -18 \text{ mA}$			-1.2	V		
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.4 \text{ V}$			-0.25	mA		
I_{IH}	High-level input current	$V_{CC} = \text{MAX}$	$V_I = V_{CC} \text{ MAX}$			40	μA		
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$	$I_{OL} = 16 \text{ mA}$			0.5	V		
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$	MIL $I_{OH} = -2 \text{ mA}$ COM $I_{OH} = -3.2 \text{ mA}$			2.4	V		
I_{OZL}	Off-state output current	$V_{CC} = \text{MAX}$	$V_O = 0.4 \text{ V}$			-40	μA		
I_{OZH}			$V_O = 2.4 \text{ V}$			40			
I_{OS}	Output short-circuit current*	$V_{CC} = 5 \text{ V}$	$V_O = 0 \text{ V}$	-20		-90	mA		
I_{CC}	Supply current	$V_{CC} = \text{MAX}$. All inputs TTL; all outputs open					140	185	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typical at 5.0 V V_{CC} and 25°C T_A .

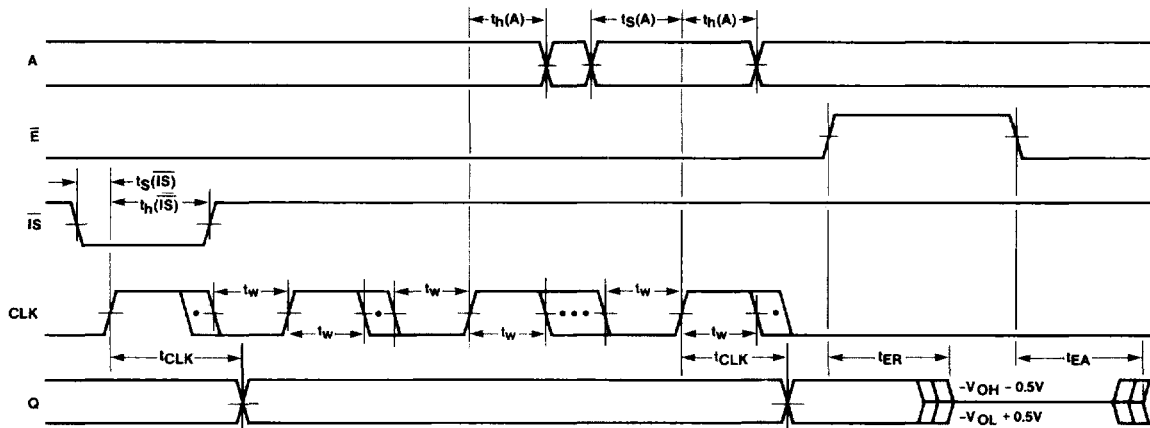
Switching Characteristics Over Operating Conditions and using Standard Test Load

SYMBOL	PARAMETER	TYP†	MILITARY				COMMERCIAL				UNIT
			53RA1681A		53RA1681		63RA1681A		63RA1681		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CLK}	Clock to output Delay	10	20	25	15	20	ns				
t_{EA}	Enable to output access time (\bar{E})	15	30	35	25	30	ns				
t_{ER}	Disable to output recovery time (\bar{E})	15	30	35	25	30	ns				

† Typical at 5.0 V V_{CC} and 25°C T_A .

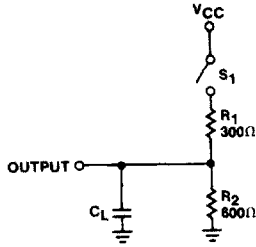
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Definition of Waveforms



- NOTES: 1. Input pulse amplitude 0 V to 3.0 V.
 2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
 3. Input access measured at the 1.5 V level.
 4. Switch S_1 is closed. $C_L = 30$ pF and outputs measured at 1.5 V output level for all tests except t_{EA} and t_{ER} .
 5. t_{EA} is measured at the 1.5 V output level with $C_L = 30$ pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.
 t_{ER} is tested with $C_L = 5$ pF. S_1 is open for "1" to high impedance test, measured at $V_{OH} - 0.5$ V output level; S_1 is closed for "0" to high impedance test measured at $V_{OL} + 0.5$ V output level.

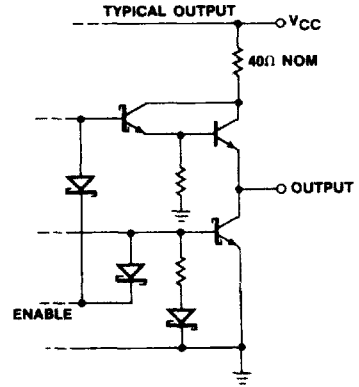
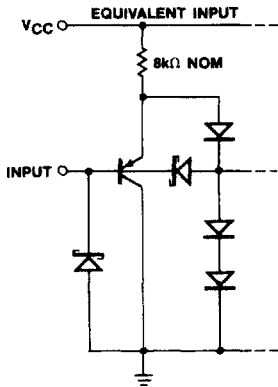
Switching Test Load



Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Schematic of Inputs and Outputs



Commercial Programmers

Monolithic Memories PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine.

ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember — The best PROMs available can be made unreliable by improper programming techniques.

PROM PROGRAMMING EQUIPMENT INFORMATION

SOURCE AND LOCATION	Data I/O Corp. 10525 Willows Rd. N.E. Redmond, WA 98073	Digelec Inc. 586 Weddell Dr. Suite 1 Sunnyvale, CA 94089
	Kontron Electronics, Inc. 630 Price Ave. Redwood City, CA 94063	Stag Microsystems Inc. 528-5 Weddell Dr. Sunnyvale, CA 94089

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Metal Mask Layout

