

APPLICATIONS

- High Frequency Applications.
- High Power Choppers And Inverters.
- Welding.
- Ultrasonic Generators.
- Induction Heating.
- 400Hz UPS.
- PWM Inverters.

KEY PARAMETERS

V_{DRM}	1400V
$I_{T(RMS)}$	370A
I_{TSM}	2000A
dV/dt	1000V/ μ s
dI/dt	1000A/ μ s
t_q	7.0 μ s

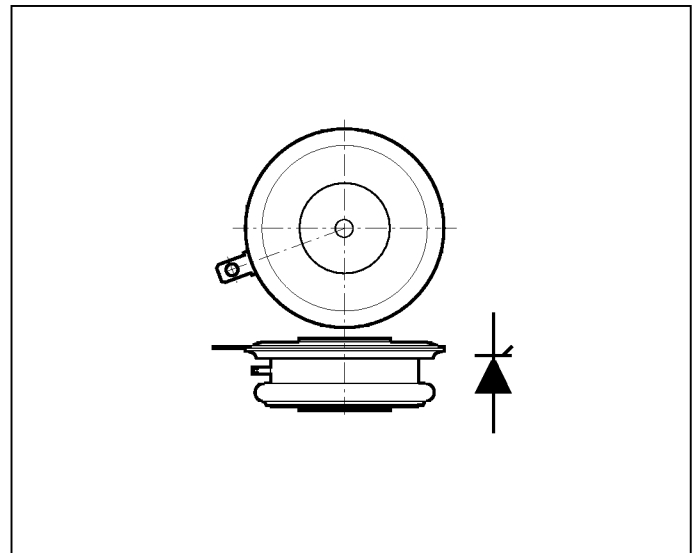
FEATURES

- Low Loss Asymmetrical Diffusion Structure.
- High Interdigitated Amplifying Gate.
- Gate Assisted Turn-off With Exclusive Bypass Diode.
- Fully Characterised For Operation up to 40kHz..
- Directly Compatible With 220-480 A.c. Mains..

VOLTAGE RATINGS

Type Number	Repetitive Peak Off-state Voltage V_{DRM} V	Repetitive Peak Reverse Voltage V_{RRM} V
TA329 14 Q	1400	10
TA329 12 Q	1200	10
TA329 10 Q	1000	10

Lower voltage grades available.



Outline type code: MU86. See package outlines for further information.

CURRENT AND SURGE RATINGS

Symbol	Parameter	Conditions	Max.	Units
Double Side Cooled				
$I_{T(RMS)}$	RMS value	Half sine wave, duty cycle 50%, $T_{case} = 80^{\circ}C$, $T_j = 125^{\circ}C$.	370	A
I_{TSM}	Surge (non-repetitive) on-state current	$T_j = 125^{\circ}C$, $t_p = 1ms$, $V_R = 0$	2000	A
I^2t	I^2t for fusing	$t_p \geq 10ms$	20×10^3	A ² s

THERMAL AND MECHANICAL DATA

Symbol	Parameter	Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance - junction to case	Double side cooled	dc	-	0.085	°C/W
		Single side cooled	Anode dc	-	0.153	°C/W
			Cathode dc	-	0.204	°C/W
$R_{th(c-h)}$	Thermal resistance - case to heatsink	Clamping force 4.0kN with mounting compound	Double side	-	0.02	°C/W
			Single side	-	0.04	°C/W
T_{vj}	Virtual junction temperature	On-state (conducting)		-	135	°C
		Reverse (blocking)		-	125	°C
T_{stg}	Storage temperature range			-40	150	°C
-	Clamping force			3.6	4.4	kN

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Conditions		Min.	Max.	Units
V_{TM}	Maximum on-state voltage	At 600A peak, $T_{case} = 125^{\circ}C$		-	2.5	V
I_{RRM}	Peak reverse current	At V_{RRM} , $T_{case} = 125^{\circ}C$		-	30	mA
I_{DRM}	Off-state current	At V_{DRM} , $T_{case} = 125^{\circ}C$		-	1	mA
dV/dt	Maximum linear rate of rise of off-state voltage	To 60% V_{DRM} , $T_j = 125^{\circ}C$, Gate open circuit		-	1000	V/ μ s
dI/dt	Rate of rise of on-state current	Gate source 20V, 20 Ω $t_r \leq 5\mu$ s.	Non-repetitive	-	1000	A/ μ s
			Repetitive	-	500	A/ μ s
$t_q^{\dagger}$	Max. gate assisted turn-off time (with feedback diode)	$T_j = 125^{\circ}C$, $I_{T(PK)} = 200A$, $t_p = 25\mu$ s (half sine wave), $V_R = DF451$ Diode voltage drop, dV/dt = 600V/ μ s (linear to 60% V_{DRM}), $V_{GK} = -5V$		-	7	μ s
t_q	Max. turn-off time (with feedback diode)	$T_j = 125^{\circ}C$, $I_{TM} = 100A$, $t_p > 100\mu$ s, dI _R /dt = 30A/ μ s, $V_R = 1V$, dV/dt = 600V/ μ s (linear to 60% V_{DRM}), Gate open.		-	10	μ s

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Conditions	Typ.	Max.	Units
V_{GT}	Gate trigger voltage	$V_{DWM} = 12V, R_L = 3\Omega, T_{case} = 25^\circ C$	-	4	V
I_{GT}	Gate trigger current	$V_{DWM} = 12V, R_L = 3\Omega, T_{case} = 25^\circ C$	-	250	mA
V_{RGM}	Peak reverse gate voltage	-	-	7	V
I_{FGM}	Peak forward gate current	-	-	10	A
P_{GM}	Peak gate power	-	-	50	W
$P_{G(AV)}$	Average gate power	-	-	15	W

CURVES

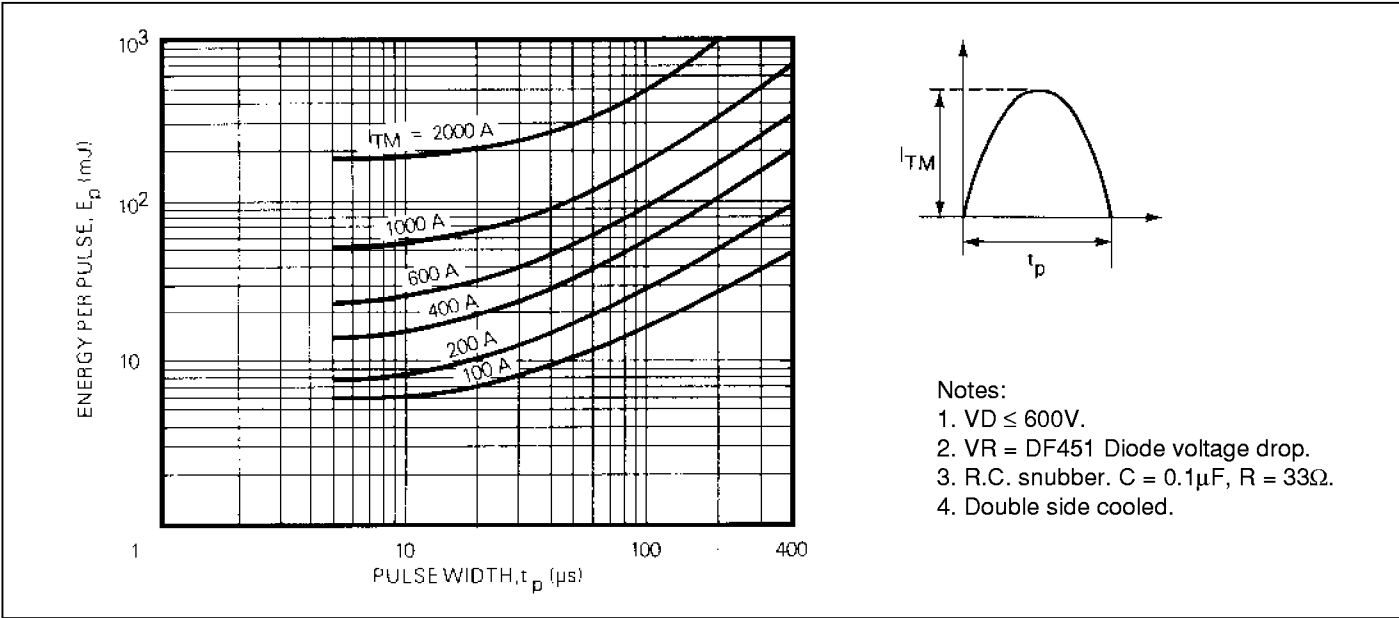


Fig.1 Energy per pulse for sinusoidal pulses.

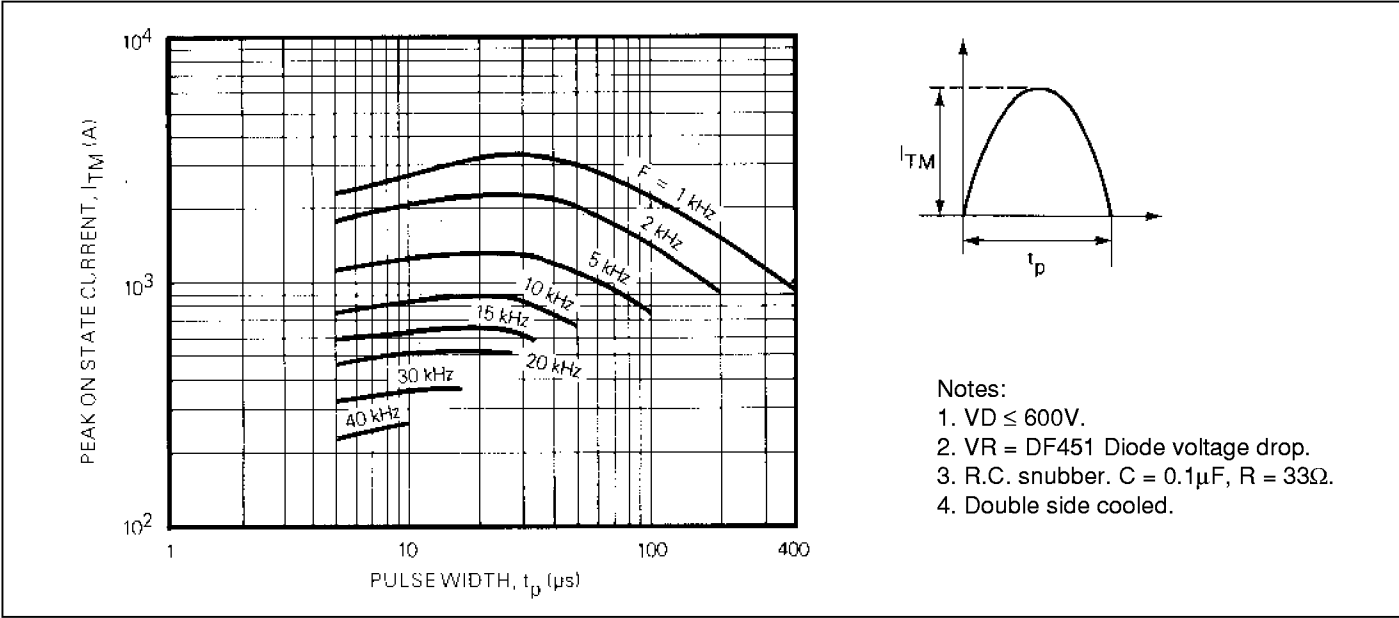
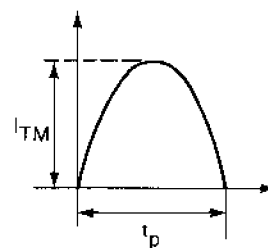
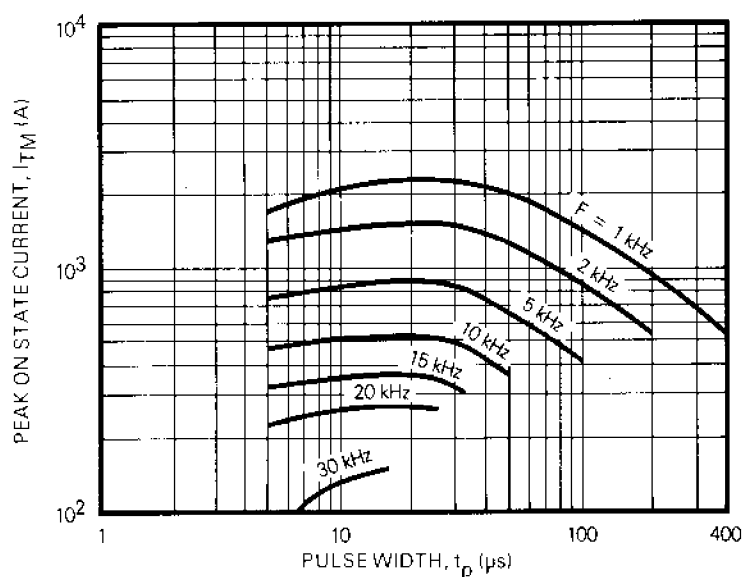


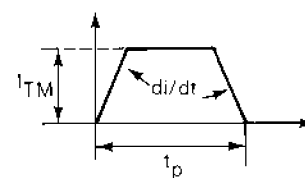
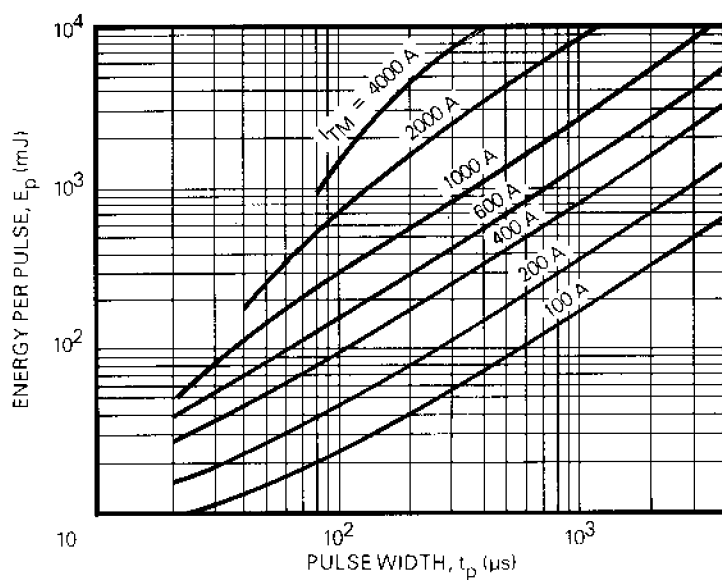
Fig.2 Maximum allowable peak on-state current vs pulse width for $T_{case} = 65^\circ C$.



Notes:

1. $V_D \leq 600V$.
2. V_R = DF451 Diode voltage drop.
3. R.C. snubber. $C = 0.1\mu F$, $R = 33\Omega$.
4. Double side cooled.

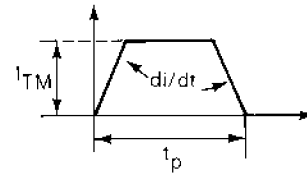
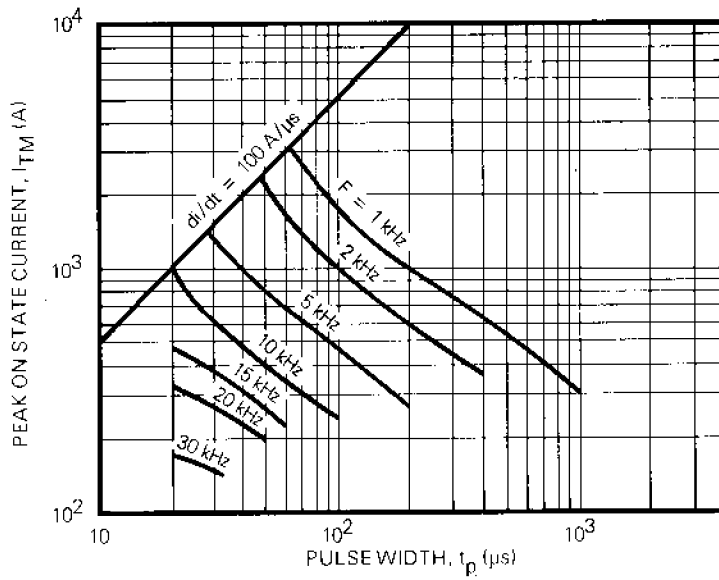
Fig.3 Maximum allowable peak on-state current vs pulse width for $T_{case} = 90^\circ C$.



Notes:

1. $di/dt = 100A/\mu s$.
2. $V_D \leq 600V$.
3. V_R = DF451 Diode voltage drop.
4. R.C. snubber. $C = 0.1\mu F$, $R = 33\Omega$.
5. Double side cooled.

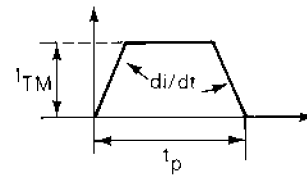
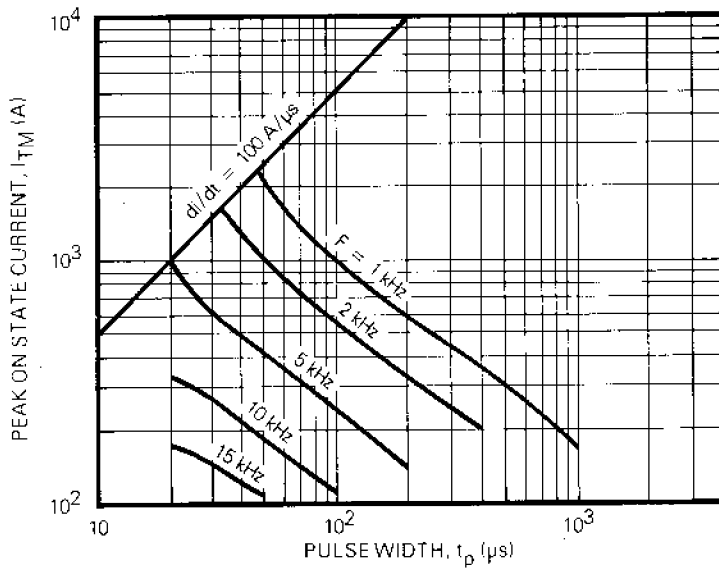
Fig.4 Energy per pulse for trapezoidal pulses



Notes:

1. $di/dt = 100 \text{ A}/\mu\text{s}$.
2. $V_D \leq 600 \text{ V}$.
3. $V_R = \text{DF451 Diode voltage drop}$.
4. R.C. snubber. $C = 0.1 \mu\text{F}$, $R = 33 \Omega$.
5. Double side cooled.

Fig.5 Maximum allowable peak on-state current vs pulse width for $T_{\text{case}} = 65^\circ\text{C}$.



Notes:

1. $di/dt = 100 \text{ A}/\mu\text{s}$.
2. $V_D \leq 600 \text{ V}$.
3. $V_R = \text{DF451 Diode voltage drop}$.
4. R.C. snubber. $C = 0.1 \mu\text{F}$, $R = 33 \Omega$.
5. Double side cooled.

Fig.6 Maximum allowable peak on-state current vs pulse width for $T_{\text{case}} = 90^\circ\text{C}$.

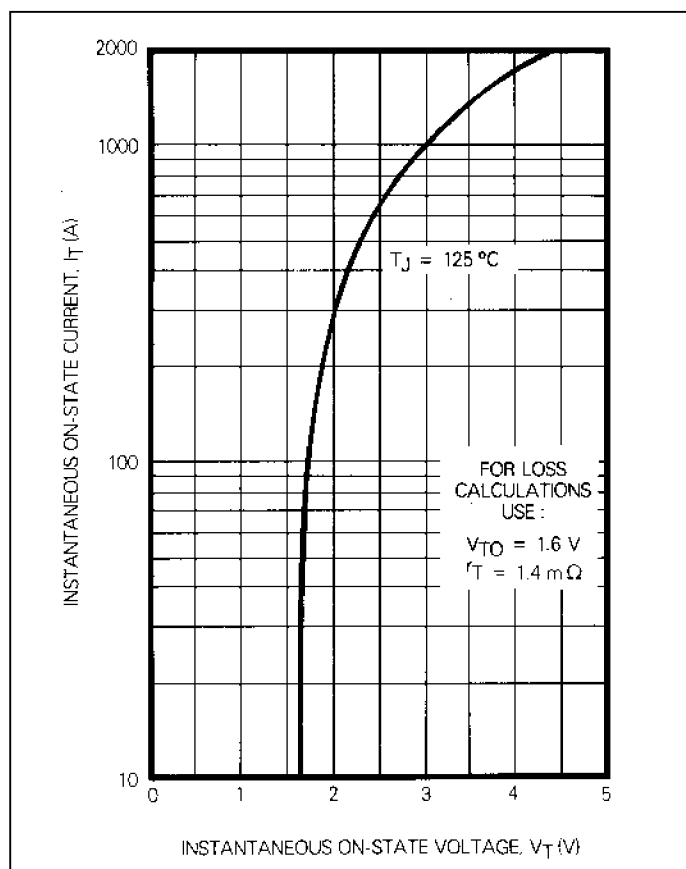


Fig.7 Maximum on-state conduction characteristic

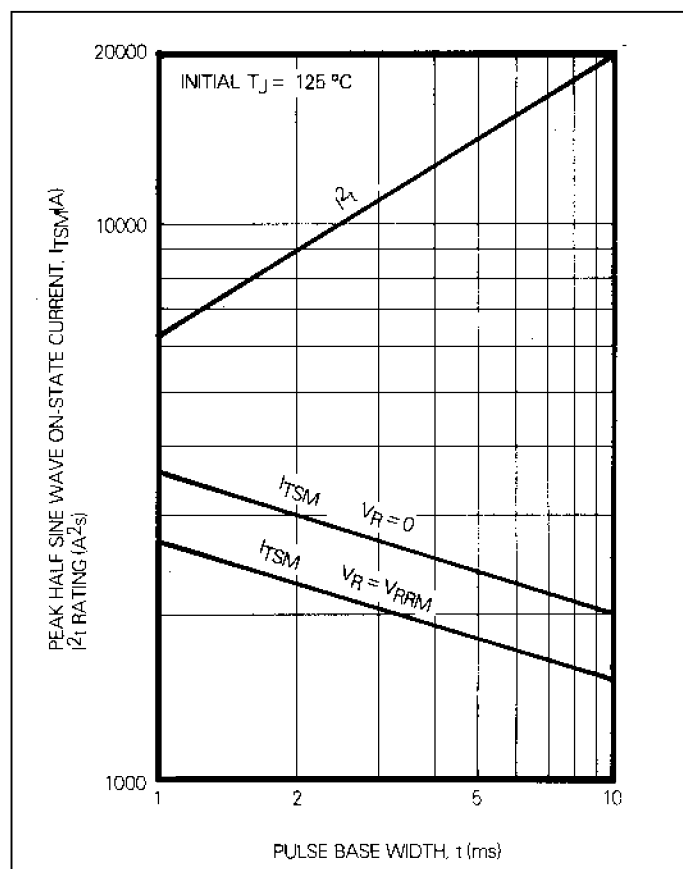
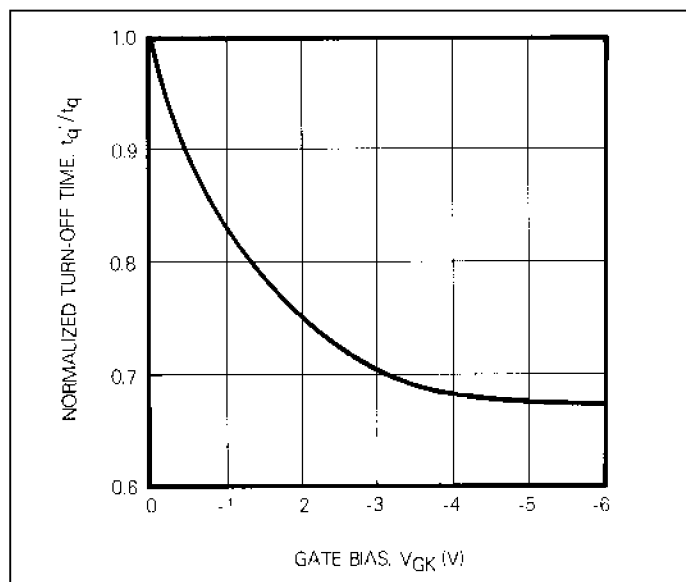
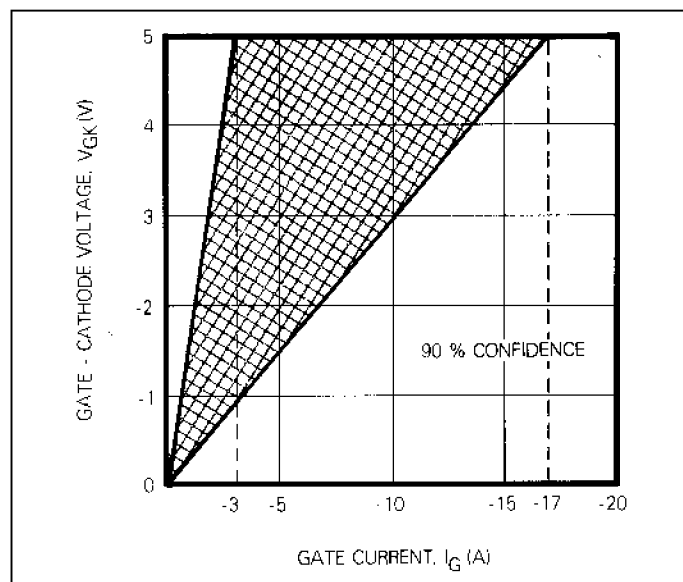
Fig.8 Non-repetitive sub-cycle surge on-state current and P_t rating.Fig.9 Typical variation of effective turn-off time ($t_q^†$) with negative gate bias.

Fig.10 Reverse gate characteristics

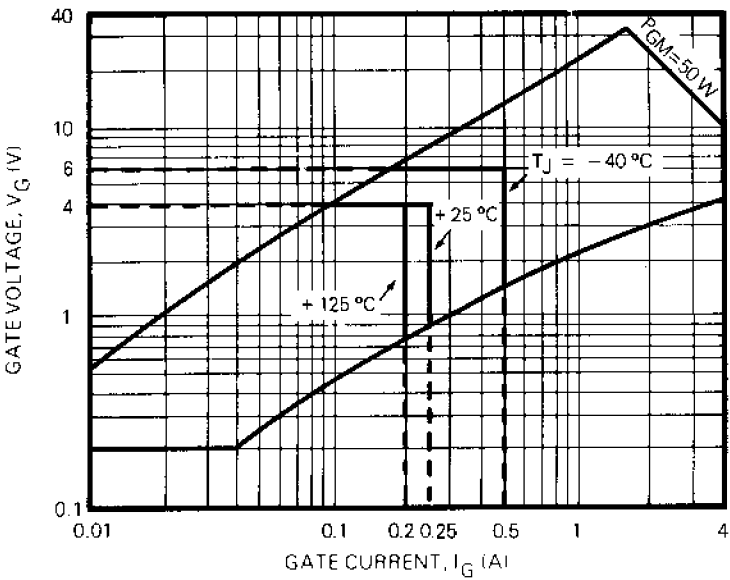


Fig.11 Gate trigger characteristics

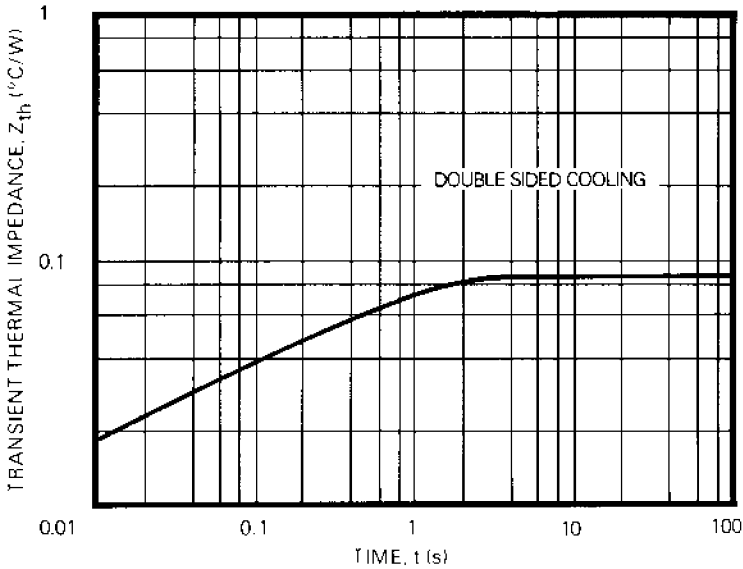
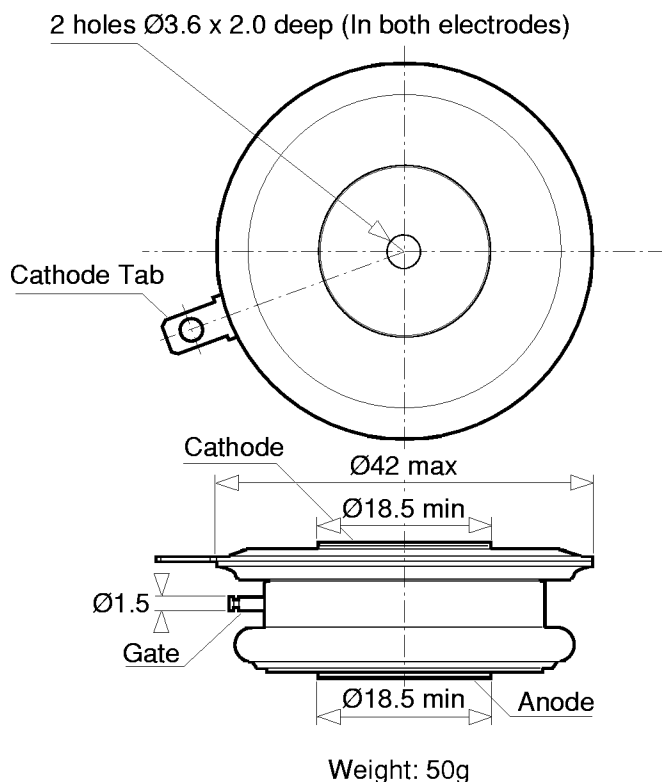


Fig.12 Transient thermal impedance - junction to case

PACKAGE DETAILS - MU86

For further package information, please contact your local Customer Service Centre. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



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