EK23C4000

512K x 8 / 256K x 16 CMOS Mask ROM

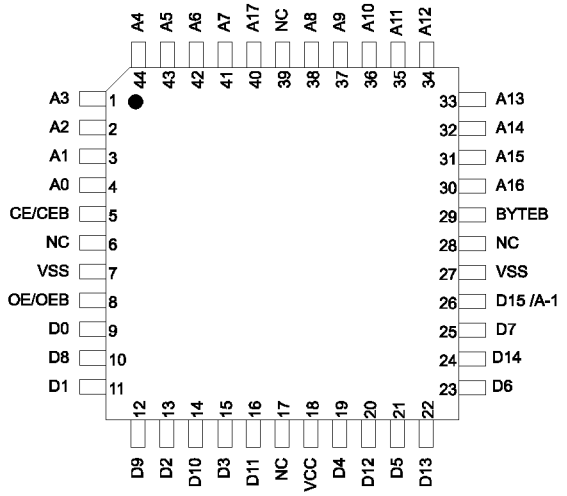
Features

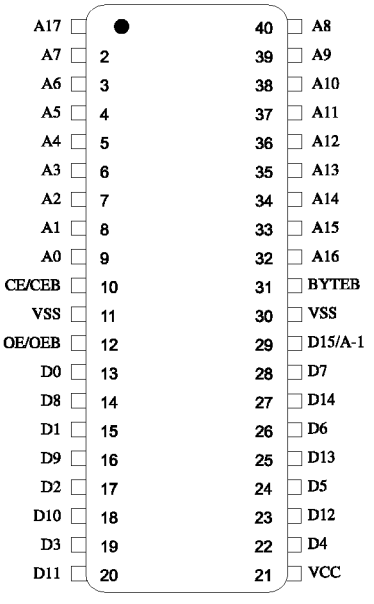
- Address Access Times
  100ns, 120ns, 150ns, 200ns
- Operating Current
  60 mA
- Standby Current
  100 mA
- Single 5V ±10% Power Supply
- Configurations
  Byte mode: 512K x 8
  Word mode: 256K x 16
- TTL Compatible
- Package Options
  44 pin QFP
  40 pin SOP
  40 pin 600 mil PDIP
  Dice Form

Description

The EK23C4000 is a 4 megabit mask programmable read-only-memory organized as 524,288 x 8 bits or 262,144 x 16 bits. The organization is controlled by the BYTEB signal. It is designed for easy interface to all microprocessors and other applications that need high density non-volatile memory storage. The active state of chip enable and output enable are mask programmable to active high or low. The device is fabricated using high performance CMOS technology.

Pin Configuration





EUREKA MICROELECTRONICS, INC.
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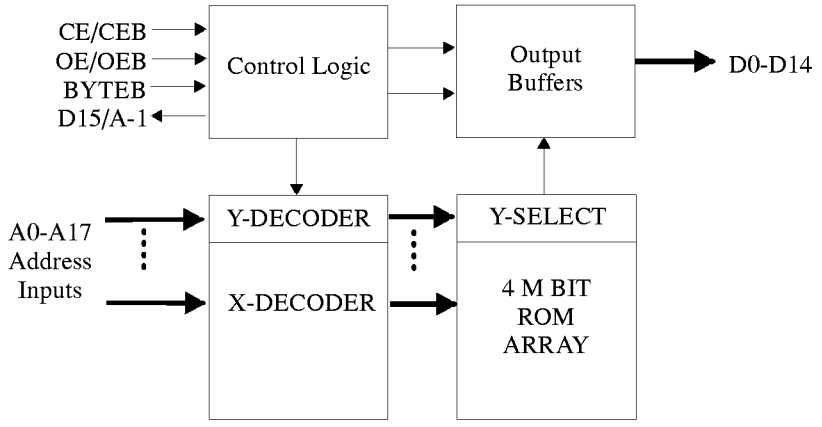
Pin Assignment

Symbol	Description
A0-A17	Address Inputs
D0-D14	Data Inputs / Outputs
D15/A-1	D15 (Word Mode) / LSB Address (Byte Mode)
OE/OEB	Output Enable
CE/CEB	Chip Enable
BYTEB	WORD/BYTE Selection
NC	No Connect
Vcc	Power Supply
Vss	Ground

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Power Supply Voltage	V_{CC}	-0.5 to 7.0	V
Input Voltage	V_{IN}	-0.5 to Vcc + 0.5	V
Output Voltage	V_{OUT}	-0.5 to Vcc + 0.5	V
Operating Temperature	T_{OPR}	0 to +70	°C
Storage Temperature	T_{STG}	-55 to +150	°C
Power Dissipation	P_D	0.5	W

Stresses greater than those listed under Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth Table

Byte Mode (BYTEB=VSS; D8-D14 = High-Z)

CE / CEB	OE / OEB	D15 / A-1	Mode	D0-D7	Supply Current
Inactive	X	X	Deselected	High - Z	Standby (ICC2)
Active	Inactive	X	Deselected	High - Z	Operating (ICC1)
Active	Active	L	Selected	Low Byte	Operating (ICC1)
Active	Active	H	Selected	High Byte	Operating (ICC1)

Word Mode (BYTEB=VCC)

CE / CEB	OE / OEB	D15 / A-1	Mode	D0-D14	Supply Current
Inactive	X	High - Z	Deselected	High - Z	Standby (Icc2)
Active	Inactive	High - Z	Deselected	High - Z	Operation (Icc1)
Active	Active	Data Out	Selected	Data Out	Operation (Icc1)

DC Characteristics

(T_A =0°C to + 70°C; V_{CC} = +5V ±10% unless otherwise noted; Note 1)

Description	Symbol	Conditions	Min	Max	
Input Low Voltage	V_{IL}		-0.5	0.8	V
Input High Voltage	V_{IH}		2.2	Vcc+0.5	V
Input Leakage Current	I_{LI}	V_{IN} = Vss to V_{CC}	-	10	µA
Output Leakage Current	I_{LO}	V_{IN}=Vss to V_{CC}; Outputs Deselected	-	10	µA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA	2.4	-	V
Operating Supply Current	ICC1	Note 1	-	60	mA
Standby Supply Current	ICC2	CEB = VIH or CE = VIL	-	1	mA
Power Down Current	ICC3	CEB ≥ V_{CC}-0.2V or CE ≤ Vss+0.2V	-	100	µA

AC Characteristics

(TA = 0 to +70°C, VCC = 5V ±10%)

DESCRIPTION		-10		-12		-15		-20			
	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
Cycle Time	t CYC	100	-	120	-	150	-	200	-	ns	
Address Access Time	t AA	-	100	-	120	-	150	-	200	ns	
Chip Enable Access Time	t CE	-	100	-	120	-	150	-	200	ns	2
Output Enable Access Time	t OE	-	60	-	70	-	80	-	90	ns	3
Output Hold From Addrees Change	t OH	10	-	10	-	10	-	10	-	ns	
Output to Low-Z Delay	t LZ	0	-	0	-	0	-	0	-	ns	
Chip Disable to High-Z	t HZ	-	70	-	70	-	70	-	70	ns	4
BYTE Access Time	t BHA	-	100	-	120	-	150	-	200	ns	
BYTE Output Hold Time	t OHB	0	-	0	-	0	-	0	-	ns	
BYTE Output Delay Time	t BHZ	-	70	-	70	-	70	-	70	ns	
BYTE Output Setup Time	t BLZ	10	-	10	-	10	-	10	-	ns	

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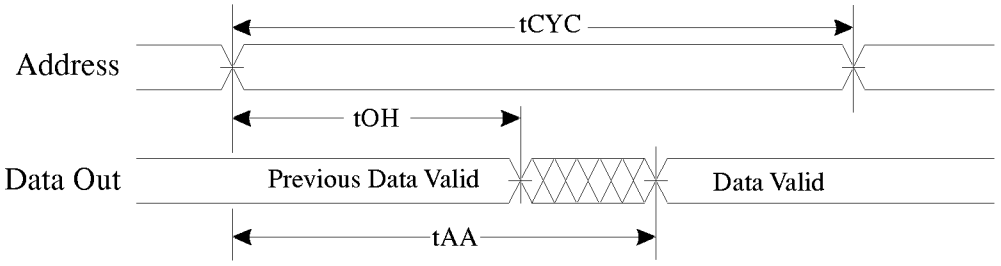
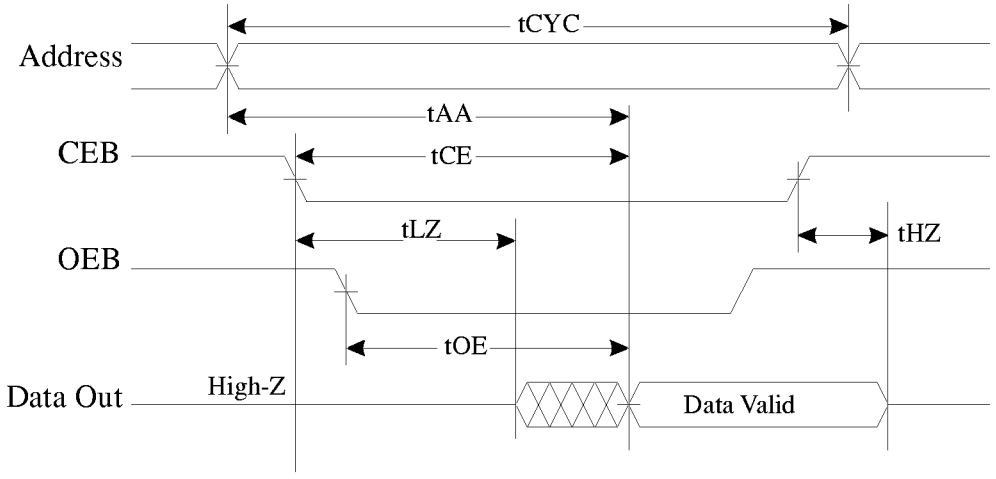
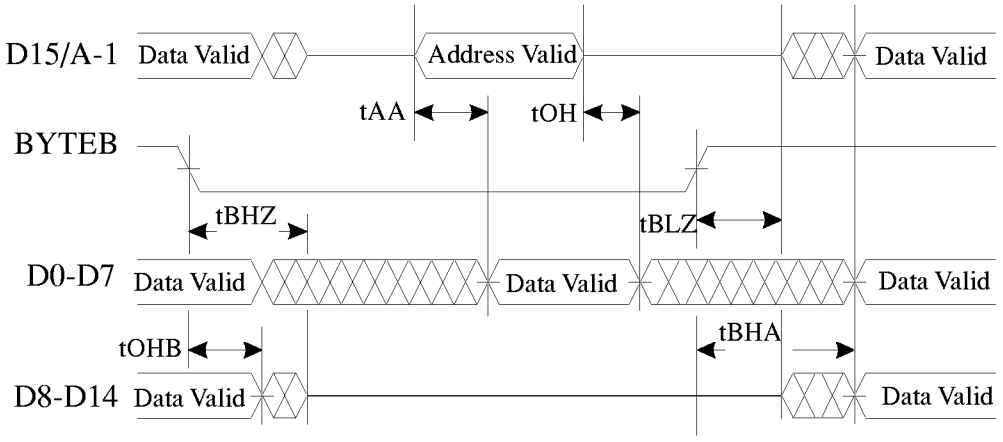
Address Access



Chip Enable Access



Byte / Word Switching



AC Test Conditions

(TA = 0 to +70° C, VCC = 5V ±10%, see Fig.1)

Parameter	Symbol	Conditions	Units
Input Pulse High Level	VIH	2.4	V
Input Pulse Low Level	VIL	0.4	V
Input Rise Time	TR	10	ns
Input Fall Time	TF	10	ns
Input and Output Timing Reference Level		1.5	V

AC Test Loads

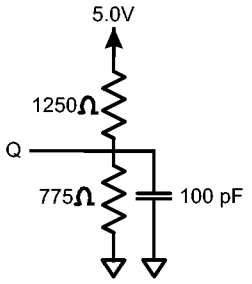


Figure 1A - AC Test Load

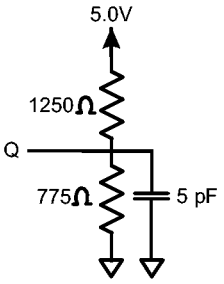


Figure 1B - High-Z Test Load

Notes:

1. Measured with device selected at f=5 Mhz and outputs unloaded
2. CE and CEB are represented by CEB in this data sheet. CE is of the opposite polarity of CEB in the timing diagrams.
3. OE and OEB are represented by OEB in this data sheet. OE is of the opposite polarity of OEB in the timing diagrams.
4. Measured at ±500mv from steady state with the High-Z load.

Ordering Information

(Order by Complete Part Number)

EK 23C4000 X - Y

- Eureka Prefix
- Part Number
- Package Type
  - Q = 44 pin QFP
  - S = 40 pin SOP
  - K = 600 mil PDIP
- 10=100ns, 12=150ns, 15=150ns, 20=200ns

EK D 23C4000

- Eureka Prefix
- Die Form
- Part Number

Note: Please indicate active states of CE/CEB and OE/OEB on ordering Form

MASK ROM Ordering Information Sheet

EUREKA ROM Code NO.:

KIT with : _____ EUREKA ROM

Part NO.:

1. Customer:	Agent:
2. Access Time: 5V: ( )100ns ( )120ns ( )150ns ( )200ns 3V: ( )200ns ( )250ns ( )300ns	5. Output Organization: x 8 bits (Byte Mode) x 16 Bits (Word Mode) x8 / x16 bits (Pin Selection)
3. Package Type: DIP: ( ) 28 ( ) 32 ( ) 40 ( ) 42 SOP: ( ) 28 ( ) 32 ( ) 44 QFP: ( ) 44 ( ) 64 ( ) Die Form ( ) Wafer Form	6. Top Marking : ( ) EUREKA standard ( ) Customer Specification
4. Control Pin Information: ( )CE ( ) CEB ( )OE ( ) OEB	7. Application

8. Checksum of each address range: Please list the file name or label name of the ROM code isks or EPROMs. (please use attachment if necessary)

Mask ROM address	file/label name	D0-D7 Checksum	

9. Total Checksum:

10. When Should EUREKA go into production? ( ) After receiving customer's ROM code hard-copy list OR ( ) After customer approves the EUREKA generated hard-copy list	11. Special Requirement:

Signatures:

Customer : _____ EUREKA Agent: _____ EUREKA Sales: _____

Date: _____ Date: _____ Date: _____

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