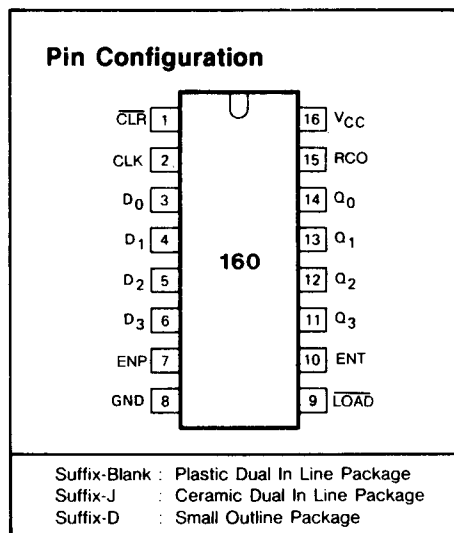


GD54/74HC160, GD54/74HCT160

SYNCHRONOUS DECADE COUNTER WITH ASYNCHRONOUS CLEAR

General Description

These devices are identical in pinout to the 54/74LS160. They contain a 4-bit decade counter consisting of four flip-flops. All flip-flops are clocked simultaneously on the positive edge of the clock input. Counters may be preset using the load input at the rising edge of clock. All the counters may be cleared asynchronously by utilizing the clear input. When the clear is taken low the counter is cleared immediately regardless of the clock. The HC/HCT 160 is similar in function to the HC/HCT 162 which is cleared synchronously. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications



Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current: 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

OPERATING MODE	INPUTS					OUTPUTS		
	CLR	CLK	ENP	ENT	LOAD	D _n	Q _n	RCO
reset (clear)	L	↑	X	X	X	X	L	L
parallel load	H	↑	X	X	L	L	L	L
	H	↑	X	X	L	h	H	*
count	H	↑	h	h	h	X	count	*
hold (do nothing)	H	X	L	X	h	X	q _n	*
	H	X	X	L	h	X	q _n	L

Note to function table

* The RCO outputs is HIGH when ENT is HIGH and the counter is at terminal count (HLLH)
 H = HIGH voltage level
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CLK transition
 L = LOW voltage level
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CLK transition
 q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CLK transition
 X = don't care
 ↑ = LOW-to-HIGH CLK transition

Logic Diagram

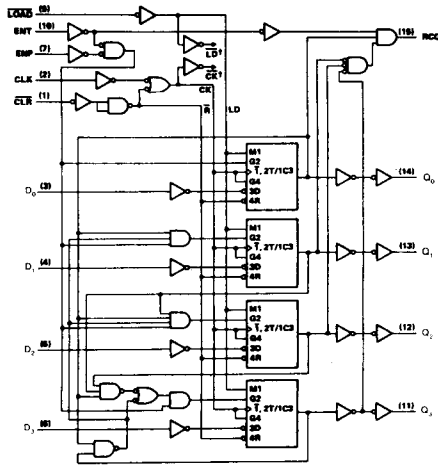


Fig. 1 Logic diagram

Output Sequence

Illustrated below is the following sequence:

1. Clear outputs to zero (HC/HCT 160 is asynchronous)
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit

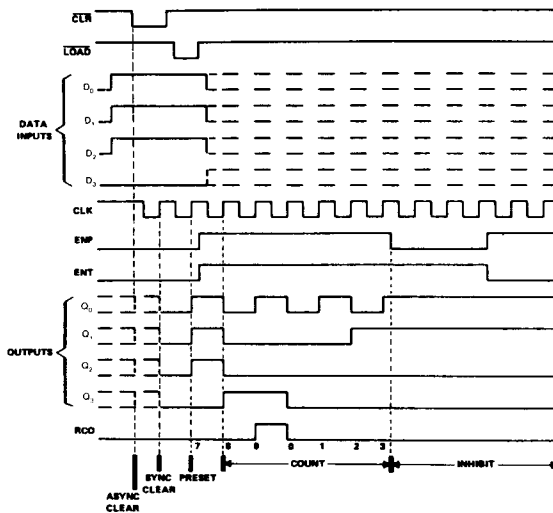


Fig. 2 Output sequence

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5 V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC160		GD54HC160		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.		
V _{IH}	HIGH level input Voltage		2.0	1.5			1.5		1.5		V	
			4.5	3.15		3.15		3.15				
			6.0	4.2		4.2		4.2				
V _{IL}	LOW level input voltage		2.0			0.3		0.3		0.3	V	
			4.5			0.9		0.9		0.9		
			6.0			1.2		1.2		1.2		
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0	1.9	2.0		1.9		1.9	V	
				4.5	4.4	4.5		4.4		4.4		
		or V _{IL}	I _{OH} =-4mA I _{OH} =-5.2mA	4.5	3.98	4.3		3.84		3.7		
				6.0	5.48	5.2		5.34		5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0			0.1		0.1		V	
				4.5			0.1		0.1			0.1
		or V _{IL}	I _{OL} =4mA I _{OL} =5.2mA	4.5		0.17	0.26		0.33			0.4
				6.0		0.15	0.26		0.33			0.4
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA	
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA	

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT160		GD54HCT160		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.		
V _{IH}	HIGH level input Voltage		4.5								V	
			to	2.0			2.0		2.0			
			5.5									
V _{IL}	LOW level input voltage		4.5								V	
			to			0.8		0.8		0.8		
			5.5									
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5		4.4		4.4	V	
				4.5	3.98	4.3		3.84		3.7		
		or V _{IL}	I _{OH} =-4mA	4.5								
				6.0								
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1		0.1		V	
				4.5			0.17	0.26		0.33		
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26		0.33			0.4
				6.0								
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA	
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA	

GD54/74HC160, GD54/74HCT160

Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V _{CC} (V)	T _A =25°C			GD74HC160		GD54HC160		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _w	Pulse width	$\overline{\text{CLR}}$ low, CLK	2.0	80			100		120		ns
			4.5	16			20		24		
			6.0	14			17		20		
t _{su}	Setup time	D _n to CLK	2.0	80			100		120		ns
			4.5	16			20		27		
			6.0	14			17		20		
		$\overline{\text{LOAD}}$ to CLK	2.0	135			170		205		ns
			4.5	25			31		40		
			6.0	22			29		35		
ENP, ENT to CLK	2.0	135			250		300		ns		
	4.5	27			50		60				
	6.0	23			43		51				
t _{rec}	Recovery time	$\overline{\text{CLR}}$ to CLK	2.0	100			125		150		ns
			4.5	20			25		30		
			6.0	17			21		26		
t _h	Hold time	All sync. input to CLK	2.0	0			0		0		ns
			4.5	0			0		0		
			6.0	0			0		0		

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V _{CC} (V)	T _A =25°C			GD74HC160		GD54HC160		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f _{max}	Maximum clock pulse frequency		2.0	6	14		5		4.2		MHz
			4.5	31	40		25		21		
			6.0	36	44		29		25		
t _{PLH} / t _{PHL}	Propagation Delay Time CLK to RCO		2.0		60	200		250		305	ns
			4.5		20	40		52		63	
			6.0		16	31		43		52	
t _{PLH} / t _{PHL}	Propagation Delay Time CLK to Qn		2.0		58	180		225		275	ns
			4.5		18	34		43		53	
			6.0		16	28		37		46	
t _{PLH} / t _{PHL}	Propagation Delay Time ENT to RCO		2.0		45	140		180		215	ns
			4.5		15	28		36		43	
			6.0		13	25		32		38	
t _{PLH} / t _{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to Qn		2.0		58	200		255		305	ns
			4.5		18	35		46		56	
			6.0		16	30		42		51	
t _{PLH} / t _{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to RCO		2.0		60	210		265		315	ns
			4.5		20	40		51		62	
			6.0		18	34		45		55	
t _{TLH} / t _{THL}	Output Transition Time		2.0		38	75		95		110	ns
			4.5		7	15		19		22	
			6.0		6	13		16		19	

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V _{CC} (V)	T _A =25 °C			GD74HCT160		GD54HCT160		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _w	Pulse width	$\overline{\text{CLR}}$ low. CLK	4.5	20			24		28		ns
t _{su}	Setup time	D _n to CLK	4.5	20			24		28		ns
		$\overline{\text{LOAD}}$ to CLK	4.5	30			38		45		ns
		ENP, ENT to CLK	4.5	30			54		64		ns
t _{rec}	Recovery time	$\overline{\text{CLR}}$ to CLK	4.5	24			29		34		ns
t _h	Hold time	All sync, input to CLK	4.5	0			0		0		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V _{CC} (V)	T _A =25 °C			GD74HCT160		GD54HCT160		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f _{max}	Maximum clock pulse frequency		4.5	16	28		13		11		MHz
t _{PLH} / t _{PHL}	Propagation Delay Time CLK to RCO		4.5		26		56		67		ns
t _{PLH} / t _{PHL}	Propagation Delay Time CLK to Qn		4.5		24		47		57		ns
t _{PLH} / t _{PHL}	Propagation Delay Time ENT to RCO		4.5		21		40		47		ns
t _{PLH} / t _{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to Qn		4.5		24		50		60		ns
t _{PLH} / t _{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to RCO		4.5		26		55		67		ns
t _{TLH} / t _{THL}	Output Transition Time		4.5		7		19		22		ns

AC Waveforms

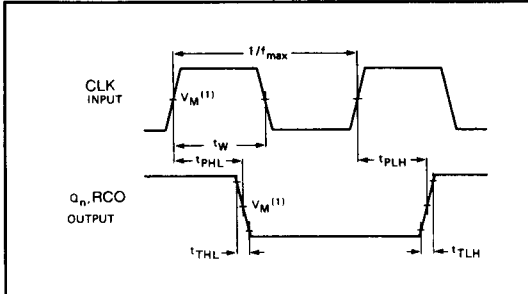


Fig. 3 Waveforms showing the clock (CLK) to outputs (Q_n , RCO) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

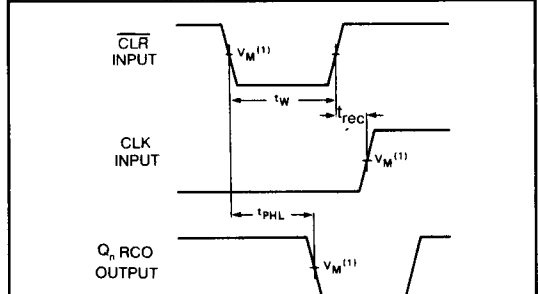


Fig. 4 Waveforms showing the master \overline{CLR} pulse width, the master clear to output (Q_n , RCO) propagation delays and the master clear to clock (CLK) recovery time.

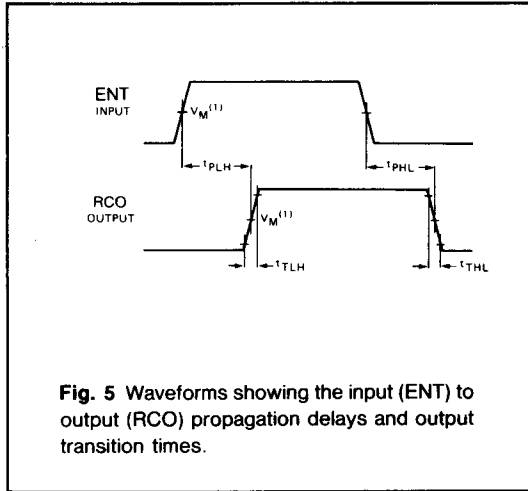


Fig. 5 Waveforms showing the input (ENT) to output (RCO) propagation delays and output transition times.

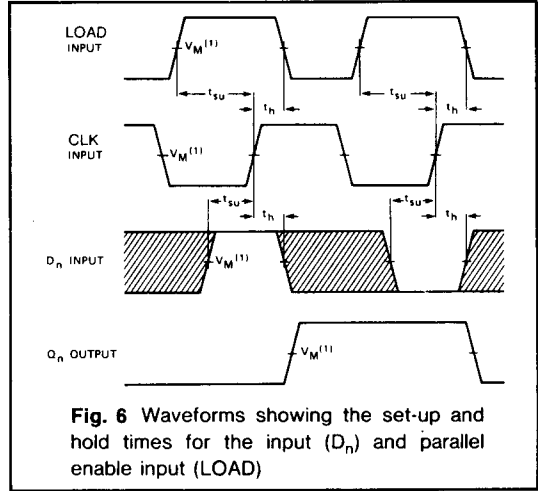


Fig. 6 Waveforms showing the set-up and hold times for the input (D_n) and parallel enable input (LOAD)

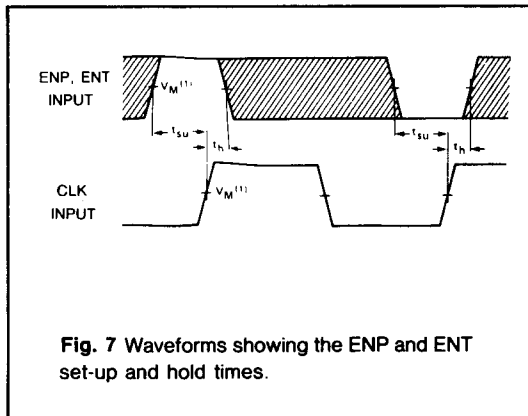


Fig. 7 Waveforms showing the ENP and ENT set-up and hold times.

Note to Figs 6 and 7

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_i = \text{GND to } V_{CC}$;
- HCT : $V_M = 1.3V$; $V_i = \text{GND to } 3V$.