



V340HPC A0 High Integration PCI System Controller for 64-bit MIPS® Processors

1.1 About the V340HPC

- Highly scalable, 64-bit PCI system controller for high performance embedded systems
- Glueless interface to MIPS R4000/R5000/R7000 family members with a 64-bit SysAD bus width, up to 100 MHz
 - Support for QED, NEC, IDT, Sandcraft, and other 64-bit MIPS-based processors
- Local bus clock speeds: 100 MHz, 83 MHz, and 75 MHz—all with external cache support
- Multiple outstanding reads with out-of-order return support for the RM7000™ processor
- Flexible operation supports either a single 64-bit, 66 MHz PCI bus or dual 32-bit, 66 MHz buses
- Integrated non-transparent PCI-to-PCI bridge
- 8 kB internal SRAM scratchpad for immediate access from the local processor
- Support for 32-bit and 64-bit PCI, up to 66 MHz
- Configurable for system host, bus master, and target operation
- PCI-to-local and local-to-PCI address translation
- Three PCI-to-local and three local-to-PCI data transfer apertures
- 6 kByte FIFO storage
- Integrated SDRAM controller
 - Support for up to 2 Gbyte of SDRAM with optional ECC protection
 - Support for discrete SDRAMs, standard DIMM(s), registered DIMM(s), and serial presence detect
 - Support for 16 Mbit–256 Mbit SDRAMs
 - 4-, 8-, 16-, or 32-bit devices
 - Integrated multi-channel prefetch buffers
- Four independent DMA channels with chaining, multiprocessor support, and fly-by DMA support
- Up to 2 kByte burst access on both local and PCI interfaces

- On-the-fly byte order (endian) conversion with automatic byte swapping
- Programmable chip select/peripheral device strobe generation
- I₂O-Ready™ ATU and messaging unit
- Interrupt controller with four configurable interrupt pins
- Four 32-bit general purpose timers
- 8-bit watchdog timer
- System heartbeat and bus watch timers
- UART serial interface
- 3.3 V operation with 5 V tolerant input
- 456-pin BGA (Ball Grid Array) package
- Tri-directional mailbox registers with doorbell interrupts
- Power-on configuration via serial EEPROM

A block diagram illustrating a sample application using the V340HPC is shown in **Figure 1-1**.

NOTE V3 Semiconductor retains the rights to change documentation, specifications, or device functionality at any time without notice. Please verify that you have the latest copy of all documents before finalizing a design.

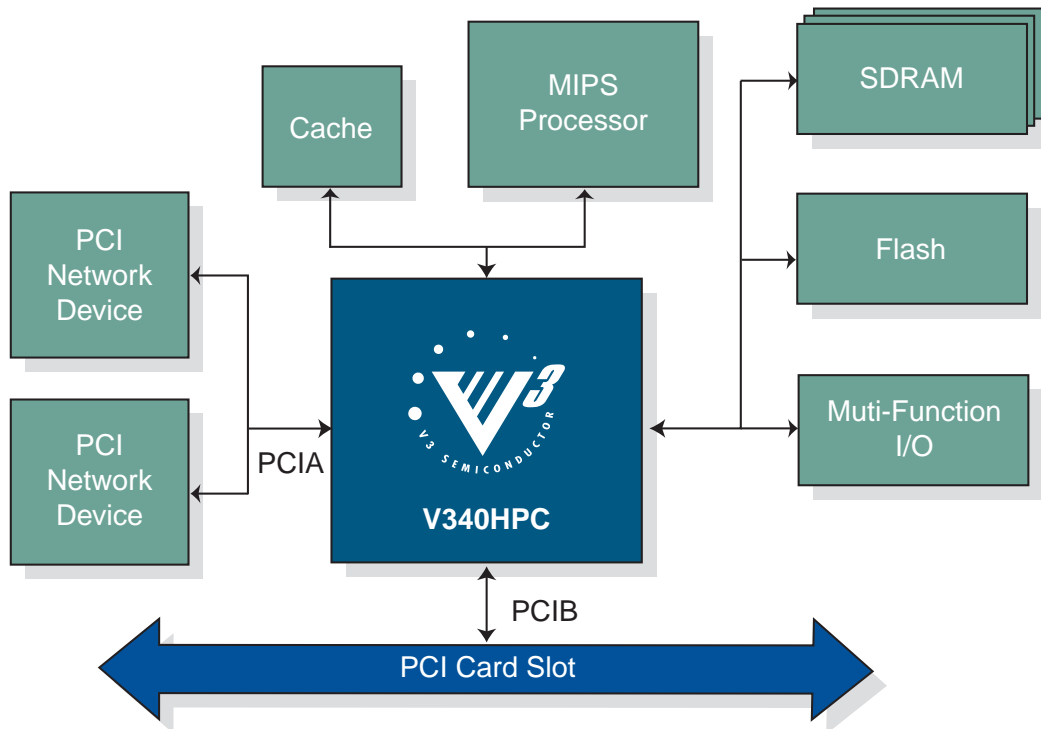


Figure 1-1: Example Application

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1.2 Product Codes

Table 1: Product Codes

Order Number	Package	Local Bus Frequency
V340HPC-100BPA0	456-pin BGA (Ball Grid Array)	100 MHz
V340HPC-83BPA0	456-pin BGA (Ball Grid Array)	83 MHz
V340HPC-75BPA0	456-pin BGA (Ball Grid Array)	75 MHz

1.3 Revision History

Table 2: Revision History

Revision Number	Date	Comments and Changes
1.00	Jan. 2001	Preliminary presilicon revision of data sheet.

1.4 Signal Descriptions and Pinouts

Table 3 lists the pin types found on the V340HPC.

Table 4 describes the function of all pins except for the PCI pins.

Table 5 describes the function of the PCI pins when the V340HPC is configured in 64-bit mode (PCIMODE = 1).

Table 6 describes the function of the PCI pins when the V340HPC is configured in 32-bit split-bus mode (PCIMODE = 0).

Table 3: Pin Types

Pin Type	Description
PCI I	PCI input only
PCI O	PCI output only
PCI I/O	PCI tri-state I/O
PCI I/O _D	PCI input with open drain output
I/O ₄	I/O pin with 4 mA output drive
I/O ₈	I/O pin with 8 mA output drive
I/O ₁₂	I/O pin with 12 mA output drive
I	input only
O ₄	output pin with 4 mA output drive
O ₈	output pin with 8 mA output drive
O ₁₀	output pin with 10 mA output drive
O ₁₂	output pin with 12 mA output drive

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Table 4: Signal Descriptions: All except for PCI pins

Signal	Type	Reset State	Description
MIPS System Bus Interface Signals			
SYSAD[63:0]	O ₈	Z	System Address/Data Bus
SYSCMD[8:0]	O ₈	Z	System Command/Data Identifier Bus
RELEASE	I		Release to signal the processor is releasing the bus to slave
$\overline{\text{WRRDY}}$	O ₈	Z	Write Ready to signal HPC can accept a processor request
$\overline{\text{VALIDIN}}$	O ₈	Z	Valid In indicates HPC is driving valid data on SYSAD and SYSCMD
VALIDOUT	I		Valid Out indicates the processor is driving valid address/data on SYSAD and SYSCMD bus
PRQST	I		Processor Request for requesting control of system interface
$\overline{\text{PACK}}$	O ₈	Z	Processor Acknowledge indicates HPC returns control of system interface back to processor
RSPSWAP	O ₈	Z	Response Swap HPC returns data to processor out of order
TCDOE	O ₈	Z	Tertiary Cache Data RAM Output Enable
TCTCE	O ₈	Z	Tertiary Cache Tag RAM Chip Enable
TCWORD[1:0]	O ₈	Z	Tertiary Cache Double Word Index
TCMATCH	O ₈	Z	Tertiary Cache Tag Match
LCLK	I		Local Clock
LRST	I		Local Reset
COLDRST	O ₁₂		Cold Reset
$\overline{\text{WARMRST}}$	O ₁₂		Warm Reset
VCCOK	O ₈		VCC is OK
Peripheral Bus Interface Signals			
ALE	O ₈	Z	Address Latch Enable
$\overline{\text{IOW}}$	O ₈	Z	IO Write
$\overline{\text{IOR}}$	O ₈	Z	IO Read
IOC[13:0]	I/O ₈	Z	IO Control
SDRAM Interface Signals			
MDATA[63:0]	I/O ₈	Z	Data
MDQM[7:0]	O ₁₀	Z	Data Mask
MDECC[7:0]	I/O ₈	Z	Error Correcting Control
$\overline{\text{RAS}}$	O ₁₂	Z	Row Address Strobe

Table 4: Signal Descriptions: All except for PCI pins

Signal	Type	Reset State	Description
CAS	O ₁₂	Z	Column Address Strobe
$\overline{\text{MWE}}$	O ₁₂	Z	Write Enable
$\overline{\text{MCS}}[3:0]$	O ₁₂	Z	Chip Selects
MA[14:0]	O ₁₂	Z	Address
JTAG Interface Signals			
TCK	I		JTAG Clock Input
$\overline{\text{TRST}}$	I		JTAG reset
TDI	I		JTAG Data In
TMS	I		JTAG Mode Select
TDO	O ₄	Z	JTAG Data Out
Serial EEPROM Interface Signals			
SCL	O ₄	X	EEPROM Clock
SDA	I/O ₄	X	EEPROM Data
Configuration Signal			
PCIMODE	I		PCIMODE: tie high for 64-bit PCI bus, tie low for two 32-bit PCI buses
CFN	I		Central Function: indicates whether HPC is the PCIA arbiter and whether it drives REQ64 during reset in 64-bit mode
RDIR	I		Reset Direction: tie low to drive $\overline{\text{PRST}}$ out and $\overline{\text{LRST}}$ in; tie high to drive $\overline{\text{LRST}}$ out and $\overline{\text{PRST}}$ in.
Power and Ground Signals			
V _{CC}	—		Power leads for external connection to a 3.3 V power board plane.
V ₂₅	—		Power leads for external connection to a 2.5 V power board plane.
GND	—		Ground leads for external connection to a ground board plane.

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Table 5: Signal Descriptions: PCI pins in 64-bit mode

Signal	Type	Reset State	Description
PCI Bus Interface Signals			
ADA[31:0]	PCI I/O	Z	Lower Address and Data multiplexed on the same pins.
CBENA[3:0]	PCI I/O	Z	Lower Bus Command and Byte Enables multiplexed on the same pins.
PARA	PCI I/O	Z	Lower Parity represents even parity across ADA[31:0] and CBENA[3:0].
FRAME \bar{A}	PCI I/O	Z	Cycle Frame indicates the beginning and burst length of an access.
IRDY \bar{A}	PCI I/O	Z	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction.
TRDY \bar{A}	PCI I/O	Z	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction.
STOP \bar{A}	PCI I/O	Z	Stop indicates that the current target is requesting the master to stop the current transaction (retry or disconnect).
DEVSELA	PCI I/O	Z	Device Select , when actively driven by a target, indicates the driving device has decoded its address as the target of the current access. As an input to the initiator, it indicates whether any device on the bus has been selected.
IDSELA	PCI I		Initialization Device Select is used as a chip select during configuration read and write transactions. It must be driven high in order to access the chip's internal configuration space.
REQ \bar{A}	PCI I/O	Z	Request indicates to the arbiter that this agent requests use of the bus.
GNT \bar{A}	PCI I/O		Grant indicates to the agent that access to the bus has been granted.
PCLKA	PCI I		PCI Clock provides timing for all transactions on the PCI bus.
PRST \bar{A}	PCI I/O	Z/L	PCI Reset acts as an input when RDIR is high, an output when RDIR is low. As an input it is asserted low to bring all internal HPC operation to a reset state.
PERR \bar{A}	PCI I/O	Z	Parity Error is used to report data parity errors during all PCI transactions except a Special Cycle.
SERR \bar{A}	PCI I/O _D	Z	System Error is used to report address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic.
PME \bar{A}	PCI I/O _D	Z	Power Management Event signals request for change in PM state.
INT[A:D]	PCI I/OD	Z	Interrupt is used to receive or generate level-sensitive interrupt requests.
PCI 64-bit Extension Signals			
ADB[31:0]	PCI I/O	Z	Upper 32-bit Data/Address

Table 5: Signal Descriptions: PCI pins in 64-bit mode

Signal	Type	Reset State	Description
CBENB[3:0]	PCI I/O	Z	Upper 4-bit Byte Enables
PARB	PCI I/O	Z	Upper Parity represents even parity for ADB[31:0] and CBENB[3:0].
FRAMEB	PCI I/O	Z	Request 64-bit Transfer
DEVSELB	PCI I/O	Z	Acknowledge 64-bit Transfer
STOPB	PCI I/O	Z	64EN as defined in the CompactPCI Hot Swap Specification.

Table 6: Signal Descriptions: PCI Pins in 32-bit Split Bus Mode

Signal	Type	Reset State	Description
PCIA Bus Interface Signals			
ADA[31:0]	PCI I/O	Z	Address and Data multiplexed on the same pins.
CBENA[3:0]	PCI I/O	Z	Bus Command and Byte Enables multiplexed on the same pins.
PARA	PCI I/O	Z	Parity represents even parity across ADA[31:0] and CBENA[3:0].
FRAMEA	PCI I/O	Z	Cycle Frame indicates the beginning and burst length of an access.
IRDYA	PCI I/O	Z	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction.
TRDYA	PCI I/O	Z	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction.
STOPA	PCI I/O	Z	Stop indicates that the current target is requesting the master to stop the current transaction (retry or disconnect).
DEVSELA	PCI I/O	Z	Device Select , when actively driven by a target, indicates the driving device has decoded its address as the target of the current access. As an input to the initiator, it indicates whether any device on the bus has been selected.
IDSELA	PCI I		Initialization Device Select is used as a chip select during configuration read and write transactions. It must be driven high in order to access the chip's internal configuration space.
REQA	PCI I/O	Z	Request indicates to the arbiter that this agent requests use of the bus.
GNTA	PCI I/O	Z	Grant indicates to the agent that access to the bus has been granted.
PCLKA	PCI I		PCI Clock provides timing for all transactions on the PCI A bus.
PRSTA	PCI I/O	Z/L	PCI Reset acts as an input when RDIR is high, an output when RDIR is low. As an input, it is asserted low to bring all internal HPC operations to a reset state.

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Table 6: Signal Descriptions: PCI Pins in 32-bit Split Bus Mode

Signal	Type	Reset State	Description
$\overline{\text{PERRA}}$	PCI I/O	Z	Parity Error is used to report data parity errors during all PCI transactions except a Special Cycle.
$\overline{\text{SERRA}}$	PCI I/O _D	Z	System Error is used to report address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic.
$\overline{\text{PMEA}}$	PCI I/O _D	Z	Power Management Event signals a request for change in PM state.
$\overline{\text{INT}}[\text{A:D}]$	PCI I/O _D	Z	Interrupt is used to receive or generate level-sensitive interrupt requests. These pins are not dedicated and can be used on either PCI bus (A or B).
PCIB Bus Interface Signals			
ADB[31:0]	PCI I/O	Z	Address and Data multiplexed on the same pins.
CBENB[3:0]	PCI I/O	Z	Bus Command and Byte Enables multiplexed on the same pins.
PARB	PCI I/O	Z	Parity represents even parity across ADB[31:0] and CBENB[3:0].
FRAMEB	PCI I/O	Z	Cycle Frame indicates the beginning and burst length of an access.
$\overline{\text{IRDYB}}$	PCI I/O	Z	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction.
$\overline{\text{TRDYB}}$	PCI I/O	Z	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction.
$\overline{\text{STOPB}}$	PCI I/O	Z	Stop indicates that the current target is requesting the master to stop the current transaction (retry or disconnect).
$\overline{\text{DEVSELB}}$	PCI I/O	Z	Device Select , when actively driven by a target, indicates the driving device has decoded its address as the target of the current access. As an input to the initiator, it indicates whether any device on the bus has been selected.
REQB	PCI I/O	Z	Request indicates to the arbiter that this agent requests the use of the bus.
$\overline{\text{GNTB}}$	PCI I/O		Grant indicates to the agent that access to the bus has been granted.
PCLKB	PCI I		PCI Clock provides timing for all transactions on the PCI B bus.
$\overline{\text{PRSTB}}$	PCI I/O	Z/L	PCI Reset acts as an input when RDIR is high, an output when RDIR is low. As an input, it is asserted low to bring all internal HPC operations to a reset state.
$\overline{\text{PERRB}}$	PCI I/O	Z	Parity Error is used to report data parity errors during all PCI transactions except a Special Cycle.
$\overline{\text{SERRB}}$	PCI I/O _D	Z	System Error is used to report address parity errors, data parity errors on the Special Cycle command, or any other system error that would have catastrophic results.

1.5 Pin Assignments

Figure 1-2 and Table 7 describe the pin assignments for the V340HPC, revision A0.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	SYSDA[16]	SYSDA[50]	SYSDA[24]	SYSDA[59]	SYSDA[68]	SYSDA[27]	SYSDA[21]	SYSDA[19]	SYSDA[48]	SYSDA[64]	SYSDA[23]	V _{CC} OK	IOW	IOC[6]	IOC[8]	IOC[12]	LCLK	VDDAP	MDATA[62]	MDATA[31]	MDATA[58]	MDQM[3]	MDATA[57]	MA[11]	MDATA[24]	MDQM[6]	
B	SYSDA[28]	SYSDA[3]	SYSDA[54]	SYSDA[61]	SYSDA[48]	SYSDA[20]	SYSDA[18]	SYSDA[22]	SYSDA[65]	SYSDA[57]	IOR	IOC[2]	ALE	IOC[8]	IOC[13]	CFNB	VSSAP	VSSAP	MDATA[30]	MDATA[41]	MDATA[27]	MDQM[2]	MDATA[66]	MDQM[7]	MA[10]	MA[4]	
C	SYSDA[30]	TCDCE	SYSDA[0]	SYSDA[1]	SYSDA[31]	SYSDA[29]	SYSDA[5]	SYSDA[52]	SYSDA[19]	SCL	LRST	SDA	IOC[1]	IOC[0]	IOC[4]	IOC[7]	PCIMODE	VBBP	VDDOP	MDATA[63]	MDATA[60]	MDATA[28]	MDATA[26]	GROUND	MDQM[2]	MCS[3]	
D	SYSDA[63]	SYSCMD[4]	SYSDA[2]	SYSDA[3]	SYSCMD[6]	SYSDA[60]	SYSDA[17]	SYSDA[53]	SYSDA[25]	SYSDA[26]	GROUND	WARMRST	COLDRST	IOC[6]	IOC[3]	IOC[11]	IOC[10]	NC	VSSOP	GROUND	MDATA[29]	MDATA[59]	GROUND	MA[9]	MA[8]	MA[7]	
E	SYSDA[32]	SYSCMD[1]	TCTCE	SYSCMD[7]	V _{CC}	V _{CC}	V ₂₅ (2.5 V)	GROUND	V _{CC}	V _{CC}	GROUND	V ₂₅ (2.5 V)	V _{CC}	V _{CC}	V ₂₅ (2.5 V)	GROUND	V _{CC}	V _{CC}	V ₂₅ (2.5 V)	GROUND	V _{CC}	GROUND	MA[6]	MDATA[55]	MDATA[23]	MDATA[54]	
F	SYSDA[34]	TCWORD[1]	SYSCMD[8]	SYSCMD[2]	V _{CC}																	V _{CC}	MDECC[7]	MDATA[22]	MDATA[53]	MDATA[21]	
G	SYSDA[36]	SYSCMD[5]	SYSCMD[3]	TCWORD[0]	V ₂₅ (2.5 V)																	V ₂₅ (2.5 V)	MDATA[18]	MDATA[20]	MDATA[20]	MDECC[3]	
H	SYSCMD[0]	SYSDA[43]	VALIDOUT	RELEASE	GROUND																	GROUND	MDECC[6]	MCS[2]	MDATA[50]	MDATA[51]	
J	SYSDA[14]	VALIDIN	TCMATCH	SYSDA[8]	V _{CC}																	V _{CC}	MCS[5]	MDATA[16]	MDATA[44]	MDECC[2]	
K	SYSDA[12]	SYSDA[38]	PRCK	WRFRDY	V _{CC}																	V _{CC}	MCS[0]	MCS[1]	MDATA[48]	MDATA[17]	
L	SYSDA[10]	SYSDA[47]	SYSDA[38]	SYSDA[4]	V ₂₅ (2.5 V)																		V ₂₅ (2.5 V)	MDATA[16]	WRCS	MDATA[47]	WRITE
M	SYSDA[16]	SYSDA[15]	FRGST	SYSDA[41]	GROUND																		GROUND	MDATA[14]	MDATA[49]	MA[13]	MA[12]
N	ESPFSMP	SYSDA[45]	SYSDA[11]	SYSDA[13]	V _{CC}																		V _{CC}	MDATA[46]	MDATA[12]	MDATA[13]	
P	RDR	SYSDA[30]	SYSDA[40]	SYSDA[27]	V _{CC}																		V _{CC}	MDATA[15]	MDATA[16]	MDATA[11]	MDATA[44]
R	SYSDA[9]	INTB	SYSDA[44]	SYSDA[42]	V ₂₅ (2.5 V)																		V ₂₅ (2.5 V)	MDATA[9]	MDATA[42]	MDATA[40]	MDATA[8]
T	SYSDA[37]	INTD	SYSDA[9]	INTC	GROUND																		GROUND	MA[1]	MDATA[41]	MA[2]	MA[4]
U	REQM	FMEA	GNTR	INTA	V _{CC}																		V _{CC}	MA[9]	MA[5]	MA[0]	MDQM[5]
V	ADA[30]	ADA[29]	ADA[28]	PRESTA	V _{CC}																		V _{CC}	MDQM[4]	MDQM[0]	MDATA[32]	MDQM[1]
W	ADA[25]	VOA[0]	ADA[4]	ADA[31]	V ₂₅ (2.5 V)																		V ₂₅ (2.5 V)	MDATA[38]	MDATA[6]	MDATA[37]	MDATA[7]
Y	IDSELA	ADA[23]	ADA[27]	ADA[26]	GROUND																		GROUND	MDECC[0]	MDATA[5]	MDATA[36]	MDECC[1]
AA	CBENA[3]	ADA[22]	ADA[21]	ADA[20]	V _{CC}																		V _{CC}	MDATA[4]	MDATA[56]	MDATA[3]	MDECC[4]
AB	FRAMEA	ADA[19]	ADA[18]	ADA[17]	GROUND	V _{CC}	GROUND	V ₂₅ (2.5 V)	V _{CC}	V _{CC}	GROUND	V ₂₅ (2.5 V)	V _{CC}	V _{CC}	V ₂₅ (2.5 V)	GROUND	V _{CC}	V _{CC}	V ₂₅ (2.5 V)	GROUND	V _{CC}	V _{CC}	MDATA[2]	MDATA[3]	MDATA[32]	MDATA[0]	
AC	STOPA	DEVSELA	CBENA[2]	GROUND	GROUND	VIDA[2]	GROUND	ADA[5]	ADA[3]	GROUND	GROUND	REG3	ADB[30]	GROUND	TROYE	GROUND	ADB[23]	GROUND	ADB[18]	ADB[14]	GROUND	ADB[7]	TDI	MDATA[24]	MDATA[1]	MDECC[5]	
AD	TRDA	VOA[1]	GROUND	ADA[11]	ADA[14]	ADA[10]	VSSAO	ADA[4]	ADA[2]	GNTR	CBENB[2]	ADB[26]	TRDYE	DEVSELE	STOPB	ADB[26]	PARB	ADB[21]	ADB[17]	ADB[13]	ADB[10]	VIDB[2]	ADB[4]	GROUND	TDO	TMS	
AE	ADA[16]	PARA	CBENA[0]	TRDYA	ADA[13]	ADA[9]	VBR0	ADA[7]	ADA[1]	PCLKA	CBENB[1]	ADB[31]	FRAMEB	PERRB	ADB[28]	ADB[25]	ADB[22]	ADB[20]	ADB[16]	ADB[12]	ADB[9]	ADB[6]	ADB[3]	ADB[1]	GROUND	TCK	
AF	CBENA[1]	ADA[15]	PERRA	BERRA	ADA[12]	ADA[8]	VDDAG	ADA[6]	ADA[0]	PCLKA	CBENB[0]	VIOB[0]	BERRB	ADB[27]	ADB[24]	VIOB[1]	ADB[19]	ADB[15]	ADB[11]	ADB[8]	ADB[5]	ADB[2]	ADB[0]	FRSTB	TRSTB		

Figure 1-2: V340HPC Pinouts

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Table 7: V340HPC Pin Assignments

PIN #	Signal	PIN #	Signal	PIN #	Signal	PIN #	Signal	PIN #	Signal	PIN #	Signal
A1	SYSAD[16]	C3	SYSAD[0]	E5	V _{CC}	J3	TCMATCH	N5	V _{CC}	T16	GROUND
A2	SYSAD[50]	C4	SYSAD[1]	E6	V _{CC}	J4	SYSAD[6]	N11	GROUND	T22	GROUND
A3	SYSAD[24]	C5	SYSAD[31]	E7	V ₂₅ (2.5 V)	J5	V _{CC}	N12	GROUND	T23	MA[1]
A4	SYSAD[59]	C6	SYSAD[29]	E8	GROUND	J22	V _{CC}	N13	GROUND	T24	MDATA[41]
A5	SYSAD[58]	C7	SYSAD[51]	E9	V _{CC}	J23	MCAS	N14	GROUND	T25	MA[2]
A6	SYSAD[27]	C8	SYSAD[52]	E10	V _{CC}	J24	MDATA[19]	N15	GROUND	T26	MA[4]
A7	SYSAD[21]	C9	SYSAD[19]	E11	GROUND	J25	MDATA[49]	N16	GROUND	U1	REQA
A8	SYSAD[5]	C10	SCL	E12	V ₂₅ (2.5 V)	J26	MDECC[2]	N22	V _{CC}	U2	PMEA
A9	SYSAD[49]	C11	LRST	E13	V _{CC}	K1	SYSAD[12]	N23	MDATA[46]	U3	GNTA
A10	SYSAD[56]	C12	SDA	E14	V _{CC}	K2	SYSAD[38]	N24	MDATA[12]	U4	INTA
A11	SYSAD[23]	C13	IOC[1]	E15	V ₂₅ (2.5 V)	K3	PACK	N25	MDATA[43]	U5	V _{CC}
A12	V _{CC} OK	C14	IOC[0]	E16	GROUND	K4	WRRDY	N26	MDATA[13]	U22	V _{CC}
A13	IOW	C15	IOC[4]	E17	V _{CC}	K5	V _{CC}	P1	RDIR	U23	MA[5]
A14	IOC[5]	C16	IOC[7]	E18	V _{CC}	K22	V _{CC}	P2	SYSAD[39]	U24	MA[3]
A15	IOC[8]	C17	PCIMODE	E19	V ₂₅ (2.5 V)	K23	MCS[0]	P3	SYSAD[40]	U25	MA[0]
A16	IOC[12]	C18	VBPP	E20	GROUND	K24	MCS[1]	P4	SYSAD[7]	U26	MDQM[5]
A17	LCLK	C19	VDDDP	E21	V _{CC}	K25	MDATA[48]	P5	V _{CC}	V1	ADA[30]
A18	VDDAP	C20	MDATA[63]	E22	GROUND	K26	MDATA[17]	P11	GROUND	V2	ADA[29]
A19	MDATA[62]	C21	MDATA[60]	E23	MA[6]	L1	SYSAD[10]	P12	GROUND	V3	ADA[28]
A20	MDATA[31]	C22	MDATA[28]	E24	MDATA[55]	L2	SYSAD[47]	P13	GROUND	V4	PRSTA
A21	MDATA[58]	C23	MDATA[26]	E25	MDATA[23]	L3	SYSAD[36]	P14	GROUND	V5	V _{CC}
A22	MDQM[3]	C24	GROUND	E26	MDATA[54]	L4	SYSAD[4]	P15	GROUND	V22	V _{CC}
A23	MDATA[57]	C25	MDQM[2]	F1	SYSAD[34]	L5	V ₂₅ (2.5 V)	P16	GROUND	V23	MDQM[4]
A24	MA[11]	C26	MCS[3]	F2	TCWORD[1]	L11	GROUND	P22	V _{CC}	V24	MDQM[0]
A25	MDATA[24]	D1	SYSAD[63]	F3	SYSCMD[8]	L12	GROUND	P23	MDATA[10]	V25	MDATA[39]
A26	MDQM[6]	D2	SYSCMD[4]	F4	SYSCMD[2]	L13	GROUND	P24	MDATA[15]	V26	MDQM[1]
B1	SYSAD[28]	D3	SYSAD[2]	F5	V _{CC}	L14	GROUND	P25	MDATA[11]	W1	ADA[25]
B2	SYSAD[3]	D4	SYSAD[33]	F22	V _{CC}	L15	GROUND	P26	MDATA[44]	W2	VIOA[0]
B3	SYSAD[54]	D5	SYSCMD[6]	F23	MDECC[7]	L16	GROUND	R1	SYSAD[8]	W3	ADA[24]
B4	SYSAD[62]	D6	SYSAD[60]	F24	MDATA[22]	L22	V ₂₅ (2.5 V)	R2	INTB	W4	ADA[31]
B5	SYSAD[61]	D7	SYSAD[17]	F25	MDATA[53]	L23	MDATA[16]	R3	SYSAD[44]	W5	V ₂₅ (2.5 V)
B6	SYSAD[48]	D8	SYSAD[53]	F26	MDATA[21]	L24	MRA5	R4	SYSAD[42]	W22	V ₂₅ (2.5 V)
B7	SYSAD[20]	D9	SYSAD[25]	G1	SYSAD[35]	L25	MDATA[47]	R5	V ₂₅ (2.5 V)	W23	MDATA[38]
B8	SYSAD[18]	D10	SYSAD[26]	G2	SYSCMD[5]	L26	MWE	R11	GROUND	W24	MDATA[6]
B9	SYSAD[22]	D11	GROUND	G3	SYSCMD[3]	M1	SYSAD[46]	R12	GROUND	W25	MDATA[37]
B10	SYSAD[55]	D12	WARMRST	G4	TCWORD[0]	M2	SYSAD[15]	R13	GROUND	W26	MDATA[7]
B11	SYSAD[57]	D13	COLDRST	G5	V ₂₅ (2.5 V)	M3	PRQST	R14	GROUND	Y1	IDSELA
B12	IOR	D14	IOC[6]	G22	V ₂₅ (2.5 V)	M4	SYSAD[41]	R15	GROUND	Y2	ADA[23]
B13	IOC[2]	D15	IOC[3]	G23	MDATA[18]	M5	GROUND	R16	GROUND	Y3	ADA[27]
B14	ALE	D16	IOC[11]	G24	MDATA[52]	M11	GROUND	R22	V ₂₅ (2.5 V)	Y4	ADA[26]
B15	IOC[9]	D17	IOC[10]	G25	MDATA[20]	M12	GROUND	R23	MDATA[9]	Y5	GROUND
B16	IOC[13]	D18	N/C	G26	MDECC[3]	M13	GROUND	R24	MDATA[42]	Y22	GROUND
B17	CFNB	D19	VSSDP	H1	SYSCMD[0]	M14	GROUND	R25	MDATA[40]	Y23	MDECC[0]
B18	VSSAP	D20	GROUND	H2	SYSAD[43]	M15	GROUND	R26	MDATA[8]	Y24	MDATA[5]
B19	MDATA[30]	D21	MDATA[29]	H3	VALIDOUT	M16	GROUND	T1	SYSAD[37]	Y25	MDATA[36]
B20	MDATA[61]	D22	MDATA[59]	H4	RELEASE	M22	GROUND	T2	INTD	Y26	MDECC[1]
B21	MDATA[27]	D23	GROUND	H5	GROUND	M23	MDATA[14]	T3	SYSAD[9]	AA1	CBENA[3]
B22	MDATA[25]	D24	MA[9]	H22	GROUND	M24	MDATA[45]	T4	INTC	AA2	ADA[22]
B23	MDATA[56]	D25	MA[8]	H23	MDECC[6]	M25	MA[13]	T5	GROUND	AA3	ADA[21]
B24	MDQM[7]	D26	MA[7]	H24	MCS[2]	M26	MA[12]	T11	GROUND	AA4	ADA[20]
B25	MA[10]	E1	SYSAD[32]	H25	MDATA[50]	N1	RSPSWAP	T12	GROUND	AA5	V _{CC}
B26	MA[14]	E2	SYSCMD[1]	H26	MDATA[51]	N2	SYSAD[45]	T13	GROUND	AA22	V _{CC}
C1	SYSAD[30]	E3	TCTCE	J1	SYSAD[14]	N3	SYSAD[11]	T14	GROUND	AA23	MDATA[4]
C2	TCDOE	E4	SYSCMD[7]	J2	VALIDIN	N4	SYSAD[13]	T15	GROUND	AA24	MDATA[35]

Table 7: V340HPC Pin Assignments

PIN #	Signal	PIN #	Signal	PIN #	Signal	PIN #	Signal	PIN #	Signal	PIN #	Signal
AA25	MDATA[3]	AB21	V _{CC}	AC17	ADB[23]	AD13	TRDYB	AE9	ADA[1]	AF5	ADA[12]
AA26	MDECC[4]	AB22	V _{CC}	AC18	GROUND	AD14	DEVSELB	AE10	PCLKB	AF6	ADA[8]
AB1	FRAMEA	AB23	MDATA[2]	AC19	ADB[18]	AD15	STOPB	AE11	CBENB[3]	AF7	VDDAO
AB2	ADA[19]	AB24	MDATA[33]	AC20	ADB[14]	AD16	ADB[26]	AE12	ADB[31]	AF8	ADA[6]
AB3	ADA[18]	AB25	MDATA[32]	AC21	GROUND	AD17	PARB	AE13	FRAMEB	AF9	ADA[0]
AB4	ADA[17]	AB26	MDATA[0]	AC22	ADB[7]	AD18	ADB[21]	AE14	PERRB	AF10	PCLKA
AB5	GROUND	AC1	STOPA	AC23	TDI	AD19	ADB[17]	AE15	ADB[28]	AF11	CBENB[1]
AB6	V _{CC}	AC2	DEVSELA	AC24	MDATA[34]	AD20	ADB[13]	AE16	ADB[25]	AF12	CBENB[0]
AB7	GROUND	AC3	CBENA[2]	AC25	MDATA[1]	AD21	ADB[10]	AE17	ADB[22]	AF13	VIOB[0]
AB8	V ₂₅ (2.5 V)	AC4	GROUND	AC26	MDECC[5]	AD22	VIOB[2]	AE18	ADB[20]	AF14	SERRB
AB9	V _{CC}	AC5	GROUND	AD1	TRDYA	AD23	ADB[4]	AE19	ADB[16]	AF15	ADB[27]
AB10	V _{CC}	AC6	VIOA[2]	AD2	VIOA[1]	AD24	GROUND	AE20	ADB[12]	AF16	ADB[24]
AB11	GROUND	AC7	GROUND	AD3	GROUND	AD25	TDO	AE21	ADB[9]	AF17	VIOB[1]
AB12	V ₂₅ (2.5 V)	AC8	ADA[5]	AD4	ADA[11]	AD26	TMS	AE22	ADB[6]	AF18	ADB[19]
AB13	V _{CC}	AC9	ADA[3]	AD5	ADA[14]	AE1	ADA[16]	AE23	ADB[3]	AF19	ADB[15]
AB14	V _{CC}	AC10	GROUND	AD6	ADA[10]	AE2	PARA	AE24	ADB[1]	AF20	ADB[11]
AB15	V ₂₅ (2.5 V)	AC11	GROUND	AD7	VSSAO	AE3	CBENA[0]	AE25	GROUND	AF21	ADB[8]
AB16	GROUND	AC12	REQB	AD8	ADA[4]	AE4	TRDYA	AE26	TCK	AF22	ADB[5]
AB17	V _{CC}	AC13	ADB[30]	AD9	ADA[2]	AE5	ADA[13]	AF1	CBENA[1]	AF23	ADB[2]
AB18	V _{CC}	AC14	GROUND	AD10	GNTB	AE6	ADA[9]	AF2	ADA[15]	AF24	ADB[0]
AB19	V ₂₅ (2.5 V)	AC15	TRDYB	AD11	CBENB[2]	AE7	VBBO	AF3	PERRA	AF25	PRSTB
AB20	GROUND	AC16	GROUND	AD12	ADB[29]	AE8	ADA[7]	AF4	SERRA	AF26	TRSTB

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1.6 DC Specifications

The DC specifications for the PCI bus signals reference those given in the *PCI Local Bus Specification*, Revision 2.2, Section 4.2. For more information on the PCI DC specifications, see the *PCI Local Bus Specification*.

Table 8: Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage	3.6	V
V_{IN}	DC input voltage	-0.3 to 5.75	V
T_{STG}	Storage temperature range	-65 to 150	°C

Table 9: Guaranteed Operating Conditions

Symbol	Parameter	Value	Units	
V_{CC}	Supply voltage 3.3 volt	3.0 to 3.6	V	
V_{25}	Supply voltage 2.5 volt	V340HPC-75BPA0	2.3 to 2.7	V
		V340HPC-83BPA0		
		V340HPC-100BPA0	2.4 to 2.6	
J_{max}	Maximum Junction temperature	125	°C	
θ_{JA}	Junction-to-ambient thermal resistance	17.2	°C/w	
θ_{JC}	Junction-to-case thermal resistance	11	°C/w	
T_A	Ambient temperature range	0 to 70	°C	

1.6.1 Local Bus DC Specifications

Table 10: Local Bus Signals DC Operating Specifications

Symbol	Description	Conditions	Min	Max	Units
V_{IL}	Low level input voltage			1.0	V
V_{IH}	High level input voltage		2.1		V
I_{IL}	Low level input current	$V_{IN} = GND$	-10		μA
I_{IH}	High level input current	$V_{IN} = V_{CC}$		10	μA
V_{OL}	Low level output voltage			0.4	V
V_{OH}	High level output voltage		2.4		V
I_{OZ}	Tristate output leakage current	$V_{IN} = GND$	-10	10	μA
I_{OS}	Output short circuit current	$V_{CC} = 3.6 V$	-55	55	mA
C_{IO}	Input and output capacitance			4	pF

1.6.2 PCI Bus DC Specifications

Table 11: PCI Bus Signals DC Operating Specifications

Symbol	Parameter	3.3 V Signaling			5 V Signaling			Units
		Condition	Min	Max	Condition	Min	Max	
V_{CC}	Supply Voltage		3.0	3.6		3.0	3.6	V
V_{IH}	Input high voltage ^a		$0.5 V_{CC}$	4.1		1.9	5.75	V
V_{IL}	Input low voltage		-0.5	$0.33 V_{CC}$		-0.5	0.9	V
I_{IL}	Input leakage current ^b	$0 < V_{IN} < V_{CC}$	-10	10	$0 < V_{IN} < V_{CC}$	-70	70	μ A
V_{OH}	Output high voltage	$I_{OUT} = -500 \mu$ A	$0.9 V_{CC}$		$I_{OUT} = -2$ mA	2.4		V
V_{OL}	Output low voltage	$I_{OUT} = 1500 \mu$ A		$0.1 V_{CC}$	$I_{OUT} = 6$ mA		0.55	V
C_{IN}	Input pin capacitance ^c			10			10	pF
C_{CLK}	PCLK pin capacitance		5	12		5	12	pF
C_{IDSEL}	IDSEL pin capacitance ^d			8			8	pF

- a. Custom 5 V tolerant PCI buffers are used in the design.
- b. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.
- c. Absolute maximum pin capacitance for a PCI unit is 10 pF (except for CLK).
- d. Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].

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1.7 AC Specifications

The AC specifications for the PCI bus signals match those given in the *PCI Local Bus Specification*, Revision 2.2, Section 4.2. For more information on the PCI AC specifications, including the V/I curves for 3.3 V signalling, see the *PCI Local Bus Specification*.

1.7.1 PCI Bus Timings

Table 12: PCI Bus Signals AC Operating Specifications (33 MHz)

Symbol	Parameter	Condition	Min	Max	Units
$I_{OH(AC)}$	Switching current high	$0 < V_{OUT} \leq 0.3 V_{CC}$	$-12 V_{CC}$		mA
		$0.3 V_{CC} < V_{OUT} < 0.9 V_{CC}$	$-17.1 (V_{CC} - V_{OUT})$		mA
		$0.7 V_{CC} < V_{OUT} < V_{CC}$		Equation C	
	(Test point)	$V_{OUT} = 0.7 V_{CC}$		$-32 V_{CC}$	mA
$I_{OL(AC)}$	Switching current low	$V_{CC} > V_{OUT} \geq 0.6 V_{CC}$	$16 V_{CC}$		mA
		$0.6 V_{CC} > V_{OUT} > 0.1 V_{CC}$	$26.7 V_{OUT}$		mA
		$0.18 V_{CC} > V_{OUT} > 0$		Equation D	
	(Test point)	$V_{OUT} = 0.18 V_{CC}$		$38 V_{CC}$	mA
I_{CL}	Low clamp current	$-3 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1) / 0.015$		mA
I_{CH}	High clamp current	$V_{CC} + 4 > V_{IN} \geq V_{CC} + 1$	$25 + (V_{IN} - V_{CC} - 1) / 0.015$		mA
t_R	Unloaded output rise time	$0.2 V_{CC} - 0.6 V_{CC}$ load	1	4	V/ns
t_F	Unloaded output fall time	$0.6 V_{CC} - 0.2 V_{CC}$ load	1	4	V/ns

Table 13: PCI Bus Signals, AC Operating Specifications (66 MHz)

Symbol	Parameter	Condition	Min	Max	Units
$I_{OH(AC,min)}$	Switching current high, minimum	$V_{OUT} = 0.3 V_{CC}$	$-12 V_{CC}$		mA
$I_{OH(AC,max)}$	Switching current high, maximum	$V_{OUT} = 0.7 V_{CC}$		$-32 V_{CC}$	mA
$I_{OL(AC,min)}$	Switching current low, minimum	$V_{OUT} = 0.6 V_{CC}$	$16 V_{CC}$		mA
$I_{OL(AC,max)}$	Switching current low, maximum	$V_{OUT} = 0.18 V_{CC}$		$38 V_{CC}$	mA
I_{CL}	Low clamp current	$-3 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1) / 0.015$		mA
I_{CH}	High clamp current	$V_{CC} + 4 > V_{IN} \geq V_{CC} + 1$	$25 + (V_{IN} - V_{CC} - 1) / 0.015$		mA
t_R	Output rise slew rate	$0.3 V_{CC}$ to $0.6 V_{CC}$	1	4	V/ns
t_F	Output fall slew rate	$0.6 V_{CC}$ to $0.3 V_{CC}$	1	4	V/ns

1.7.2 Local Bus Timings

Table 14: Local Bus AC Test Conditions

Symbol	Parameter	Limits	Units
V_{CC}	Supply voltage, 3.3 volt operation	3.0 to 3.6	V
V_{25}	Supply voltage 2.5 volt	V340HPC-75BPA0 V340HPC-83BPA0	2.3 to 2.7
		V340HPC-100BPA0	2.4 to 2.6
V_{IN}	Input low and high voltages	0.4 and 2.0	V
C_{OUT}	Capacitive load on output and I/O pins	50	pF

Table 15: Capacitive Derating for Output and I/O Pins

Output Drive Limit	Supply voltage	Derating
4 mA	3.3 volt	+0.30 ns/pF for loads > 50pF
8 mA	3.3 volt	+0.15 ns/pF for loads > 50pF
10 mA	3.3 volt	+0.12 ns/pF for loads > 50pF
12 mA	3.3 volt	+0.10 ns/pF for loads > 50pF

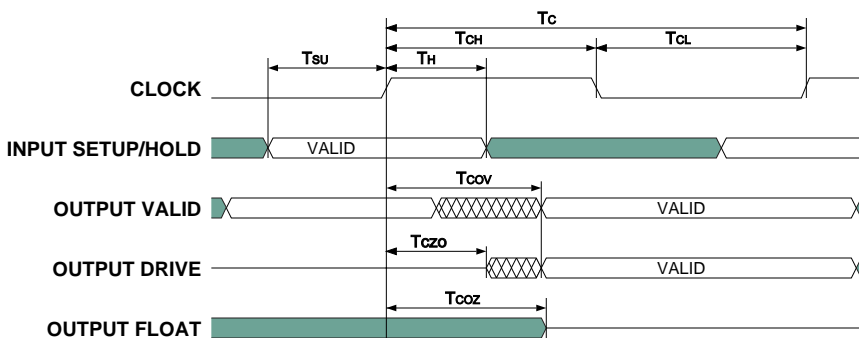


Figure 1-3: Clock and Synchronous Signals

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Table 16: Local Bus Timing Parameters for $V_{CC} = 3.3 \text{ Volts} \pm 10\%$

#	Symbol	Description	Units	V340HPC-100BPA0		V340HPC-83BPA0		V340HPC-75BPA0	
				Min	Max	Min	Max	Min	Max
1	T_C	LCLK period	ns	10		12		13.3	
2	T_{CH}	LCLK high time (measured at 1.5 V)	ns	4		5		6	
3	T_{CL}	LCLK low time (measured at 1.5 V)	ns	4		5		6	
4	T_{SU}	Synchronous input setup	ns	2		2		2	
5	T_H	Synchronous input hold	ns	2		2		2	
6	T_{CZO}	LCLK to output drive delay	ns		4		6		7
7	T_{COV}	LCLK to output valid delay	ns		4		5		6
8	T_{COZ}	LCLK to output float delay	ns	0	2	0	2	0	2
9	T_{RST}	Reset period when \overline{LRST} used as input	ns	$16 T_C$		$16 T_C$		$16 T_C$	

Table 17: PCI Bus Timing Parameters for $V_{CC} = 3.3 \text{ Volts} \pm 10\%$

#	Symbol	Description	Units	V340HPC-100BPA0		V340HPC-83BPA0		V340HPC-75BPA0	
				Min	Max	Min	Max	Min	Max
1	T_C	PCLK period	ns	15		16		17	
2	T_{CH}	PCLK high time (measured at 1.5 V)	ns	6		6		6	
3	T_{CL}	PCLK low time (measured at 1.5 V)	ns	6		6		6	
4	T_{SU}	Synchronous input setup to PCLK	ns	3		3		4	
5	T_H	Synchronous input hold from PCLK	ns	0		0		0	
6	T_{CZO}	PCLK to output to drive delay	ns		7		8		9
7	T_{COV}	PCLK to output valid delay	ns		7		8		9
8	T_{COZ}	PCLK to output float delay	ns		9		11		12
9	T_{RST}	Reset period when \overline{PRSTA} used as input	ns	$16 T_C$		$16 T_C$		$16 T_C$	

1.7.3 Serial EEPROM Port Timings

The clock for the serial EEPROM interface is derived by dividing the local bus clock. The waveforms generated are shown in **Figure 1-4**.

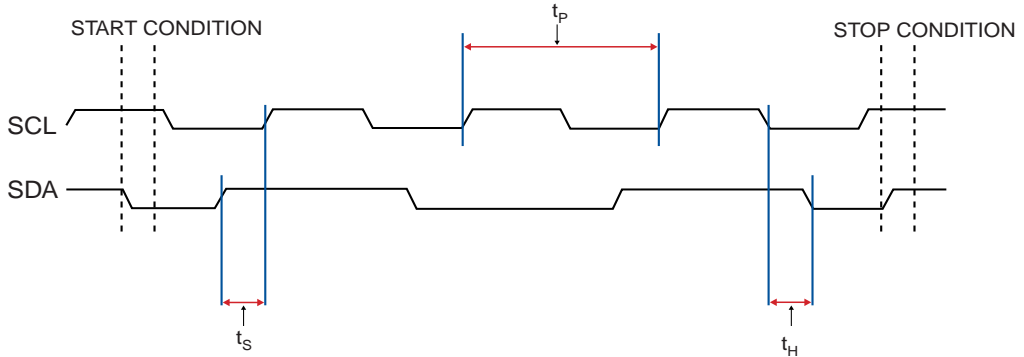


Figure 1-4: Serial EEPROM Waveforms and Timings

Table 18: Serial EEPROM Waveform and Timing Information

Symbol	Description	Min	Max
t_P	Clock Period	192 + 4 local clocks	4064 + 4 local clocks
t_S	Setup Time	48 + 1 local clocks	1016 + 1 local clocks
t_H	Hold Time	48 + 1 local clocks	1016 + 1 local clocks

1.8 Getting Help from V3 Semiconductor

If you need assistance with a technical question, please contact us. E-mail is the quickest and most efficient way to get technical support from V3. The V3 Web site also contains a wealth of technical support information, as well as the most up-to-date technical documents. Visit us on the Web at: <http://www.vcubed.com>.

Corporate Office
250 Consumers Road, Suite 901
Toronto, Ontario, Canada
M2J 4V6
Telephone: 1-877-283-7364
(416) 497-8884
Fax: (416) 497-1160
E-mail: V3help@vcubed.com

Sales Office
2348G Walsh Avenue
Santa Clara, California 95051
USA
Telephone: 1-800-488-8410
(408) 988-1050
Fax: (408) 988-2601

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