IS31FL3726

16-CHANNEL COLOR LED DRIVER

June 2018

GENERAL DESCRIPTION

The IS31FL3726 is comprised of constant-current drivers designed for color LEDs. The output current value can be set using an external resistor. The output current value can be adjusted from 5mA to 60mA through the external resistor.

As a result, all outputs will have virtually the same current levels.

This driver incorporates 16-channel constant current outputs, a 16-bit shift register, a 16-bit latch and a 16-bit AND-gate circuit.

These drivers have been designed using the CMOS process.

APPLICATIONAS

- Cellular phones
- MP3/MP4/CD/minidiskplayers
- Toys

FEATURES

- Output current capability and number of outputs: 60mA × 16 outputs
- Constant current range: 5mA to 60mA
- Application output voltage: ≥0.4V
- For anode-common LEDs
- Power supply voltage range, V_{DD} = 3.3V to 5.5V
- Serial and parallel data transfer rate: 20MHz (Max. cascade connection)
- Operating temperature range, T_A= -40°C ~ +85°C
- Package: QFN-24 (4mm×4mm) and eTSSOP-24
- Current accuracy (All output on)

Output voltage	Current Accuracy		Output Current
	Between Bits	Between ICs	
≥0.4V	±4%	±20%	5mA ~ 60mA

TYPICAL APPLICATION CIRCUIT

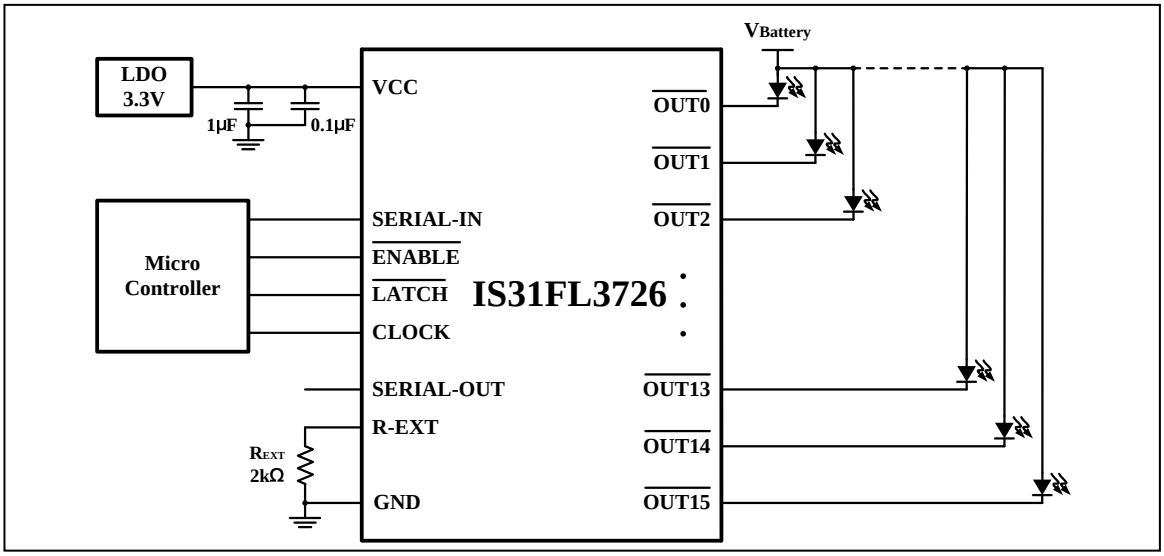


Figure 1 Typical Application Circuit

TYPICAL APPLICATION CIRCUIT (CONTINUE)

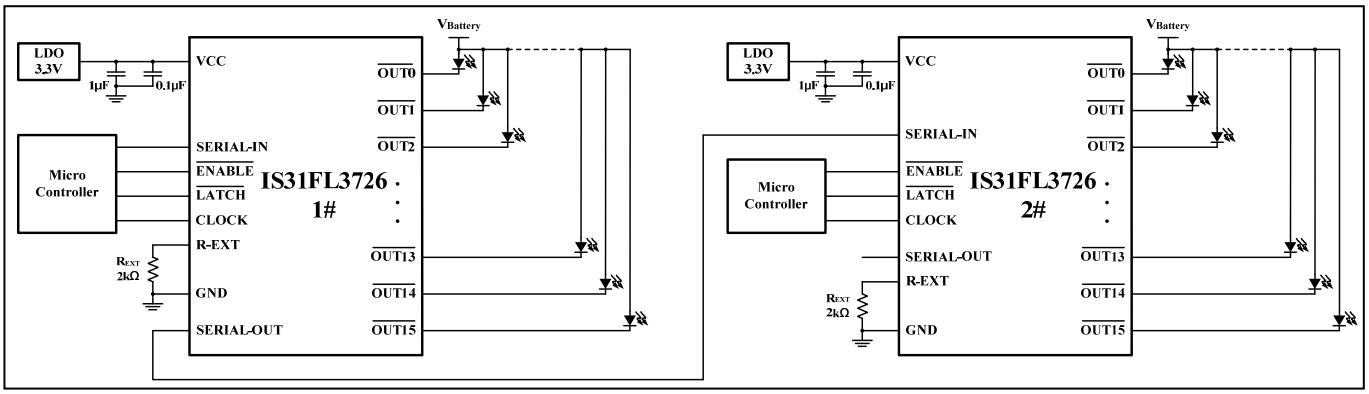
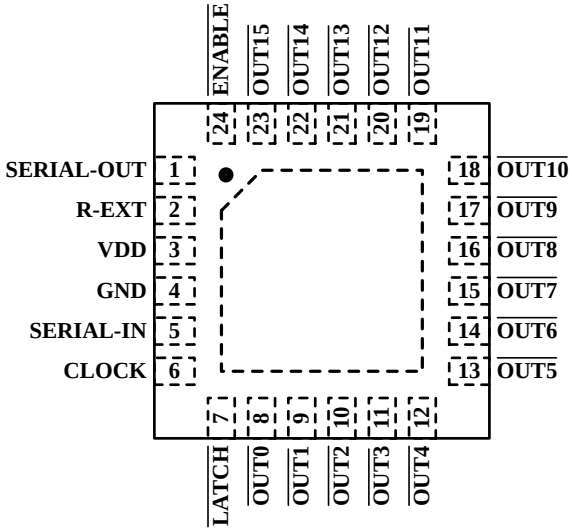
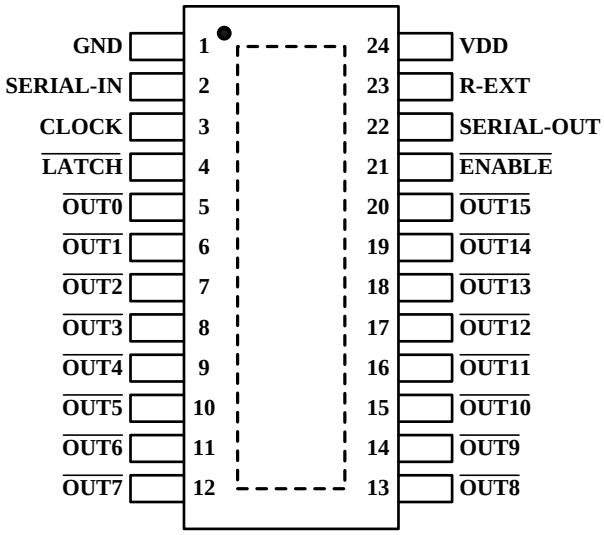


Figure 2 Typical Application Circuit (Synchronization-Work)

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-24	
eTSSOP-24	

PIN DESCRIPTION

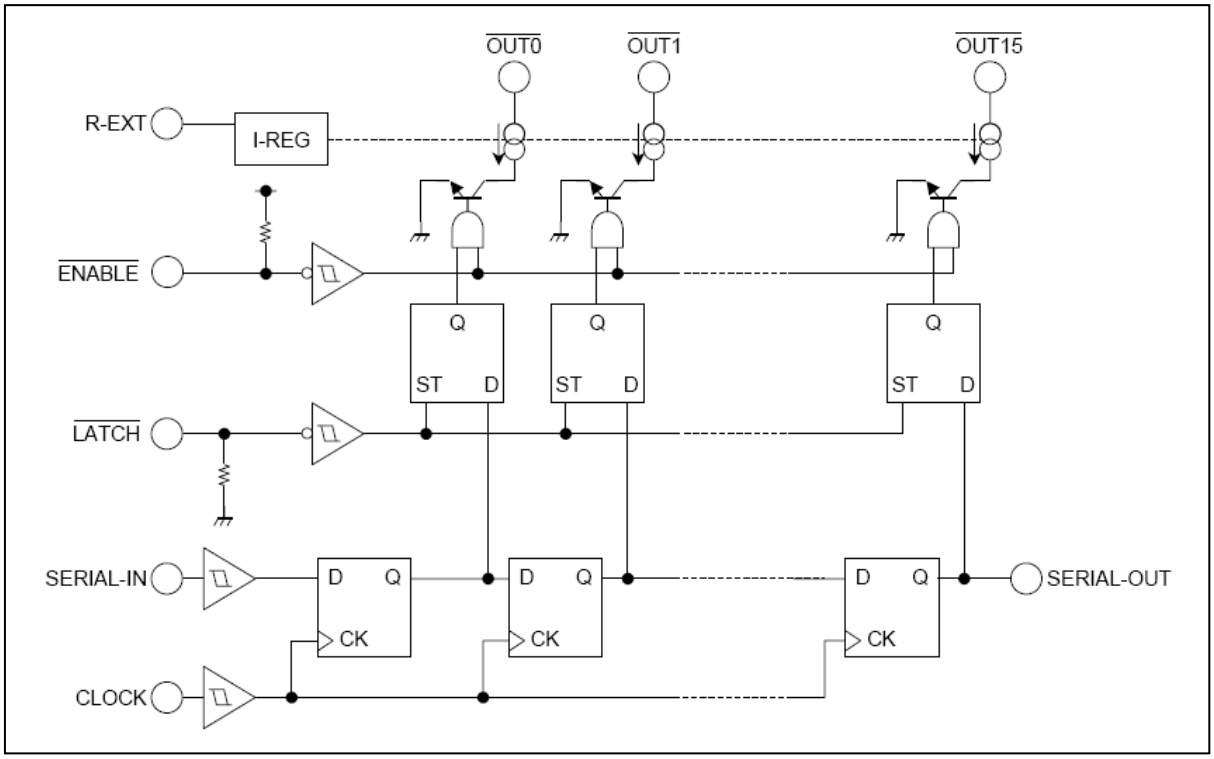
No.		Pin	Description
QFN	eTSSOP		
1	22	SERIAL-OUT	Output terminal for serial data input on SERIAL-IN terminal.
2	23	R-EXT	Input terminal used to connect an external resistor. This regulated the output current.
3	24	VDD	Supply voltage terminal.
4	1	GND	GND terminal for control logic.
5	2	SERIAL-IN	Input terminal for serial data for data shift register.
6	3	CLOCK	Input terminal for clock for data shift on rising edge.
7	4	$\overline{\text{LATCH}}$	Input terminal for data strobe When the $\overline{\text{LATCH}}$ input is driven High, data is not latched. When it is pulled Low ， data is latched.
8 ~ 23	5~20	$\overline{\text{OUT0}}$~$\overline{\text{OUT15}}$	Constant-current output terminals.
24	21	$\overline{\text{ENABLE}}$	Input terminal for output enable. All outputs ($\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$) are turned off, when the $\overline{\text{ENABLE}}$ terminal is driven High .And are turned on, when the terminal is driven Low.
		Thermal Pad	Connect to GND.

ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY
IS31FL3726-QFLS2-TR	QFN-24, Lead-free	2500/Reel
IS31FL3726-ZLS2-TR IS31FL3726-ZLS2	eTSSOP-24, Lead-free	2500/Reel 62/Tube

FUNCTIONAL BLOCK DIAGRAM



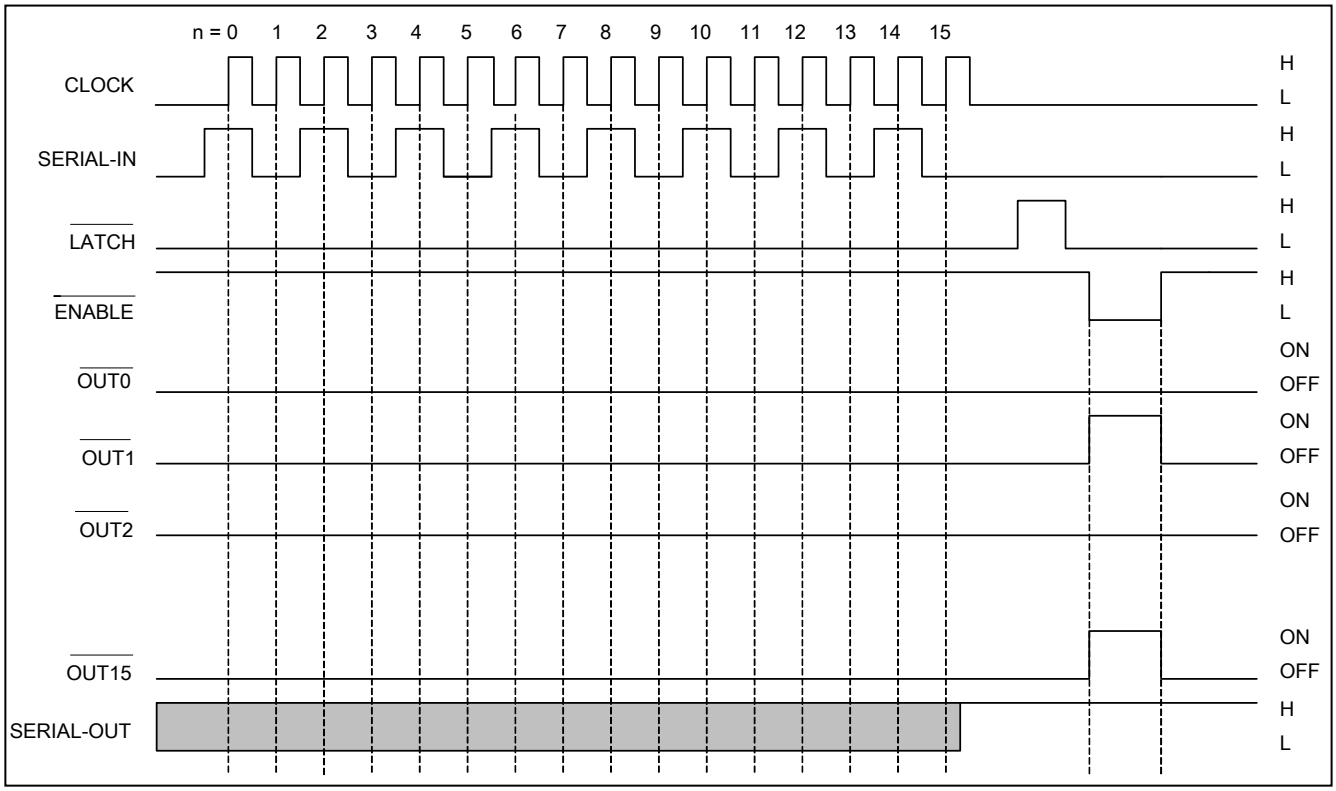


Figure 3 Timing Diagram

Warning: Latch circuit is leveled-latch circuit. Be careful because it is not triggered-latch circuit.

Note 1: The latches circuit holds data by pulling the $\overline{LATCH}$ terminal Low. And, when $\overline{LATCH}$ terminal is a High level, latch circuit doesn't hold data, and it passes from the input to the output. When $\overline{ENABLE}$ terminal is a Low level, output terminal $\overline{OUT0}$ to $\overline{OUT15}$ respond to the data, and on and off does. And, when $\overline{ENABLE}$ terminal is a High level, it offs with the output terminal regardless of the data.

Truth Table

CLOCK	$\overline{LATCH}$	$\overline{ENABLE}$	SERIAL-IN	$\overline{OUT0}$ …$\overline{OUT7}$ … $\overline{OUT15}$	SERIAL-OUT
↑	H	L	Dn	Dn …Dn-7 …Dn-15	Dn-15
↑	L	L	Dn+1	No change	Dn-14
↑	H	L	Dn+2	Dn+2 …Dn-5 …Dn-13	Dn-13
↓	X	L	Dn+3	Dn+2 …Dn-5 …Dn-13	Dn-13
↓	X	H	Dn+3	OFF	Dn-13

Note 2: $\overline{OUT0}$ to $\overline{OUT15}$ =On when Dn = H; $\overline{OUT0}$ to $\overline{OUT15}$ =Off when Dn = L. In order to ensure that the level of the power supply voltage is correct, an external resistor must be connected between R-EXT and GND.

Warning: The following conditions, $\overline{ENABLE}$=0, $\overline{LATCH}$=1, SERIAL-IN=1, cannot be configured at the same time when power on, or IS31FL3726 will be abnormal.

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ V_{DD}+0.2V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A=T_J	-40°C ~ +85°C
Junction Package thermal resistance, junction to ambient (4 layer standard test PCB based on JEDEC standard), θ_{JA}	29.1°C/W (QFN) 77.9°C/W (eTSSOP)
ESD (HBM) ESD (CDM)	±3kV ±1kV

Note 3: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITION

T_A = 25°C, unless otherwise specified.

Symbol	Characteristic	Condition	Min.	Typ.	Max.	Unit
V_{OUT}	Output voltage			0.7	4	V
f_{CLK}	Clock frequency (Note 4)	Cascade connected			20	MHz
t_{wLAT}	$\overline{LATCH}$ pulse width		50			ns
t_{wCLK}	CLOCK pulse width		25			ns
t_{wENA}	$\overline{ENABLE}$ pulse width (Note 4, 5)	Upper, I_{OUT} = 20mA	20			µs
		Lower, I_{OUT} = 20mA	20			
t_{SETUP1}	Set-up time for CLOCK terminal		10			ns
t_{HOLD}	Hold time for CLOCK terminal		10			ns
t_{SETUP2}	Set-up time for $\overline{LATCH}$ terminal		50			ns

Note 4: Guaranteed by design.

Note 5: When the pulse of the Low level is input to the $\overline{ENABLE}$ terminal held in the High level.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = 3.3V ~ 5.5V, unless otherwise specified.

Symbol	Characteristic	Condition		Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	Normal operation		3.3		5.5	V
I_{OUT1}	Output current	V_{OUT} = 0.4V V_{DD} = 3.3V	R_{EXT} = 1kΩ	15	18.7	22	mA
I_{OUT2}		V_{OUT} = 0.4V V_{DD} = 5.5V		15	18.9	22	
ΔI_{OUT1}	Output current error between bits	V_{OUT}≥0.4V, All outputs on	R_{EXT} = 1kΩ		±3	±4	%
I_{OZ}	Output leakage current input voltage	V_{OUT} = 5.0V				1	μA
V_{IH}	Input voltage			1.4			V
V_{IL}						0.4	
V_{OL}	SOUT terminal voltage	I_{OL} = 1.0mA, V_{DD} = 3.3V				0.3	V
		I_{OL} = 1.0mA, V_{DD} = 5V				0.3	
V_{OH}		I_{OH} = -1.0mA, V_{DD} = 3.3V		3			
		I_{OH} = -1.0mA, V_{DD} = 5V		4.7			
%/V_{DD}	Output current supply voltage regulation	When V_{DD} is changed 3.3V to 5.5V			-1		%
$R_{(UP)}$	Pull-up resistor	$\overline{ENABLE}$ terminal		250	500	750	kΩ
$R_{(DOWN)}$	Pull-down resistor	$\overline{LATCH}$ terminal					
$I_{DD(OFF)1}$	Supply current	V_{OUT} = 5V	R_{EXT} = OPEN		1		mA
$I_{DD(OFF)2}$		V_{OUT} = 5V All outputs off	R_{EXT} = 1kΩ		4.5		
$I_{DD(ON)1}$		V_{OUT} = 0.7V All outputs on	R_{EXT} = 1kΩ		5		

SWITCHING CHARACTERISTICS

T_A = 25°C, unless otherwise specified.

Symbol	Characteristic	Condition	Min.	Typ.	Max.	Unit
t_{pLH1}	Propagation delay	CLK-$\overline{OUTn}$, $\overline{LATCH}$ = "H" $\overline{ENABLE}$ = "L"		80	200	ns
t_{pLH2}		$\overline{LATCH}$–$\overline{OUTn}$, $\overline{ENABLE}$ = "L"		80	200	
t_{pLH3}		$\overline{ENABLE}$-$\overline{OUTn}$, $\overline{LATCH}$ = "H"		2000		
t_{pLH}		CLK-SERIAL OUT	3	5		
t_{pHL1}		CLK-$\overline{OUTn}$, $\overline{LATCH}$ = "H" $\overline{ENABLE}$ = "L"		160	250	
t_{pHL2}		$\overline{LATCH}$-$\overline{OUTn}$, $\overline{ENABLE}$ = "L"		160	250	
t_{pHL3}		$\overline{ENABLE}$-$\overline{OUTn}$, $\overline{LATCH}$ = "H"		200	350	
t_{pLH}		CLK-SERIAL OUT	4	6		
t_{or}	Output rise time	10%~90% of voltage waveform	30	150	200	ns
t_{of}	Output fall time	90%~10% of voltage waveform	150	200	250	ns
t_r	Maximum CLOCK rise time	When not on PCB (Note)			5	µs
t_f	Maximum CLOCK fall time				5	µs

Conditions: (Refer to test circuit.)

Topr = 25°C, V_{DD}=V_{IH} =3.3V and 5V, V_{OUT} = 0.7V, V_{IL} =0V, R_{EXT} =1000Ω, V_L =3.0V, R_L=60Ω, C_L=10.5pF

Note 6:

1. If the device is connected in a cascade and tr/tf for the waveform is large, it may not be possible to achieve the timing required for data transfer. Please consider the timings carefully.

2. Delay between outputs. The IS31FL3726 has graduated delay circuits between outputs. The fixed delay time is 5ns (typical), OUT1 has 5ns delay, OUT2 has 10 ns delay, etc. This delay prevents large inrush currents, which reduce power supply bypass capacitor requirements when the outputs turn on. The delay works during switch on and switch off of each output channel. LEDs that have not turned on before $\overline{ENABLE}$ is low will still turn on and off at the determined delayed time regardless of the state of $\overline{ENABLE}$. Therefore, every LED will be illuminated for the amount of time $\overline{ENABLE}$ is pulled high.

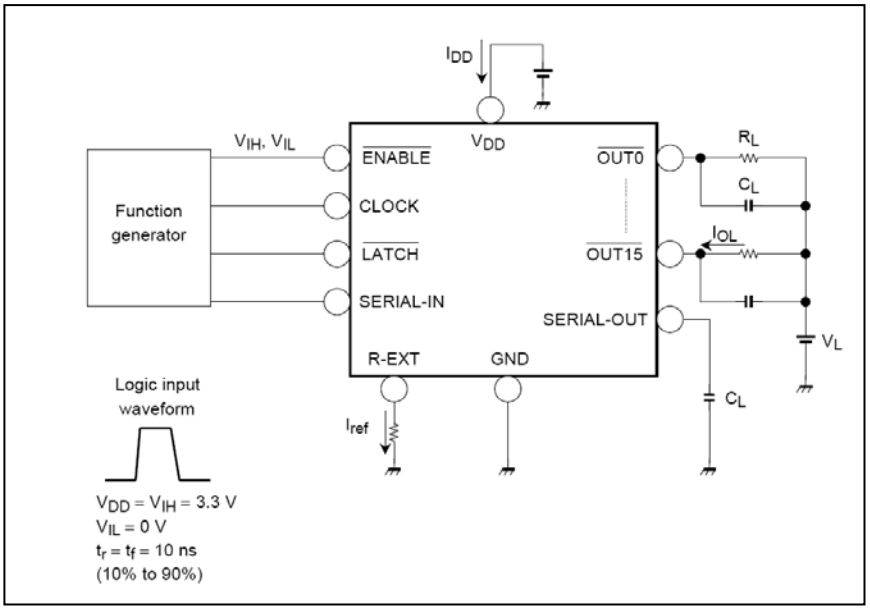
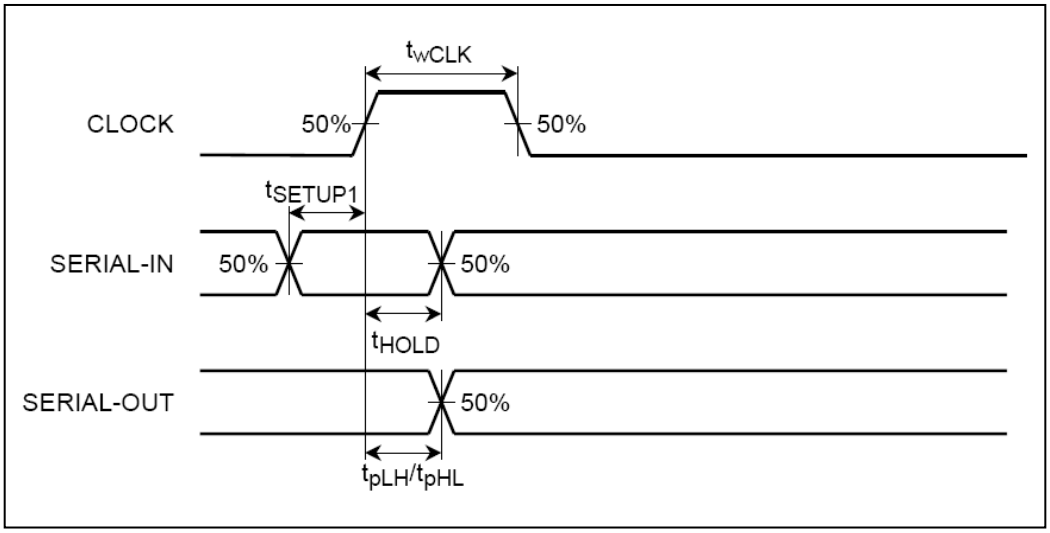


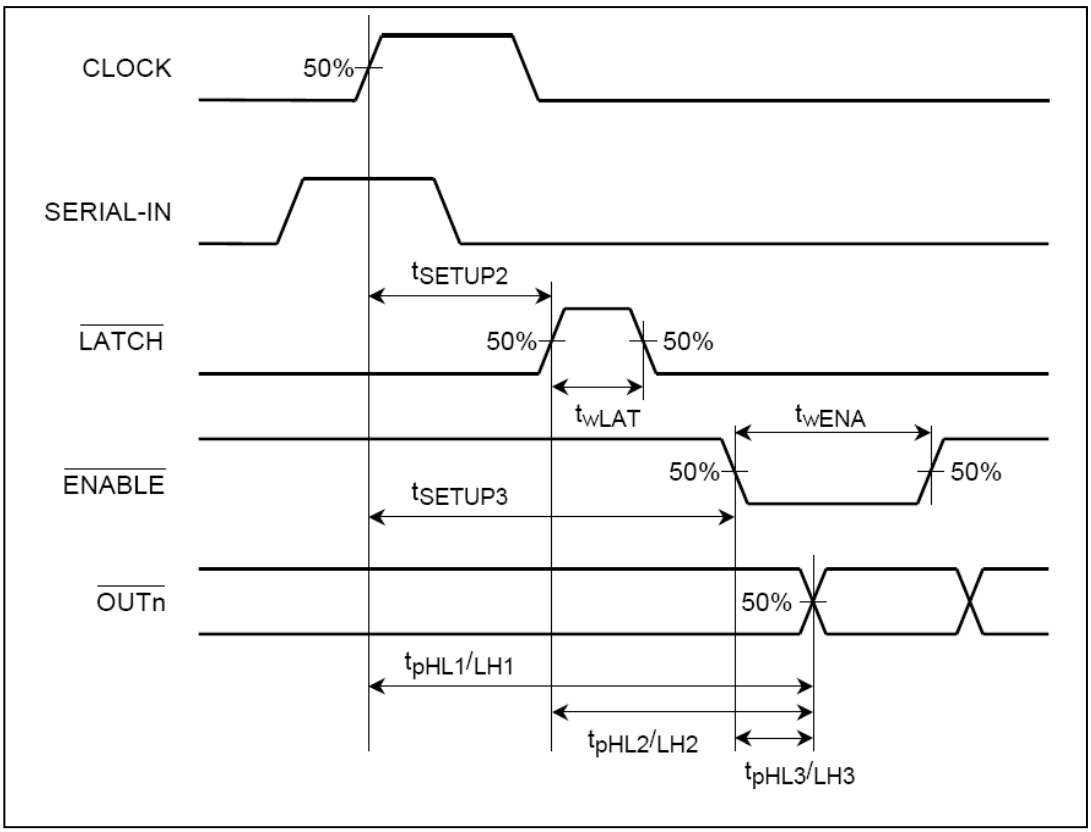
Figure 4 Test Diagram

TIMING WAVEFORM

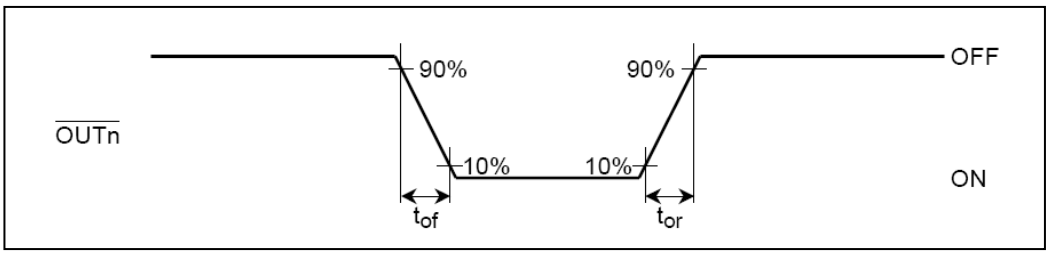
1. CLOCK, SERIAL-IN, SERIAL-OUT



2. CLOCK, SERIAL-IN, $\overline{\text{LATCH}}$, $\overline{\text{ENABLE}}$, $\overline{\text{OUTn}}$



3. $\overline{\text{OUTn}}$



TYPICAL OPERATING CHARACTERISTICS

ADJUSTING OUTPUT CURRENT

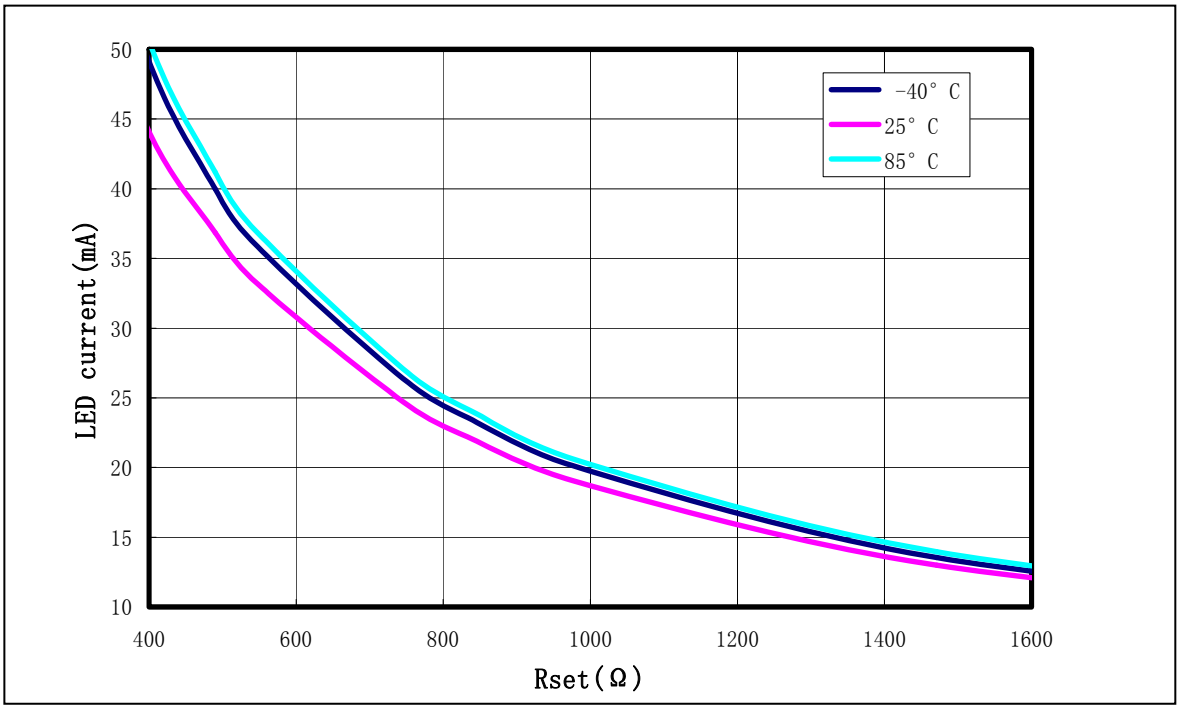
The output current of each channel is set by an external resistor R_{EXT}, the relationship between I_{OUT} and R_{EXT} is:

$$I_{OUT} = (V_{R\text{-}EXT}/R_{EXT})\times 52$$

the $V_{R\text{-}EXT}$ is 0.36V in the IS31FL3726,so we can count the I_{OUT} as :

$$I_{OUT} = 0.36\times 52/R_{EXT}.$$

As show in the figure below:



CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

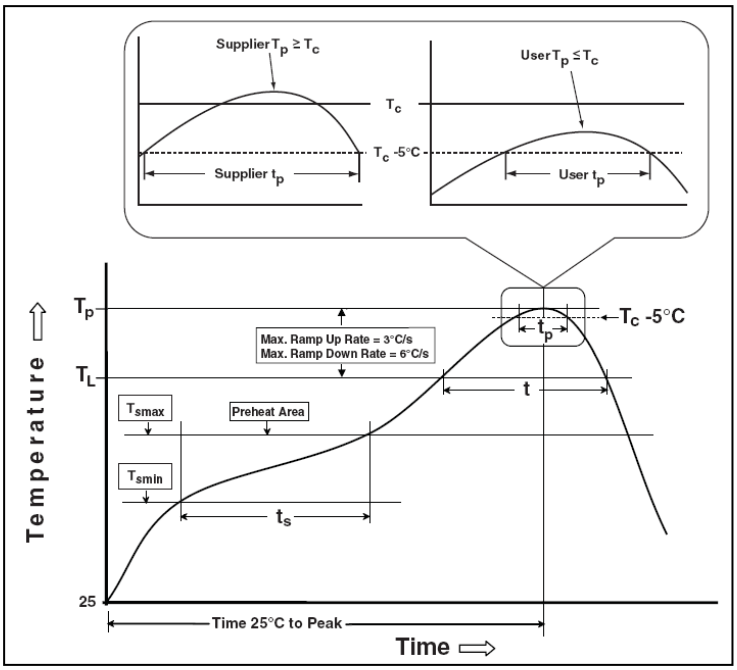
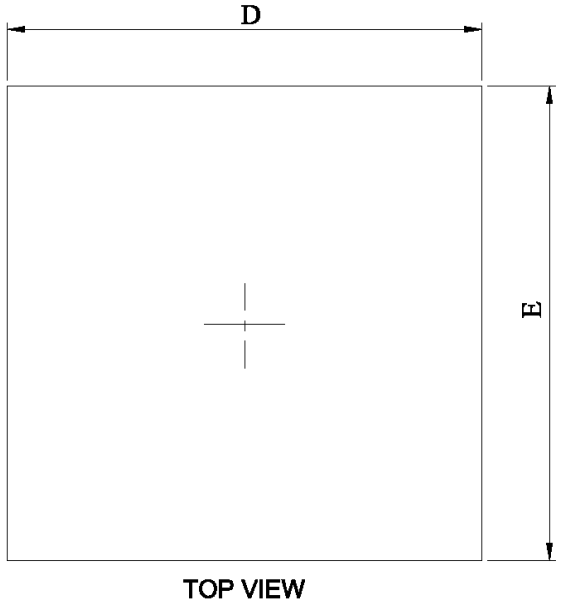


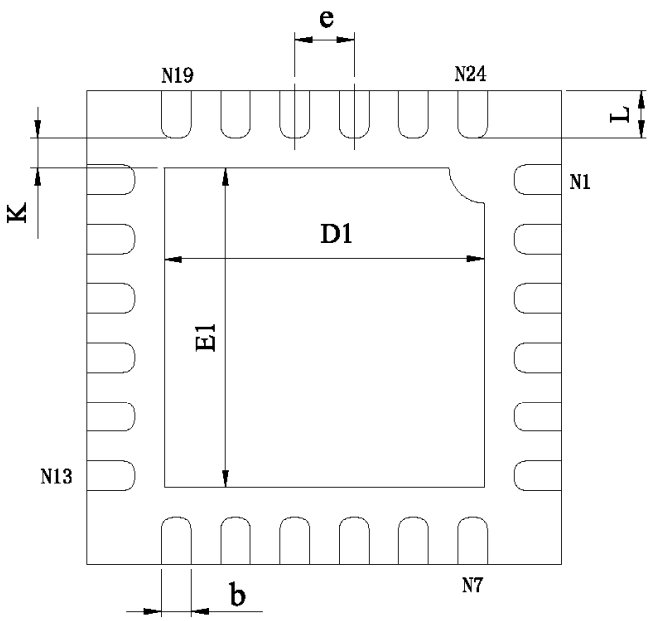
Figure 5 Classification Profile

PACKAGE INFORMATION

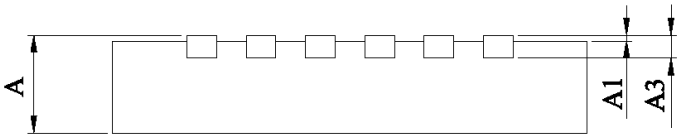
QFN-24



TOP VIEW



BOTTOM VIEW

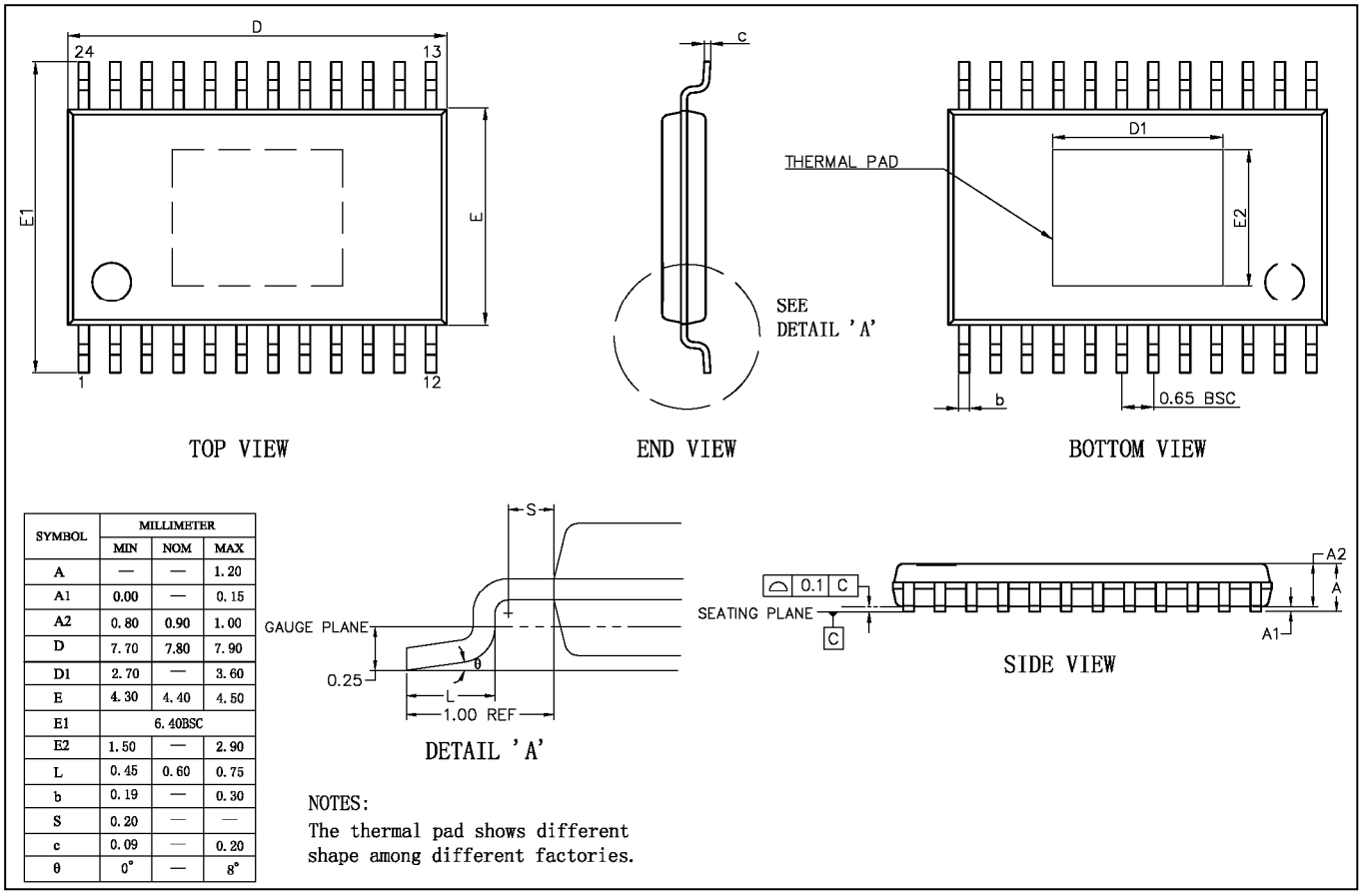


SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.203REF		
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D1	2.30	—	2.80
e	0.50BSC		
E1	2.30	—	2.80
L	0.30	0.40	0.50
b	0.18	0.25	0.30
K	0.20MIN		

NOTES:
The thermal pad shows different shape among different factories.

eTSSOP-24

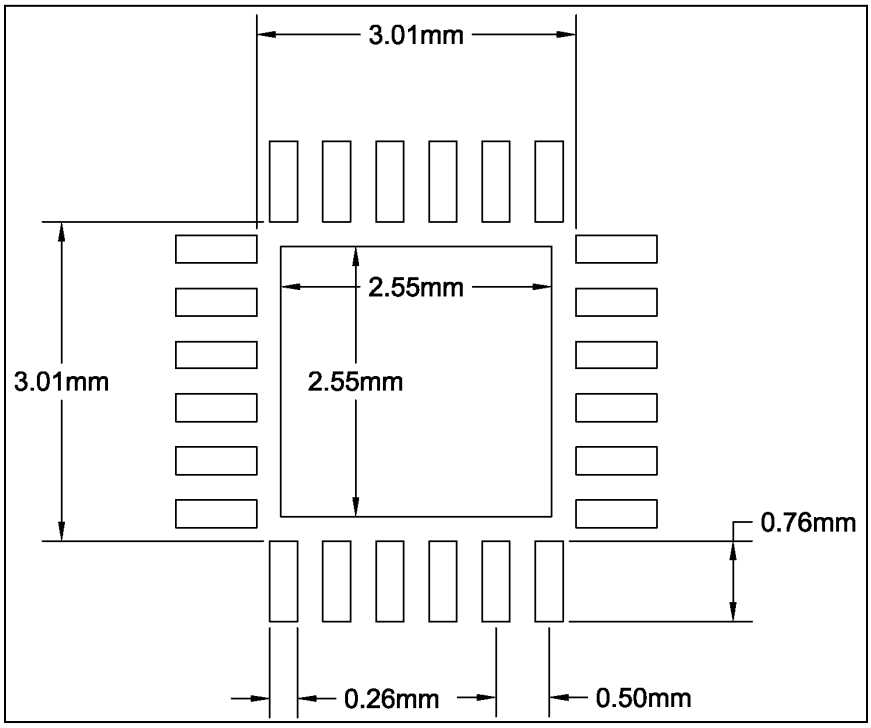


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.00	—	0.15
A2	0.80	0.90	1.00
D	7.70	7.80	7.90
D1	2.70	—	3.60
E	4.30	4.40	4.50
E1	6.40BSC		
E2	1.50	—	2.90
L	0.45	0.60	0.75
b	0.19	—	0.30
S	0.20	—	—
c	0.09	—	0.20
θ	0°	—	8°

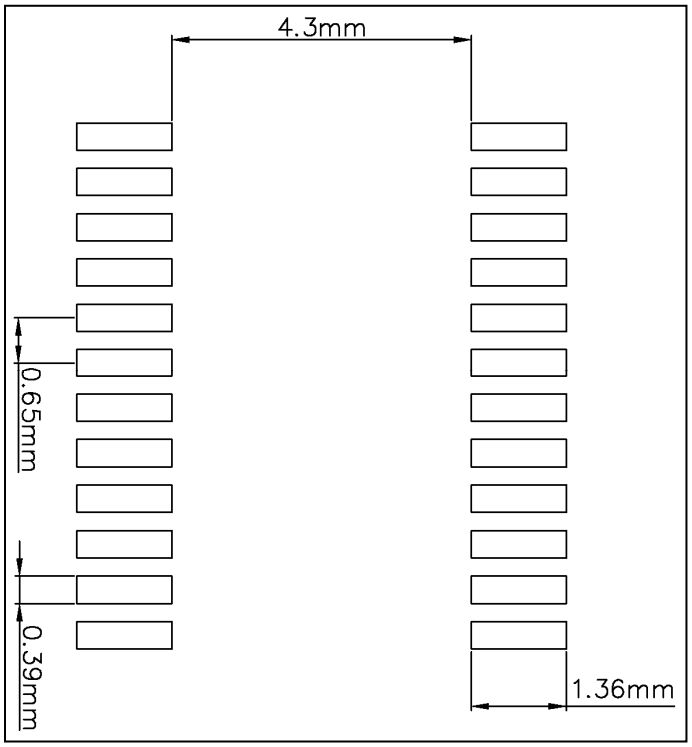
NOTES:
The thermal pad shows different shape among different factories.

RECOMMENDED LAND PATTERN

QFN-24



eTSSOP-24



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
B	Initial release	2013.06.18
C	1. Update the Title 2. Add RECOMMENDED LAND PATTERN 3. Add REVISION HISTORY 4. Add RJA and ESD value 5. Add Figure 2 for Synchronization-Work	2018.05.30