



SN54LS/74LS673 SN54LS/74LS674

DESCRIPTION — The SN54LS/74LS673 and SN54LS/74LS674 are 3-state 16-bit shift registers.

The LS673 is a 16-bit shift register and a 16-bit storage register in a single package. Serial entry and/or data reading is accomplished via a 3-state input/output (SER/Q15) port to the shift register.

Since the storage register is connected in a parallel data loop with the shift register, it may be asynchronously cleared by taking the store-clear input to a low state. The storage register may be parallel loaded with data from the shift register to provide status of the shift register via the parallel outputs. Upon command, the shift register may be parallel loaded with storage register data.

When a high logic level exists at the chip-select (\overline{CS}) input, both the shift register and storage register clocks are disabled, and the SER/Q15 is placed in a high impedance state. The store-clear function is not disabled by the chip-select.

CAUTION! To prevent false clocking of either the shift register or storage register via the chip-select input, the shift clock should be low during low-to-high transition and the store clock should be low during the high-to-low transition of chip-select.

The LS674 is a 16-bit parallel-in, serial-out shift register. Access for serial data entry or reading the shift register word in a recirculating loop is provided by a 3-state input/output (SER/Q15) port.

The LS674 has four basic modes of operation:

1. Hold
2. Write
3. Read
4. Load

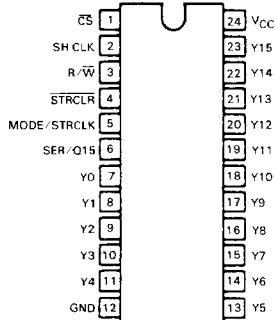
CAUTION! Transition from low-to-high level at the chip-select input should be made only when the clock input is low to avoid false clocking.

16-BIT SHIFT REGISTERS

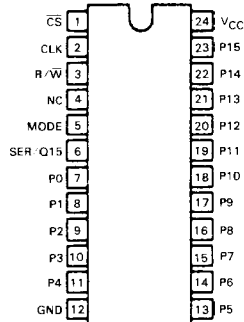
LOW POWER SCHOTTKY

CONNECTION DIAGRAMS (TOP VIEW)

SN54LS/74LS673



SN54LS/74LS674



NC — No internal connection

J Suffix — Case 623-05 (Ceramic)
N Suffix — Case 649-03 (Plastic)

5

FUNCTION TABLES

SN54LS/74LS673

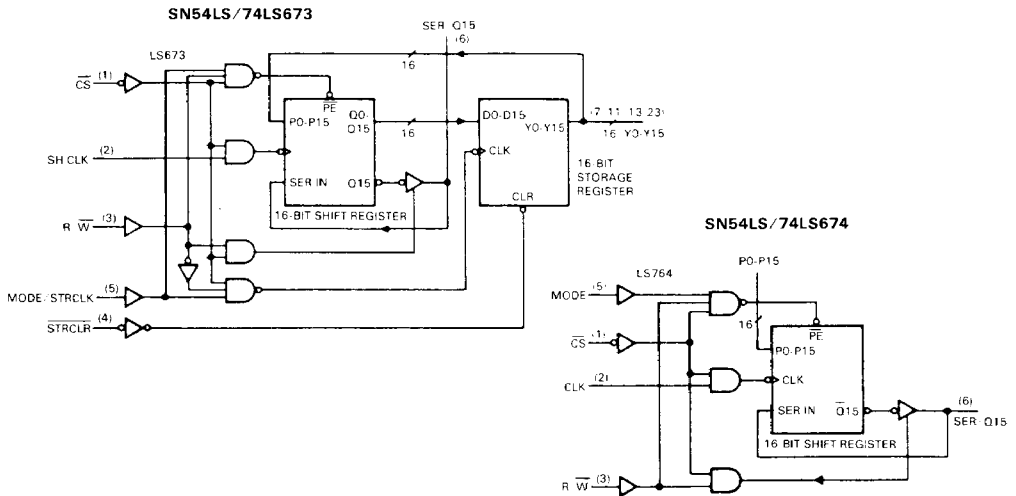
INPUTS					SER/ Q15	SHIFT REGISTER FUNCTIONS				STORAGE REGISTER FUNCTIONS	
\overline{CS}	R/W	SH CLK	STRCLR	MODE/ STRCLK		SHIFT	READ FROM SERIAL OUTPUT	WRITE INTO SERIAL OUTPUT	PARALLEL LOAD	CLEAR	LOAD
H	X	X	X	X	Z	NO	NO	NO	NO		NO
X	X	X	L	X						YES	
L	L	↓	X	X	Z	YES	NO	YES	NO		
L	H	X	X	X	Q15		YES	NO			NO
L	H	↓	X	L	Q14n	YES	YES	NO	NO		NO
L	H	↓	L	H	L	NO	YES		YES	YES	NO
L	H	↓	H	H	Y15n	NO	YES		YES	NO	NO
L	L	X	H	↑	Z		NO		NO	NO	YES

SN54LS/74LS674

INPUTS				SER/ Q15	OPERATION
\overline{CS}	R/W	MODE	CLK		
H	X	X	X	Z	Do nothing
L	L	X	↓	Z	Shift and write (serial load)
L	H	L	↓	Q14n	Shift and read
L	H	H	↓	P15	Parallel load

H = high level (steady state)
 L = low level (steady state)
 ↑ = transition from low to high level
 ↓ = transition from high to low level
 X = irrelevant (any input including transitions)
 Z = high impedance, input mode
 Q14n = content of 14th bit of the shift register before the most recent ↓ transition of the clock.
 Q15 = present content of 15th bit of the shift register
 Y15n = content of the 15th bit of the storage register before the most recent . transition of the clock.
 P15 = level of input P15

BLOCK DIAGRAMS



GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT	
V _{CC}	Supply Voltage		54 74	4.5 4.75	5.0 5.0 5.5 5.25	V	
T _A	Operating Ambient Temperature Range		54 74	-55 0	25 25 125 70	°C	
I _{OH}	Output Current — High	SER/Q15 SER/Q15	54 74			-1.0 -2.6	mA
I _{OL}	Output Current — Low	SER/Q15 SER/Q15	54 74			12 24	mA
I _{OH}	Output Current — High	Y0-Y15	54,74			-0.4	mA
I _{OL}	Output Current — Low	Y0-Y15 Y0-Y15	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	SER/Q15	54 74	2.4 2.4	3.2 3.2	V V	V _{CC} = MIN, I _{OH} = MAX
		Y0-Y15	54 74	2.5 2.7	3.4 3.4	V V	
V _{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I _{OL} = 12 mA I _{OL} = 24 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{OZH}	Output Off Current HIGH				40	μA	V _{CC} = MAX, V _{OUT} = 2.7 V
I _{OZL}	Output Off Current LOW				-400	μA	V _{CC} = MAX, V _{OUT} = 0.4 V
I _{IH}	Input HIGH Current	Others SER/Q15			20 40	μA	V _{CC} = MAX, V _{IN} = 2.7 V V _{CC} = MAX, V _{IN} = 7.0 V V _{CC} = MAX, V _{IN} = 5.5 V
		Others SER/Q15			0.1 0.1	mA	
I _{IL}	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current	Y0-Y15 LS673	-20		-100	mA	V _{CC} = MAX
		SER/Q15	-30		-130	mA	
I _{CC}	Power Supply Current	LS674			40	mA	V _{CC} = MAX
		LS673			80		

AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$

SYMBOL	PARAMETER	LIMITS						UNITS	TEST CONDITIONS
		LS673			LS674				
		MIN	TYP	MAX	MIN	TYP	MAX		
f_{MAX}	Maximum Clock Frequency	20	28		20	28		MHz	$V_{\text{CC}} = 5.0\text{ V}$ $C_L = 45\text{ pF}$, $R_L = 667\Omega$
t_{PLH} t_{PHL}	Propagation Delay, MODE/STRCLK to Y0-Y15		28 30	45 45				ns	
t_{PHL}	Propagation Delay, STRCLR to Y0-Y15		25	40				ns	
t_{PLH} t_{PHL}	Propagation Delay, SH CLK to SER/Q15		21 26	33 40					
t_{PLH} t_{PHL}	Propagation Delay, CLK to SER/Q15					21 26	33 40	ns	
t_{PZH} t_{PZL}	Output Enable Time, $\overline{\text{CS}}$, R/ $\overline{\text{W}}$ to SER/Q15		30 30	45 45		30 30	45 45	ns	
t_{PLZ} t_{PHZ}	Output Disable Time, $\overline{\text{CS}}$, R/ $\overline{\text{W}}$ to SER/Q15		25 25	40 40		25 25	40 40	ns	

AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Clock Clear Pulse Width	20			ns	$V_{\text{CC}} = 5.0\text{ V}$
t_s	Setup Time, SER/Q15, P0-P15	20			ns	
t_s	Setup Time, MODE, R/ $\overline{\text{W}}$, $\overline{\text{CS}}$	35			ns	
t_h	Hold Time, Any Input	0			ns	