RAMBUS®
RIMM™ MODULE

MT4VR3216A, MT4VR3218A, MT6VR4816A, MT6VR4818A, MT8VR6416A, MT8VR6418A, MT16VR12816A, MT16VR12818A

For the latest data sheet revisions, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- 184-pin RIMM™ module, 1mm pin spacing
- 32 Meg x 16/18 (64MB/72MB), 48 Meg x 16/18 (96MB/108MB), 64 Meg x 16/18 (128MB/144MB), 128 Meg x 16/18 (256MB/288MB)
- Uses (4, 6, 8, or 16) 8 Meg x 16/18 Direct RDRAM® devices
- High-speed 356 MHz and 400 MHz clocks with 2x data rates
- 1.6 GB/s peak I/O bandwidth
- Rambus® signaling level (RSL) using differential 356 MHz and 400 MHz transmit and receive clocks
- Packet-oriented Rambus protocol transmitted in 8-bit-long packets
- Separate control and data buses for increased data bandwidth capability
- Control bus with separate row and column buses for easier command scheduling
- Programmable output delay timing for round-trip delay of one to five cycles
- Write buffer to reduce READ latency
- Three precharge mechanisms for controller flexibility
- Programmable power states for flexibility in power consumption versus data access time
- Power-down Self Refresh and active refresh
- 32ms, 16,384 cycle refresh
- 2.5V power supply with 1.8V CMOS supply for I/Os

OPTIONS — MARKING

- Package
  184-pin RIMM module (gold) — G
- Timing (Cycle Time)
  356 MHz Clock Rate, Access Time = 50ns — -750
  356 MHz Clock Rate, Access Time = 45ns — -745
  400 MHz Clock Rate, Access Time = 50ns — -850
  400 MHz Clock Rate, Access Time = 45ns — -845
  400 MHz Clock Rate, Access Time = 40ns — -840
- Component Revision Designator
  Alpha character — Factory Defined
- Printed Circuit Board Revision Designator
  Numeric character — Factory Defined

PIN ASSIGNMENT
184-Pin RIMM Module

PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK
1	GND	93	GND	47	NC	139	NC
2	LDQA8*	94	LDQA7	48	NC	140	NC
3	GND	95	GND	49	NC	141	NC
4	LDQA6	96	LDQA5	50	NC	142	NC
5	GND	97	GND	51	V_{REF}	143	V_{REF}
6	LDQA4	98	LDQA3	52	GND	144	GND
7	GND	99	GND	53	SCL	145	SA0
8	LDQA2	100	LDQA1	54	V_{DD}	146	V_{DD}
9	GND	101	GND	55	SDA	147	SA1
10	LDQA0	102	LCFM	56	SV_{DD}	148	SV_{DD}
11	GND	103	GND	57	SWP	149	SA2
12	LCTMN	104	LCFMN	58	V_{DD}	150	V_{DD}
13	GND	105	GND	59	RSCK	151	RCMD
14	LCTM	106	NC	60	GND	152	GND
15	GND	107	GND	61	RDQB7	153	RDQB8*
16	NC	108	LROW2	62	GND	154	GND
17	GND	109	GND	63	RDQB5	155	RDQB6
18	LROW1	110	LROW0	64	GND	156	GND
19	GND	111	GND	65	RDQB3	157	RDQB4
20	LCOL4	112	LCOL3	66	GND	158	GND
21	GND	113	GND	67	RDQB1	159	RDQB2
22	LCOL2	114	LCOL1	68	GND	160	GND
23	GND	115	GND	69	RCOL0	161	RDQB0
24	LCOL0	116	LDQB0	70	GND	162	GND
25	GND	117	GND	71	RCOL2	163	RCOL1
26	LDQB1	118	LDQB2	72	GND	164	GND
27	GND	119	GND	73	RCOL4	165	RCOL3
28	LDQB3	120	LDQB4	74	GND	166	GND
29	GND	121	GND	75	RROW1	167	RROW0
30	LDQB5	122	LDQB6	76	GND	168	GND
31	GND	123	GND	77	NC	169	RROW2
32	LDQB7	124	LDQB8*	78	GND	170	GND
33	GND	125	GND	79	RCTM	171	NC
34	LSCK	126	LCMD	80	GND	172	GND
35	V_{CMOS}	127	V_{CMOS}	81	RCTMN	173	RCFMN
36	SOUT	128	SIN	82	GND	174	GND
37	V_{CMOS}	129	V_{CMOS}	83	RDQA0	175	RCFM
38	NC	130	NC	84	GND	176	GND
39	GND	131	GND	85	RDQA2	177	RDQA1
40	NC	132	NC	86	GND	178	GND
41	V_{DD}	133	V_{DD}	87	RDQA4	179	RDQA3
42	V_{DD}	134	V_{DD}	88	GND	180	GND
43	NC	135	NC	89	RDQA6	181	RDQA5
44	NC	136	NC	90	GND	182	GND
45	NC	137	NC	91	RDQA8*	183	RDQA7
46	NC	138	NC	92	GND	184	GND

*Nonfunctional on x16 devices.

GENERAL DESCRIPTION

The MT4VR3216/18A, MT6VR4816/18A, MT8VR6416/18A and MT16VR12816/18A RDRAM RIMM modules are general-purpose, high-performance, packet-oriented, dynamic random-access memories configured as 64MB/72MB, 96MB/108MB, 128/144MB and 256MB/288MB densities. The RIMM modules consist of 4, 6, 8, or 16 Direct RDRAM devices organized as 8M words by 16 or 18 bits.

The RIMM modules use Rambus signaling level (RSL) technology to achieve 356 MHz or 400 MHz clock speeds using differential clocks. Control and I/O data is transferred on both the rising and falling edges of the clock. This allows data transfers at 1.25ns per two bytes (10ns per 16 bytes) during peak operation.

All DRAM commands are communicated to the RIMM modules through a 3-bit row or 5-bit column bus inpackets which are 8 bits in length. These packets are then decoded on the RDRAM into the operation and address requiring access.

Initialization and mode configurations for the RIMM modules are accessed through slow speed CMOS Serial I/O interface.

The architecture of Direct RDRAMs allows high sustained bandwidth memory transactions for multiple, simultaneous, semi-random addresses. Each Direct RDRAM's thirty-two banks can support up to four simultaneous transactions (within bank restrictions).

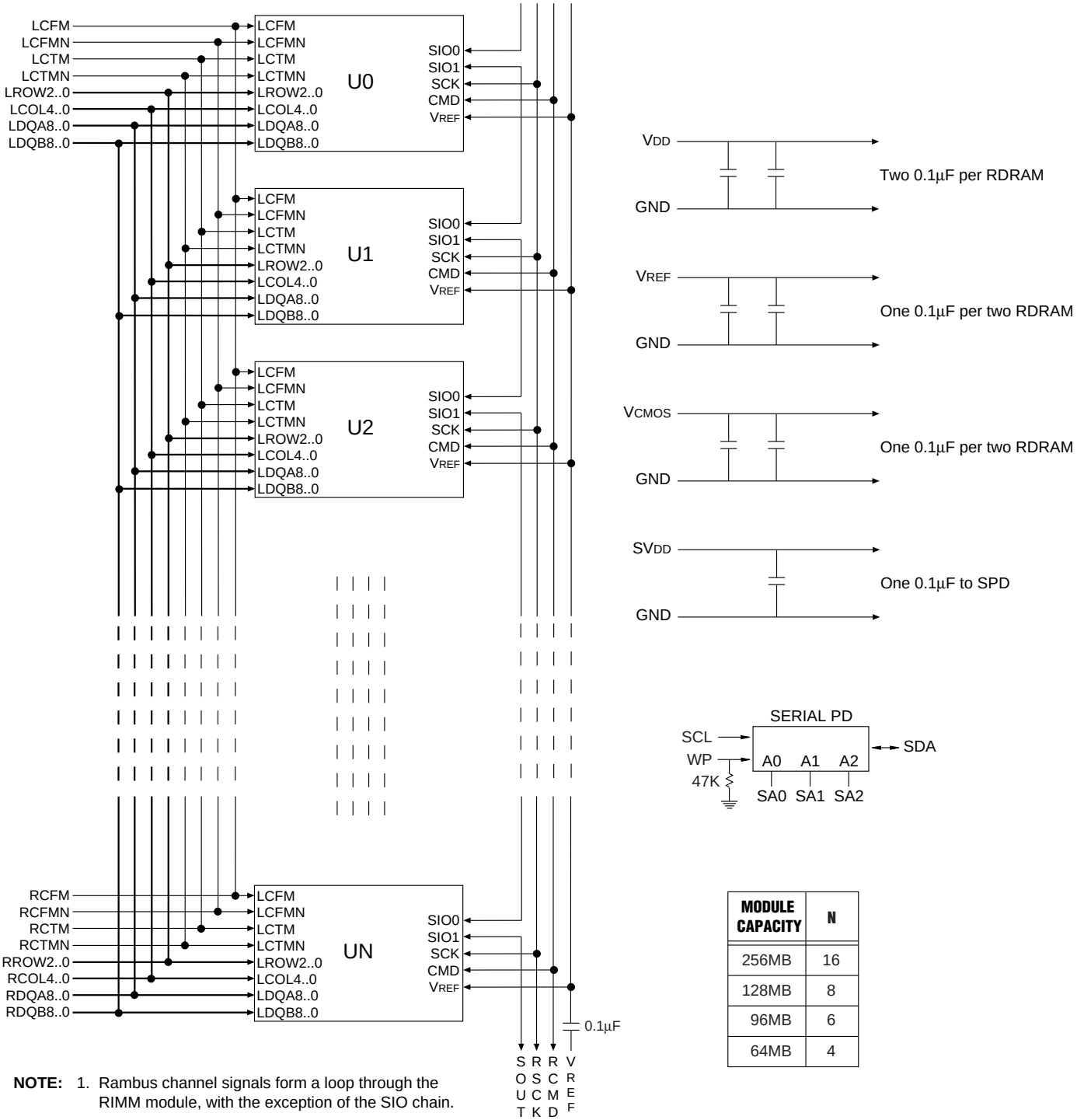
System-oriented features include power management, byte masking and x16/18 organization. The two data bits in the x18 organization are general and can be used for additional storage, bandwidth, or for error correction.

PART NUMBERS

PART NUMBER	CONFIGURATION	CLK FREQ. (MHz)	ACCESS TIME (ns)
MT4VR3216AG-750__	32 Meg x 16	356	50
MT4VR3216AG-745__	32 Meg x 16	356	45
MT4VR3216AG-850__	32 Meg x 16	400	50
MT4VR3216AG-845__	32 Meg x 16	400	45
MT4VR3216AG-840__	32 Meg x 16	400	40
MT4VR3218AG-750__	32 Meg x 18	356	50
MT4VR3218AG-745__	32 Meg x 18	356	45
MT4VR3218AG-850__	32 Meg x 18	400	50
MT4VR3218AG-845__	32 Meg x 18	400	45
MT4VR3218AG-840__	32 Meg x 18	400	40
MT6VR4816AG-750__	48 Meg x 16	356	50
MT6VR4816AG-745__	48 Meg x 16	356	45
MT6VR4816AG-850__	48 Meg x 16	400	50
MT6VR4816AG-845__	48 Meg x 16	400	45
MT6VR4816AG-840__	48 Meg x 16	400	40
MT6VR4818AG-750__	48 Meg x 18	356	50
MT6VR4818AG-745__	48 Meg x 18	356	45
MT6VR4818AG-850__	48 Meg x 18	400	50
MT6VR4818AG-845__	48 Meg x 18	400	45
MT6VR4818AG-840__	48 Meg x 18	400	40
MT8VR6416AG-750__	64 Meg x 16	356	50
MT8VR6416AG-745__	64 Meg x 16	356	45
MT8VR6416AG-850__	64 Meg x 16	400	50
MT8VR6416AG-845__	64 Meg x 16	400	45
MT8VR6416AG-840__	64 Meg x 16	400	40
MT8VR6418AG-750__	64 Meg x 18	356	50
MT8VR6418AG-745__	64 Meg x 18	356	45
MT8VR6418AG-850__	64 Meg x 18	400	50
MT8VR6418AG-845__	64 Meg x 18	400	45
MT8VR6418AG-840__	64 Meg x 18	400	40
MT16VR12816AG-750__	128 Meg x 16	356	50
MT16VR12816AG-745__	128 Meg x 16	356	45
MT16VR12816AG-850__	128 Meg x 16	400	50
MT16VR12816AG-845__	128 Meg x 16	400	45
MT16VR12816AG-840__	128 Meg x 16	400	40
MT16VR12818AG-750__	128 Meg x 18	356	50
MT16VR12818AG-745__	128 Meg x 18	356	45
MT16VR12818AG-850__	128 Meg x 18	400	50
MT16VR12818AG-845__	128 Meg x 18	400	45
MT16VR12818AG-840__	128 Meg x 18	400	40

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT8VR6416AG-750B1

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. Rambus channel signals form a loop through the RIMM module, with the exception of the SIO chain.

MODULE CAPACITY	N
256MB	16
128MB	8
96MB	6
64MB	4

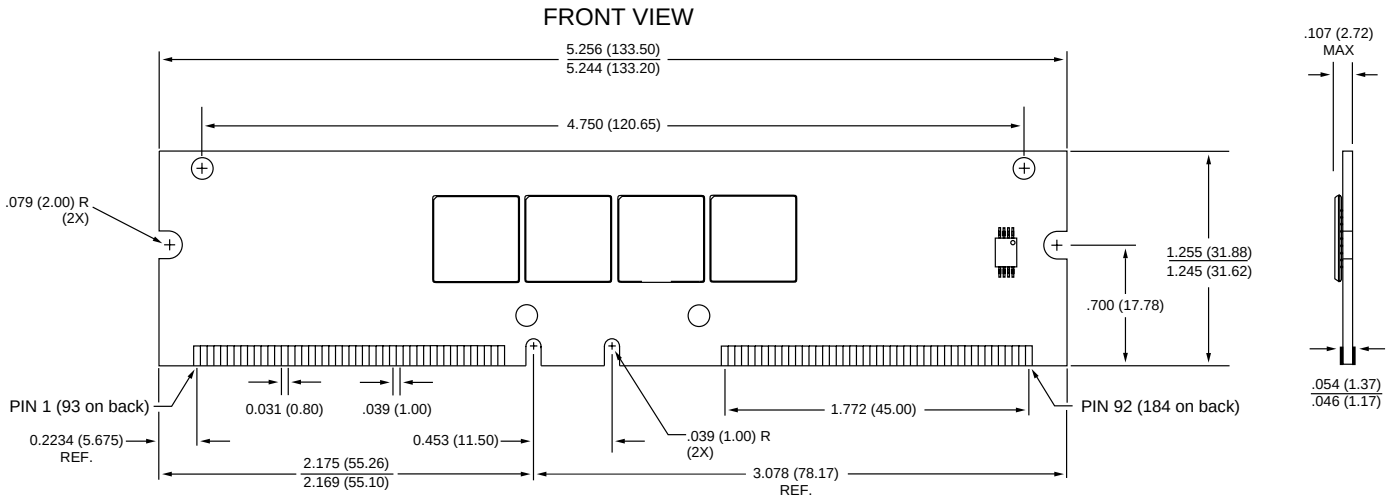
PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	I/O	TYPE	DESCRIPTION
102	LCFM	I	RSL	Clock from Master: Interface clock used for receiving RSL signals from the Channel. Positive polarity.
104	LCFMN	I	RSL	Clock from Master: Interface clock used for receiving RSL signals from the Channel. Negative polarity.
12	LCTMN	I	RSL	Clock to Master: Interface clock used for transmitting RSL signals from the Channel. Negative polarity.
14	LCTM	I	RSL	Clock to Master: Interface clock used for transmitting RSL signals from the Channel. Positive polarity.
2, 94, 4, 96, 6, 98, 8, 100, 10	LDQA8..0	I/O	RSL	Data Bus A: A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQA8 is non-functional on x16 devices.
124, 32, 122, 30, 120, 28, 118, 26, 116	LDQB8..0	I/O	RSL	Data Bus B: A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQB8 is non-functional on x16 devices.
108, 18, 110	LROW2..0	I	RSL	Row Bus: 3-bit bus containing control and address information for row accesses.
20, 112, 22, 114, 24	LCOL4..0	I	RSL	Column Bus: 5-bit bus containing control and address information for Column accesses.
175	RCFM	I	RSL	Clock from Master: Interface clock used for receiving RSL signals from the Channel. Positive polarity.
173	RCFMN	I	RSL	Clock from Master: Interface clock used for receiving RSL signals from the Channel. Negative polarity.
81	RCTMN	I	RSL	Clock to Master: Interface clock used for transmitting RSL signals from the Channel. Negative polarity.
79	RCTM	I	RSL	Clock to Master: Interface clock used for transmitting RSL signals from the Channel. Positive polarity.
91, 183, 89, 181, 87, 179, 85, 177, 83	RDQA8..0	I/O	RSL	Data Bus A: A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQA8 is non-functional on x16 devices.
153, 61, 155, 63, 157, 65, 159, 67, 161	RDQB8..0	I/O	RSL	Data Bus B: A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQB8 is non-functional on x16 devices.
169, 75, 167	RROW2..0	I	RSL	Row Bus: 3-bit bus containing control and address information for row accesses.
73, 165, 71, 163, 69	RCOL4..0	I	RSL	Column Bus: 5-bit bus containing control and address information for Column accesses.
36	SOUT	I/O	CMOS	Serial I/O: Pin for reading from and writing to the control registers. Attaches to SIO1 of the last RDRAM on the module.
128	SIN	I/O	CMOS	Serial I/O: Pin for reading from and writing to the control registers. Attaches to SIO0 of the first RDRAM on the module.

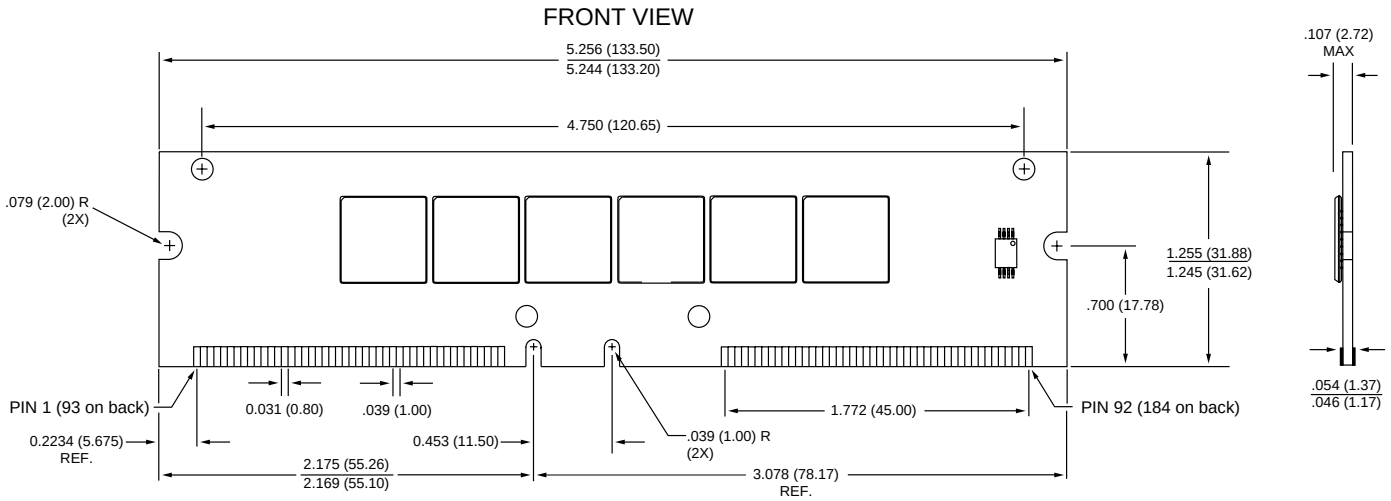
PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	I/O	TYPE	DESCRIPTION
35, 37, 127, 129	V_{CMOS}			Supply voltage for CMOS level signals.
126	LCMD	I	CMOS	Serial Command Pin: Pin used to read from and write to the control registers. Also used for power management.
34	LSCK	I	CMOS	Clock Input: Pin used to read from and write to the control registers.
151	RCMD	I	CMOS	Serial Command Input: Pin used to read from and write to the control registers. Also used for power management.
59	RSCK	I	CMOS	Clock Input: Pin used to read from and write to the control registers.
53	SCL	I	CMOS	Serial Presence-Detect Clock.
55	SDA	I/O	CMOS	Serial Presence-Detect Data (Open Collector I/O).
57	SWP	I	CMOS	Serial Presence-Detect Write Protect (active high). When low, the SPD can be written as well as read.
145	SA0	I	CMOS	Serial Presence-Detect Address 0
147	SA1	I	CMOS	Serial Presence-Detect Address 1
149	SA2	I	CMOS	Serial Presence-Detect Address 2
41, 42, 54, 58, 133, 134, 146, 150	V_{DD}			Supply voltage for the RDRAM core and interface logic.
56, 148	SV_{DD}			SPD voltage. Used for signals SCL, SDA, SWE, SA0, SA1 and SA2.
51, 143	V_{REF}			Logic threshold reference voltage for RSL signals.
1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33, 39, 52, 60, 62, 64, 66, 68, 70, 72, 74, 76, 78, 80, 82, 84, 86, 88, 90, 92, 93, 95, 97, 99, 101, 103, 105, 107, 109, 111, 113, 115, 117, 119, 121, 123, 125, 131, 144, 152, 154, 156, 158, 160, 162, 164, 166, 168, 170, 172, 174, 176, 178, 180, 182, 184	GND			Ground reference for RDRAM core and interface.
16, 38, 40, 43-50, 77, 106, 130, 132, 135-142, 171	NC (24)			No Connection. These 24 pins are all reserved for future use.

184-PIN RIMM MODULE
(64MB/72MB)

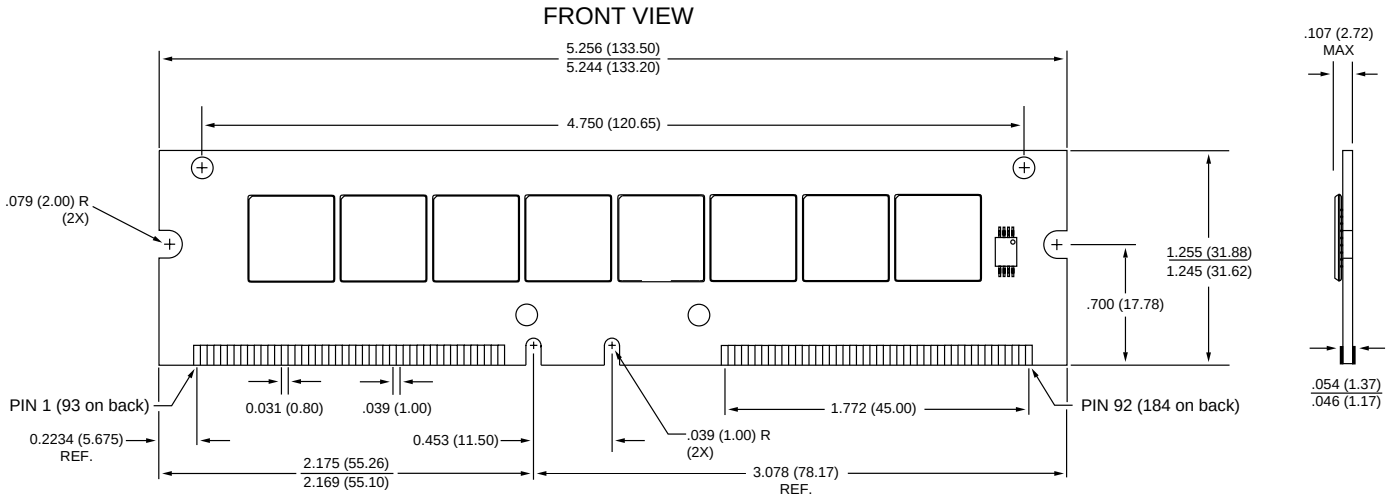


184-PIN RIMM MODULE
(96MB/108MB)

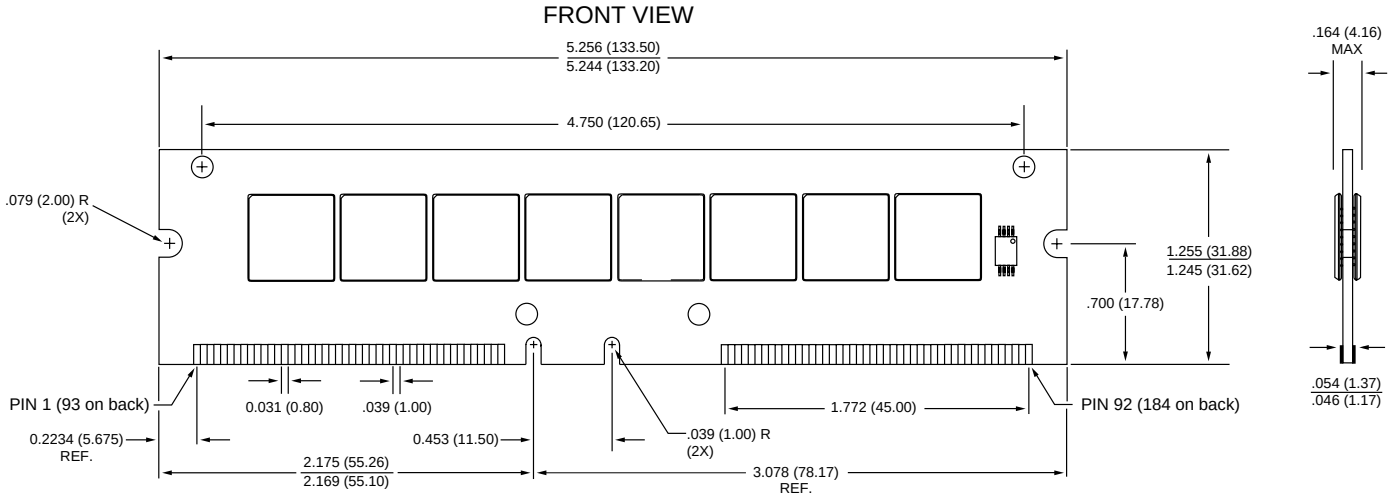


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

184-PIN RIMM MODULE
(128MB/144MB)



184-PIN RIMM MODULE
(256MB/288MB)



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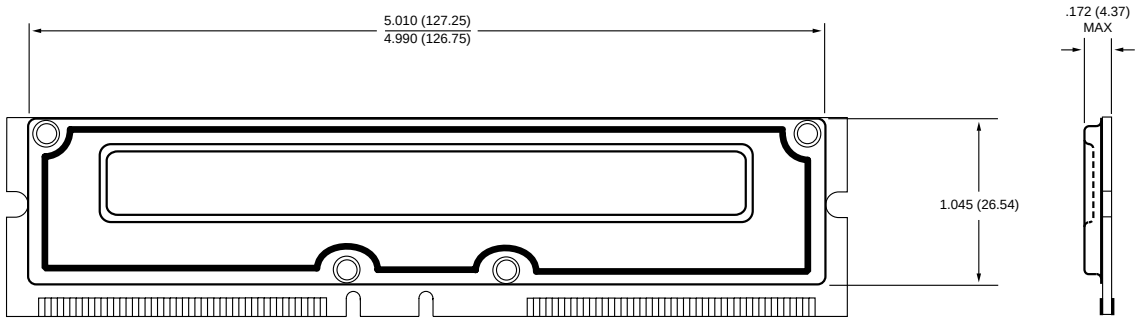
184-PIN RIMM MODULE

FRONT VIEW WITH HEAT SPREADER



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8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
E-mail: prodmktg@micron.com, Internet: http://www.micron.com, Customer Comment Line: 800-932-4992