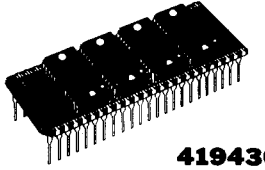
MH25616PNA-10,-12



4194304-BIT(262144-WORD BY 16-BIT)PSEUDO-PSEUDO STATIC RAM

DESCRIPTION

The MH25616PNA is 262144 word x 16 bit PSEUDO-PSEUDO static RAM and consist of four industry standard 256K x 4 bit dynamic RAMs in SOJ, two data selector in SOP and one DRAM controller in SOP. The mounting of SOJ and SOP on a dual in-line package provides any application where high densities and large quantities of memory are required.

FEATURES

Type	Access time (max) Note 1	Power dissipation (typ)
MH25616PNA-10	136ns	750mW
MH25616PNA-12	156ns	650mW

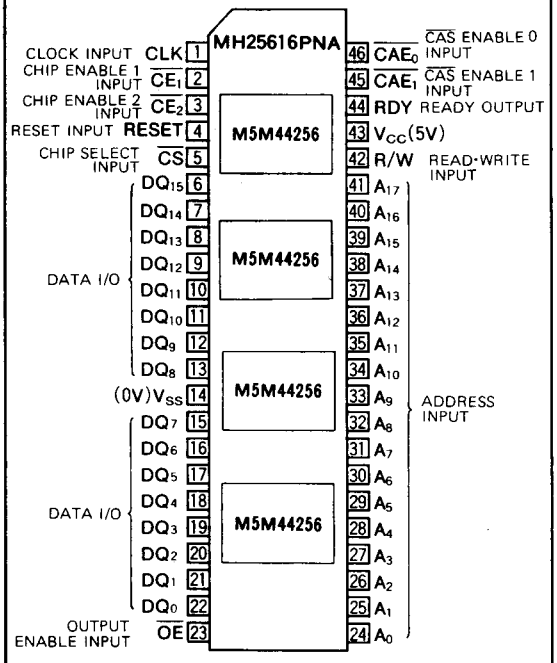
Note 1: When No-wait operation, Access time is measured from end of T1 of clock.

- Single +5V (±10%) supply operation
- 46 pin 600 mil Dual in-line package
- No Refresh
- All inputs and outputs are directly TTL compatible
- Includes (0.22μF x 7) decoupling capacitors

APPLICATION

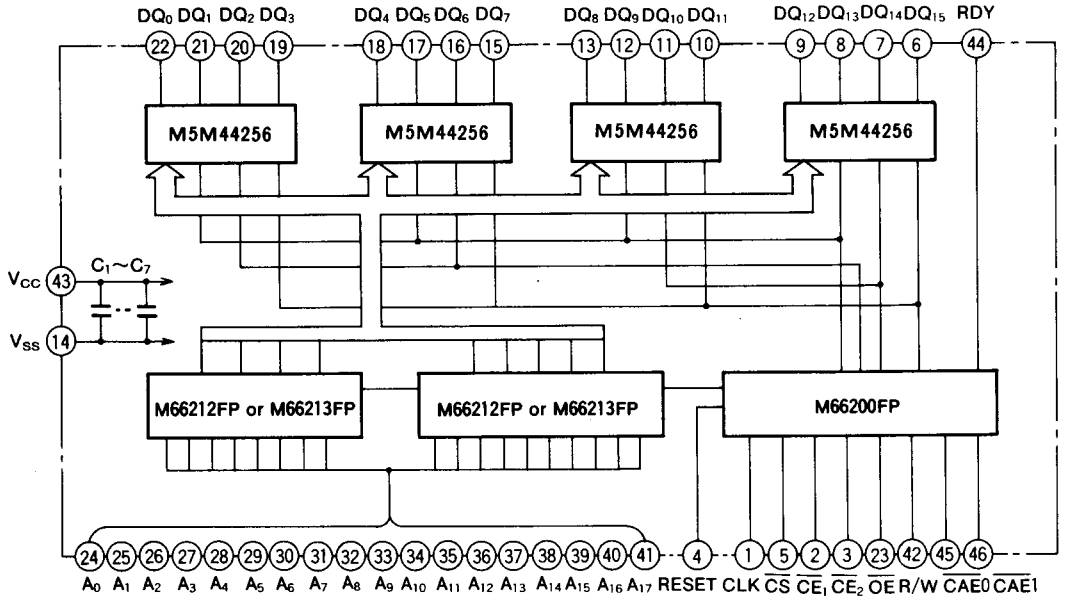
Small Capacity Memory Units

PIN CONFIGURATION (TOP VIEW)



Outline 46N1

BLOCK DIAGRAM



4194304-BIT(262144-WORD BY 16-BIT)PSEUDO-PSEUDO STATIC RAM

FUNCTION

MH25616PNA series is 262144 word by 16-bit. These devices operate on a single 5V supply, and all inputs and outputs are directly TTL compatible.

When DRAM controller counted 117th clock pulse from CLK terminal, DRAM is automatically refreshed. Accordingly, Outside refreshing is not required.

Multiplexer enable to put separate address in as SRAM.

Internal action of the MH51208PNA is of the same period as clock pulse and 1 state (time of one read or write cycle) consists of 4 clock pulses.

A write cycle is executed whenever the low level $\overline{CE_1}$ overlaps with the low level $\overline{CS}$ at the last "H" → "L" edge of T_1 (first clock pulse of write cycle). The address is determined by $\overline{CAE_0}$, $\overline{CAE_1}$ and $A_0 \sim A_{17}$.

The data is latched into a cell on the last "H" → "L" edge of T_2 (second clock pulse of write cycle) requiring the set-up and hold time relative to this edge to be maintained.

A read cycle is executed whenever the low level $\overline{CE_2}$ overlaps with the low level $\overline{CS}$ at the last "H" → "L" edge of T_1. When address is determined by $\overline{CAE_0}$, $\overline{CAE_1}$ and $A_0 \sim A_7$, data situated on the address is read.

When setting $\overline{CS}$ at high level or $\overline{CE_1}$ and $\overline{CE_2}$ at the same time at high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in floating state.

DESCRIPTION OF PINS

<table>
<tr><th>I/O</th><th>Symbol</th><th>Function</th></tr>
<tr><td></td><td>RESET</td><td>Reset input
This input resets built-in flip flop and is active H.</td></tr>
<tr><td></td><td>CLK</td><td>Clock input</td></tr>
<tr><td></td><td>$\overline{CS}$
$\overline{CE_1}$, $\overline{CE_2}$</td><td>Decode signal of CPU address
Status signal from CPU
The memory access cycle is started by $\overline{CS}$, $\overline{CE_1}$ and $\overline{CE_2}$ signals.
<table>
<tr><th>$\overline{CS}$</th><th>$\overline{CE_1}$</th><th>$\overline{CE_2}$</th><th>Mode</th></tr>
<tr><td>H</td><td>Don't care</td><td>Don't care</td><td>No-access</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>Read</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>Write</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>Read</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>No-access</td></tr>
</table></td></tr>
<tr><td></td><td>$\overline{OE}$</td><td>Read signal from CPU (assumed that read cycle finish)</td></tr>
<tr><td></td><td>R/W</td><td>Write signal from CPU (assumed that write cycle finish)</td></tr>
<tr><td></td><td>$\overline{CAE0}$
$\overline{CAE1}$</td><td>Determine the valid combination of CAS
$\overline{CAS}$ is output by active L.
<table>
<tr><th>$\overline{CAE0}$</th><th>$\overline{CAE1}$</th><th>Access area</th></tr>
<tr><td>H</td><td>H</td><td>—</td></tr>
<tr><td>L</td><td>H</td><td>$DQ_{0\sim7}$</td></tr>
<tr><td>H</td><td>L</td><td>$DQ_{8\sim15}$</td></tr>
<tr><td>L</td><td>L</td><td>$DQ_{0\sim15}$</td></tr>
</table></td></tr>
<tr><td></td><td>$A_0 \sim A_{17}$</td><td>Address signal</td></tr>
<tr><td>Output</td><td>RDY</td><td>Read signal to CPU</td></tr>
<tr><td>Input</td><td>$DQ_{0\sim15}$</td><td>Data input/output signal</td></tr>
</table>

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.5～7.0	V
V_I	Input voltage		−0.5～V_{CC}+0.5	V
V_O	Output voltage		−0.5～V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I< 0V	−20	mA
		V_I> V_{CC}	+20	
I_O	Output current		50	mA
Pd	Power dissipation	Ta＝25°C	5500	mW
Topr	Operating temperature		0～70	°C
Tstg	Storage temperature		−40～125	°C

RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted) (Note 2)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V

Note 2: All voltage valves are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, V_{CC}＝5V±10%, V_{SS}＝0V, unless otherwise noted) (Note 3)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{T+}	Threshold voltage (RESET)		V_O＝0.1, V_{CC}−0.1V, I_O＝20μA			2.4	V
V_{T-}	Threshold voltage (RESET)		V_O＝0.1, V_{CC}−0.1V, I_O＝20μA	0.6			V
V_{T+}−V_{T-}	Hysteresis width (RESET)		V_O＝0.1, V_{CC}−0.1V, I_O＝20μA	0.2		1.8	V
V_{IH}	High input voltage (other input)		V_O＝0.1, V_{CC}−0.1V, I_O＝20μA	2.0			V
V_{IL}	Low input voltage (other input)		V_O＝0.1, V_{CC}−0.1V, I_O＝20μA			0.4	V
V_{OH}	High output voltage		I_{OH}＝−5mA	2.4		V_{CC}	V
V_{OL}	Low output voltage		I_{OL}＝4.2mA	0		0.4	V
I_{IH}	High input current		V_I＝V_{CC}			1.0	μA
I_{IL}	Low input current		V_I＝GND			1.0	μA
$I_{CC1(AV)}$	Average supply current from operating (Note 4, 5)	MH25616PNA-10	Maximum repeating frequency, output open			240	mA
		MH25616PNA-12				200	
$I_{CC2(1)}$	Average supply current from V_{CC}, stand by		V_I＝2.4V, 0.4V, Output open (Note 6)			16.7	mA
$I_{CC2(2)(AV)}$			V_I＝V_{CC}, GND, f＝10MHz Output open (Note 4, 7)		3.5		mA
$I_{CC2(AV)}$	Average supply current from $\overline{V_{CC}}$, $\overline{CAS}$ before $\overline{RAS}$ refreshing (Note 4)	MH25616PNA-10	Refresh cycling, output open (5 clock from 117th clock)			240	mA
		MH25616PNA-12				220	
$C_{I(A)}$	Input capacitance,,address inputs		V_I＝V_{SS}, f＝1MHz V_I＝25mVrms			15	pF
C_I	Input capacitance (except address inputs)					15	pF
$C_{(DQ)}$	Input/output capacitance, Data input/output inputs					17	pF
$C_{O(RDY)}$	Output capacitance, RDY inputs		V_O＝V_{SS}, f＝1MHz, V_i＝25mVrms			10	pF

Note 3: Current flowing into IC is positive, out is negative.
4: $I_{CC1(AV)}$, $I_{CC2(2)(AV)}$, $I_{CC3(AV)}$ are dependent on frequency of clock pulse. Limits are measured at maximum frequency.
5: $I_{CC1(AV)}$ is dependent on output loading specified values are obtained with the output open.
6: Only one input set to this value, all other input fix V_{CC} or GND.
7: The value is setting to I_{CC3}, when it get in refresh cycle every 121 clock.

SWITCHING CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 8)

Symbol	Parameter	Limits						Unit
		MH25616PNA-10			MH25616PNA-12			
		Min	Typ	Max	Min	Typ	Max	
f	Repeating frequency	7.8		11.1	7.8		9.95	MHz
t_{PLH}	CLK, $\overline{OE}$, R/W-RDY propagation time (Note 9)			36			36	ns
t_{PHL}				36			36	ns
t_{CKA}	CLK access time			136			156	ns
t_{OFF}	Output disable time after $\overline{OE}$ high	40		65	40		70	ns

Note 8: After power-up an initial pause of 500μs and dummy cycle (Read or Write cycle by 8 times degrees) followed by CLK, $\overline{CS}$, $\overline{CE_1}$, $\overline{CE_2}$, $\overline{OE}$, R/W cycles are required before proper device operation is achieved. It may add that cycle during the initial pause, but dummy cycle is required.

9: The values are measured at loading capacitance C_L = 50pF.

TIMING REQUIREMENTS (T_a=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 10, 11)

Read, Write, Refresh Mode Cycle

Symbol	Parameter	Limits						Unit
		MH25616PNA-10			MH25616PNA-12			
		Min	Typ	Max	Min	Typ	Max	
t_{CKL}	CLK low pulse width	40		75	45		70	ns
t_{CKH}	CLK high pulse width	40		75	45		70	ns
t_{CSS}	CLK-$\overline{CS}$ setup time	20			20			ns
t_{CSH}	CLK-$\overline{CS}$ hold time	20			20			ns
t_{CE1S}	CLK-$\overline{CE_1}$ setup time	20			20			ns
t_{CE1H}	CLK-$\overline{CE_1}$ hold time	20			20			ns
t_{CE2S}	CLK-$\overline{CE_2}$ setup time	20			20			ns
t_{CE2H}	CLK-$\overline{CE_2}$ hold time	20			20			ns
t_{OES}	CLK-$\overline{OE}$ setup time	20			20			ns
t_{OEH}	CLK-$\overline{OE}$ hold time	1.5CK+10		2.5CK−20	1.5CK+10		2.5CK−20	ns
t_{RWS}	CLK-R/W setup time	20			20			ns
t_{RWH}	CLK-R/W hold time	1.0CK+10		2.0CK−20	1.0CK+10		2.0CK−20	ns
t_{AS}	CLK-ADDRESS setup time	20			20			ns
t_{AH}	CLK-ADDRESS hold time (READ)	55			55			ns
	CLK-ADDRESS hold time (WRITE)	0.5CK+55			0.5CK+55			
t_{CAS}	CLK-$\overline{CAE}$ setup time	20			20			ns
t_{CAH}	CLK-$\overline{CAE}$ hold time	20			20			ns
t_{DS}	CLK-DATA setup time	0			0			ns
t_{DH}	CLK-DATA hold time	55			60			ns
t_T	Transition time (Note 12)	3		50	3		50	ns
t_{REF}	Refresh cycle time (every 121 clocks)	10.9		15.7	12.1		15.7	μs

Note 10: The timing requirements are assumed t_T = 5ns.

11: V_I = 1.3V is reference levels for measuring timing of input signals.

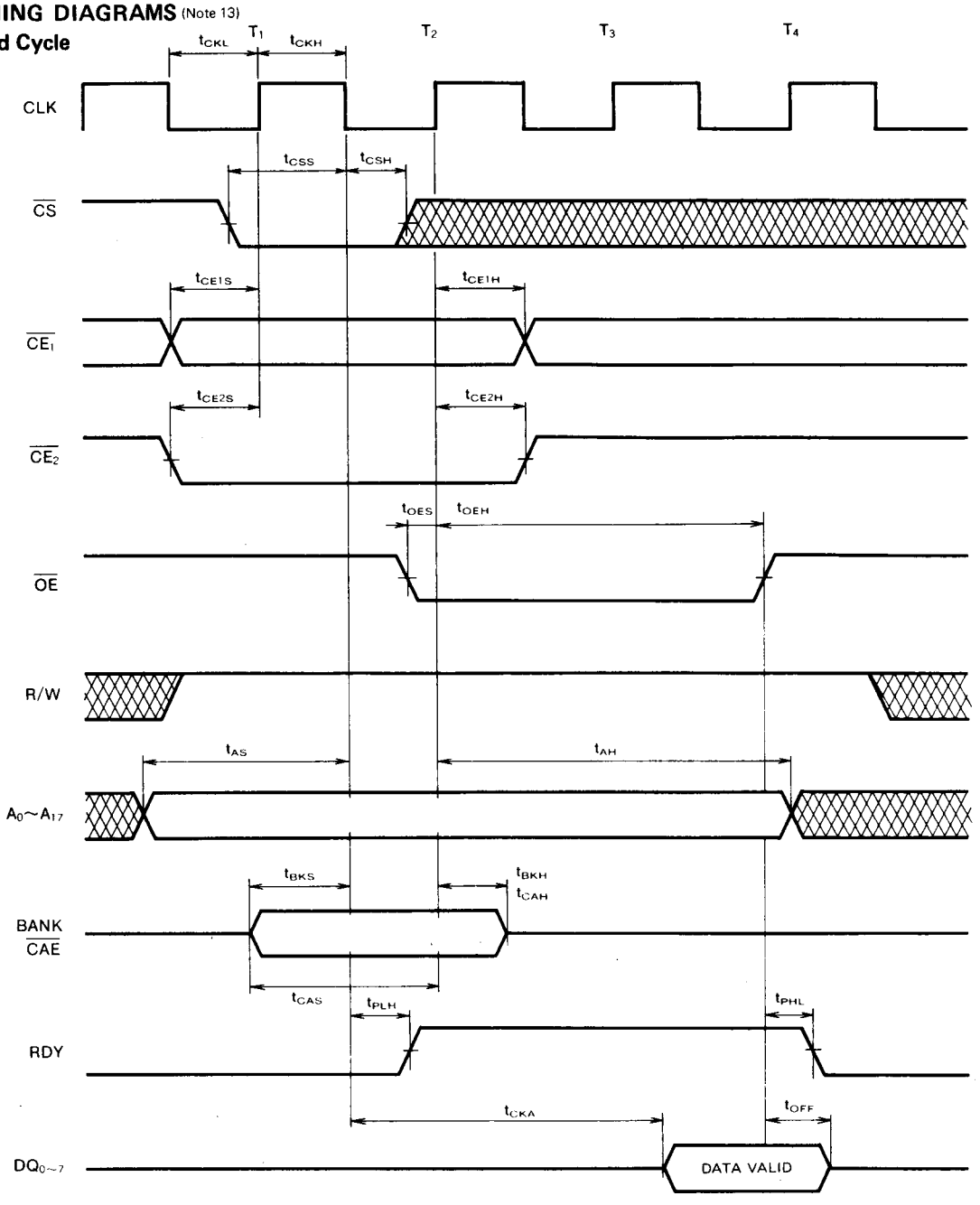
12: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Reset-Mode-Cycle

Symbol	Parameter	Limits						Unit
		MH25616PNA-10			MH25616PNA-12			
		Min	Typ	Max	Min	Typ	Max	
t_{REW}	RESET pulse width	20			20			ns
t_{REC}	CLK-RESET recovery time	20			20			ns

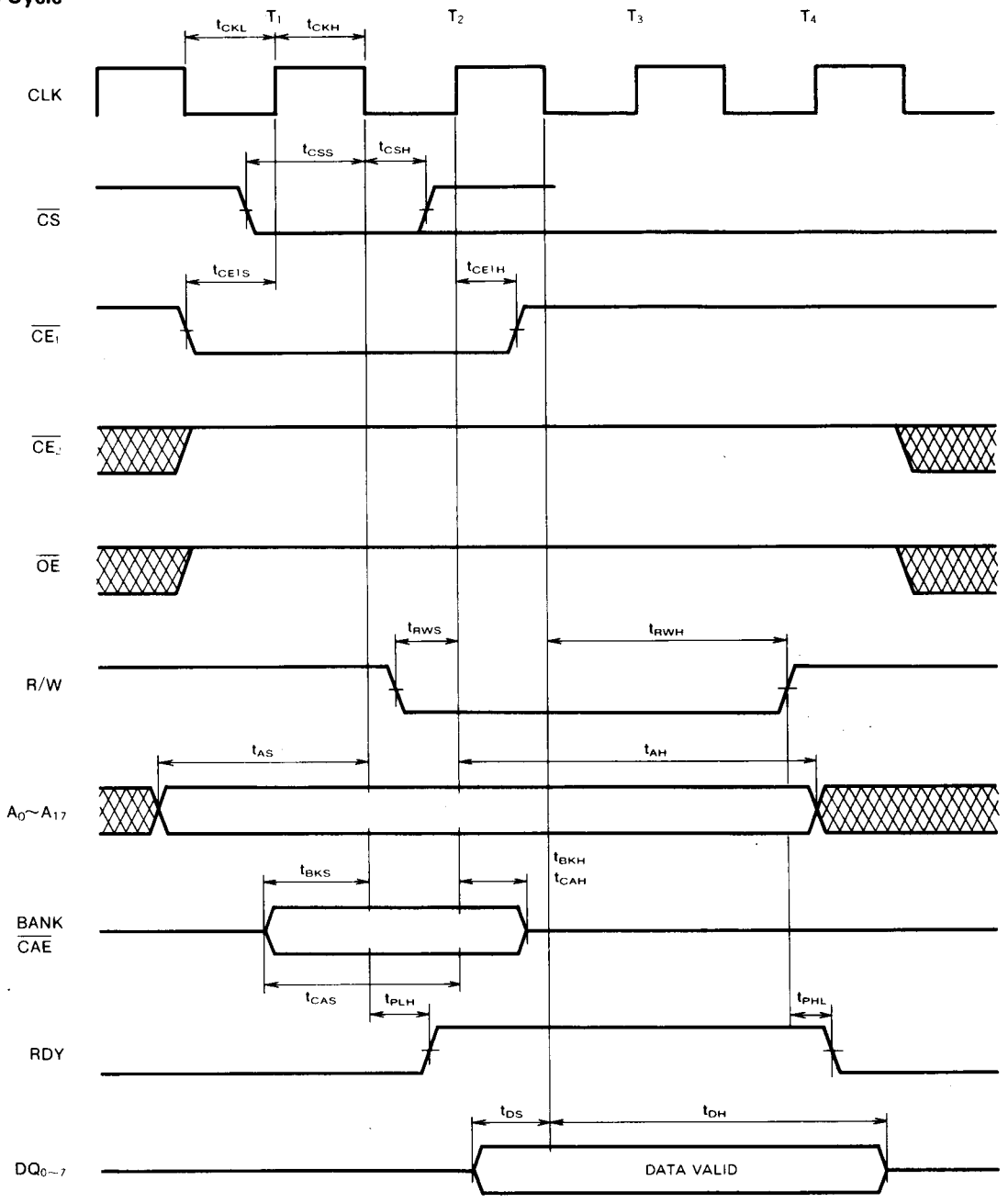
TIMING DIAGRAMS (Note 13)

Read Cycle



Note 13 Indicates the don't care input.

Write Cycle



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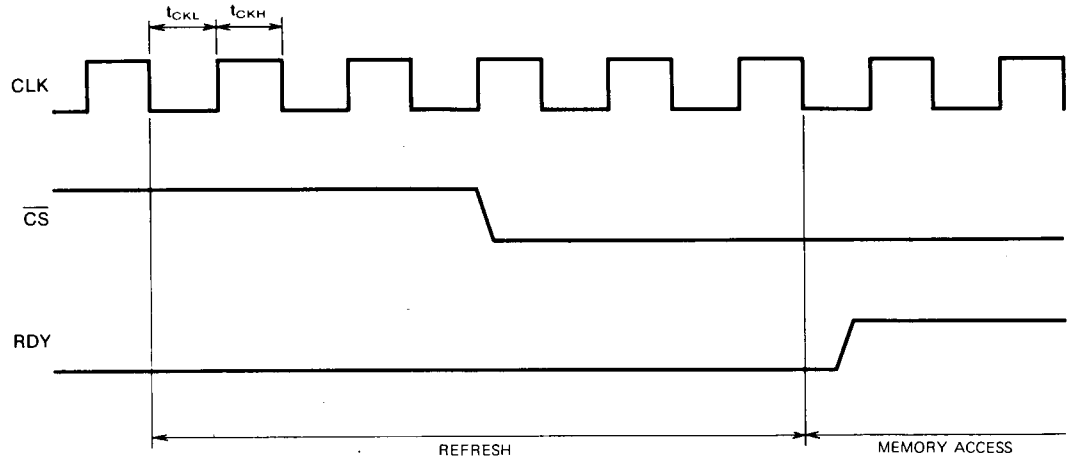
Refresh Cycle (Note 14)



Note 14: While refresh cycle, other input signal are waiting condition.

Reset Cycle