Military 54LS166

8-Bit Parallel-In Shift Register (with Clear)

ELECTRICALLY TESTED PER:
MIL-M-38510/30609

The 54LS166A is an 8-Bit Shift Register. Designed with all inputs buffered, the drive requirements are lowered to one 54LS standard load. By utilizing input clamping diodes, switching transients are minimized and system design simplified.

The 'LS166A is a parallel-in or serial-in, serial out shift register and has a complexity of 77 equivalent gates with gated clock inputs, and an overriding clear input. The shift/load input establishes the parallel-in or serial-in mode. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. Synchronous loading occurs on the next clock pulse when this is low and the parallel data inputs are enabled. Serial data flow is inhibited during parallel loading. Clocking is done on the low-to-high level edge of the clock pulse via a two input positive NOR gate, which permits one input to be used as a clock enable or clock inhibit function. Clocking is inhibited when either of the clock inputs are held high, holding either input low enables the other clock input. This will allow the system clock to be free running and the register stopped on command with the other clock input. A change from low-to-high on the clock inhibit input should only be done when the clock input is high. A buffered direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

- Synchronous Load
- Direct Overriding Clear
- Parallel to Serial Conversion

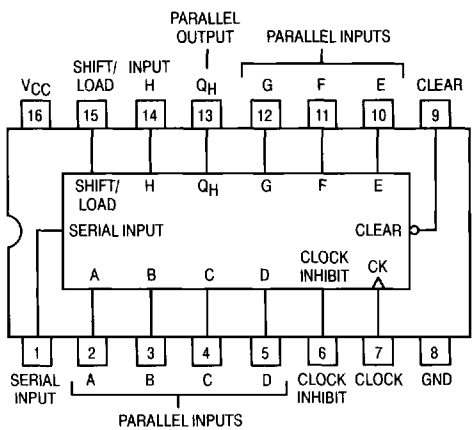
AVAILABLE AS:

1) JAN: JM38510/30609BXA
2) SMD: 8001701
3) 883: 54LS166/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

CONNECTION DIAGRAM



PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
SERIAL IN	1	1	2	GND
A	2	2	3	V_{CC}
B	3	3	4	V_{CC}
C	4	4	5	V_{CC}
D	5	5	7	V_{CC}
CLK INHIB	6	6	8	V_{CC}
CLK	7	7	9	V_{CC}
GND	8	8	10	GND
CLR	9	9	12	V_{CC}
E	10	10	13	V_{CC}
F	11	11	14	V_{CC}
G	12	12	15	V_{CC}
Q_H	13	13	17	OPEN
H	14	14	18	V_{CC}
SHF/LOAD	15	15	19	V_{CC}
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

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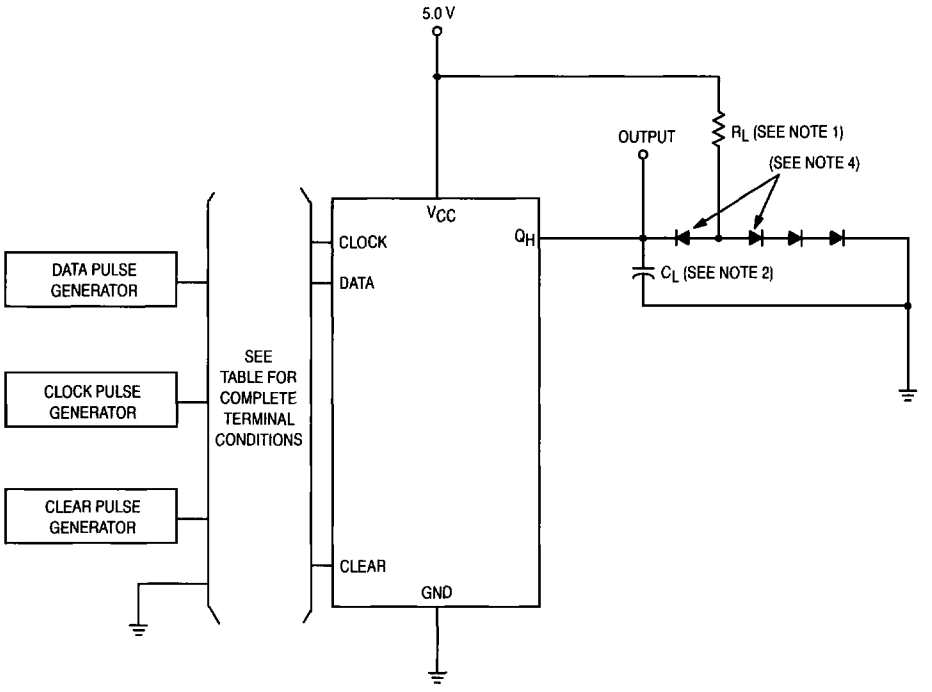
TEST CIRCUIT



REFERENCE NOTES ON PAGE 5-213

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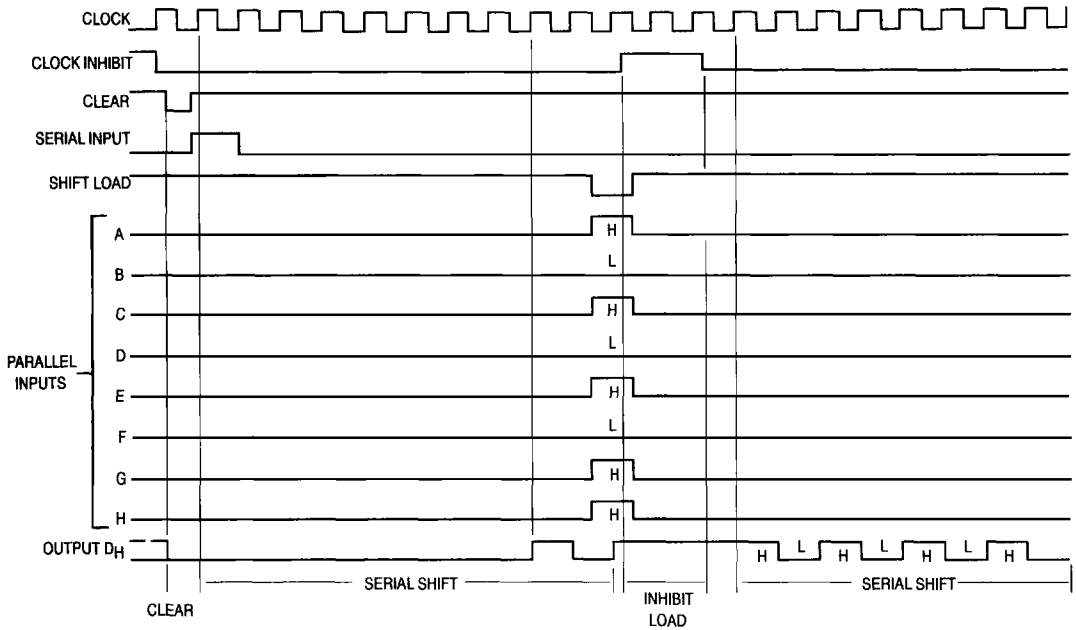
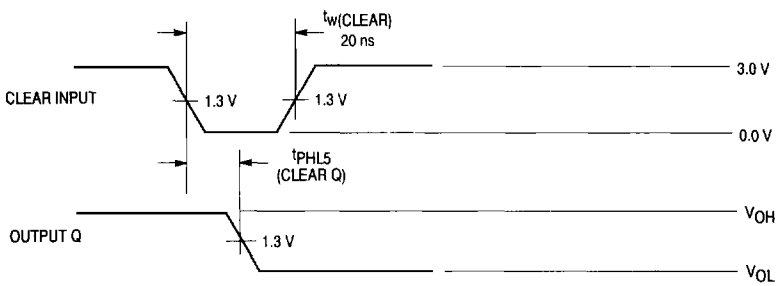
FUNCTION TABLE

Clear	Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A . . . . . H	Internal Outputs		Output Q_H
						Q_A	Q_B	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a . . . . . h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

SWITCHING WAVEFORMS

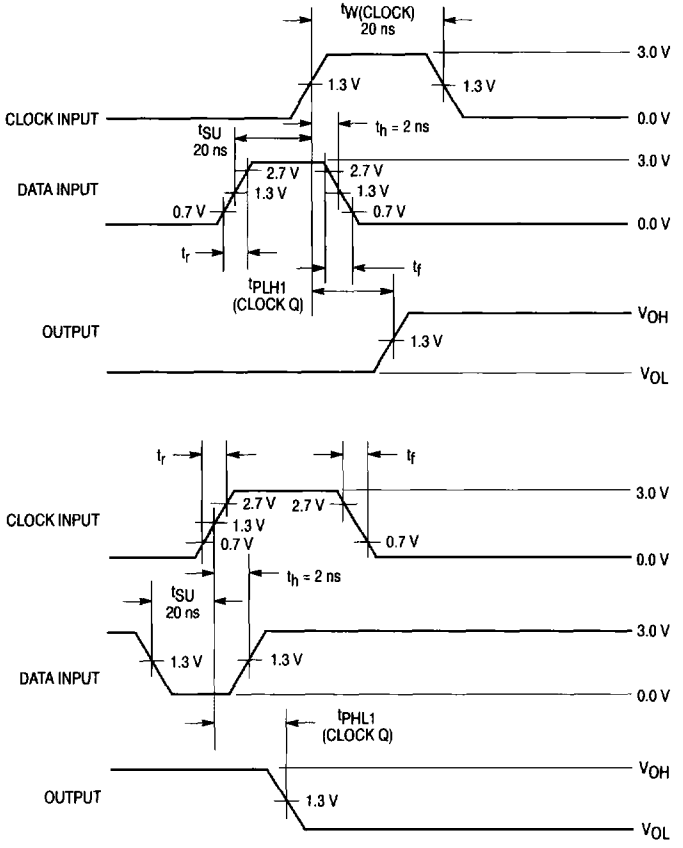
TYPICAL CLEAR, SHIFT, LOAD, INHIBIT, AND SHIFT SEQUENCES





NOTES:
1. R_L = 2.0 kΩ ± 5.0 %.
2. C_L = 50 pF ± 10%, which includes probe and jig capacitance.
3. All pulse generators have the following characteristics:
   Z_{OUT} = 50 Ω, t_f = 6.0 ns, t_r = 6.0 ns and PRR ≤ 1.0 MHz.
4. All diodes are 1N3064 or equivalent.

SWITCHING WAVEFORMS



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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −0.4 mA, V_{IH} = 2.0 V, CLR = open, CLK = (See Note 1), SHF/LD & $CLK_{INHIBIT}$ = 0.7 V.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IL} = 0.7 V, CLK = (See Note 1).
V_{IC}	Input Clamping Voltage		−1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V other inputs are open.
I_{IHH}	Logical "1" Input Current		0.1		0.1		0.1	mA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V other inputs are open.
I_{OS}	Output Short Circuit Current	−15	−100	−15	−100	−15	−100	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V, V_{OUT} = GND, CLK = (See Note 1), $CLK_{INHIBIT}$, QH & SHF/LD = GND.
I_{IL}	Logical "0" Input Current	−0.001	−0.15	−0.001	−0.15	−0.001	−0.15	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs are open, (CLK, $CLK_{INHIBIT}$ & CLR) are open.
$I_{IL(E-H)}$	Logical "0" Input Current	−0.1	−0.34	−0.1	−0.34	−0.1	−0.34	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs are open, SHF/LD = GND.
$I_{IL(SHF/LD)}$	Logical "0" Input Current	−0.001	−0.15	−0.001	−0.15	−0.001	−0.15	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs are open.
I_{CC}	Power Supply Current Off		38		38		38	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, all other inputs = GND, CLK = (See note 1).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

NOTES:

1. Apply ⌐‾‾‾‾ 2.5 V minimum/5.5 V maximum to clock Prior to test.
2. f_{MAX} minimum limit specified is the frequency of the clock input pulse. The output frequency shall be one-half of the input clock frequency. The input frequency on the "H" ↑ and ↓ are coincident with the clock ↓. Rise and fall times ≤ 6.0 ns. Input peak voltage 3.0 to 5.0 volts.
3. The limit specified for C_L = 15 pF are guaranteed but not tested.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay /Data-Output Clock to Output	5.0 —	35 35	5.0 —	46 44	5.0 —	46 44	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH1} t_{PLH1}	Propagation Delay /Data-Output Clock to Output	5.0 —	31 35	5.0 —	40 44	5.0 —	40 44	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL5} t_{PHL5}	Propagation Delay /Data-Output Clear to Output	5.0 —	40 30	5.0 —	52 38	5.0 —	52 38	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
f_{MAX}	Maximum Clock Frequency	25 25		22 –		22 –		MHz	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.