HN62444BN Series — Preliminary

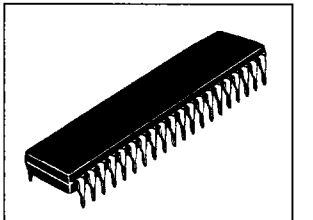
4M (256K x 16-bit) Mask ROM

■ DESCRIPTION

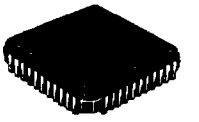
The Hitachi HN62444BN is a 4-Megabit CMOS Mask Programmable Read Only Memory organized as 262,144 x 16-bit.

The high density and high speed Nibble Access provide enough capacity and high performance to be used in a system using a high speed 16-bit or 32-bit microcomputer. In addition the low power consumption of this device makes it ideal for battery powered, portable systems.

Hitachi's HN62444B is offered with JEDEC-Standard pinouts in 40-pin Plastic DIP and 44-lead PLCC packages. The HN62444B is also packaged in a 44-lead Plastic SOP.



(DP-40)



(CP-44)

(FP-44D)

■ FEATURES

- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Normal Access Time:
  120 ns (max)
- Nibble Access Time:
  70 ns (max)
- Low Power Dissipation:
  Active Current: 150 mW (typ)
  Standby Current: 5 µW (typ)
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
  JEDEC Standard Word-Wide EPROM Pinout
- Packages:
  40-pin Plastic DIP
  44-lead PLCC
  44-lead Plastic SOP

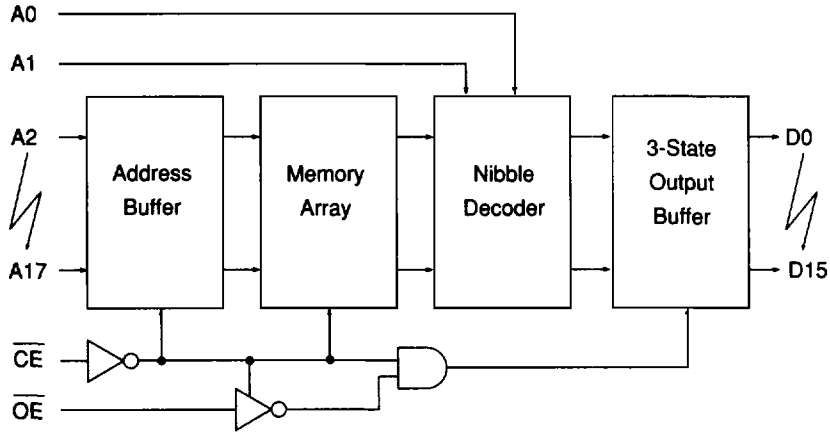
■ ORDERING INFORMATION

Type No.	Access Time	Package
HN62444BPN-12	120 ns	40-pin Plastic DIP (DP-40)
HN62444BCPN-12	120 ns	44-lead PLCC (CP-44)
HN62444BFBN-12	120 ns	44-lead Plastic SOP (FP-44D)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{17}	Address
D_0 - D_{15}	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



(BD.HN62444BN)

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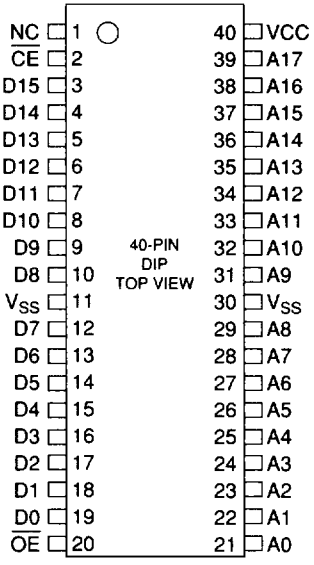
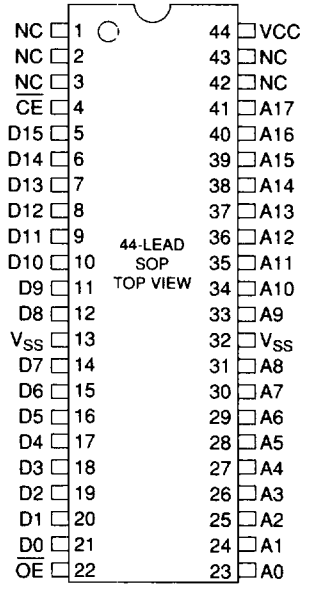
■ PIN ARRANGEMENT

HN62444BPN Series



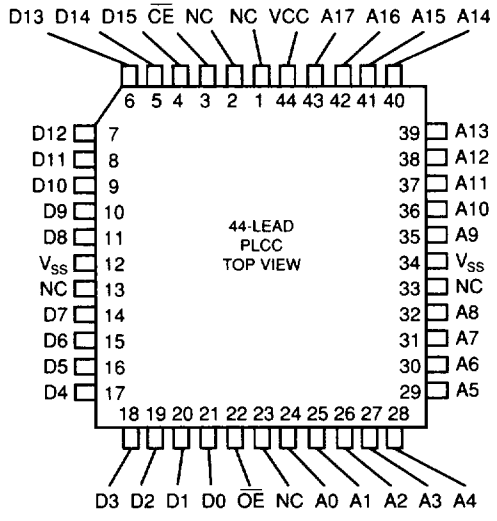
(PinD40.HN62444BN)

HN62444BFBN Series



(PinT244.HN62444BN)

HN62444BCPN Series



(PinQ44.HN62444BN)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage[1]	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage[1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Note: 1. Relative to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 5%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0V, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit
Input Capacitance	C_{IN}	-	-	15	pF
Output Capacitance	C_{OUT}	-	-	15	pF

Note: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 5%, V_{SS} = 0V, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	-	10	µA	$\overline{CE}$ = 2.4, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	-	120	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = min.
Standby V_{CC} Current	I_{SB1}	-	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{cc}$ to -0.2V
	I_{SB2}	-	-	3	mA	V_{CC} = 5.5 V, $\overline{CE} \geq$ 2.4V
Input Voltage	V_{IH}	2.4	-	V_{CC}+0.3	V	
	V_{IL}	-0.3	-	0.45	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.4	V	I_{OL} = 2.1 mA

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■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 5%, V_{SS} = 0V, T_a = 0 to 70°C)

Test Conditions

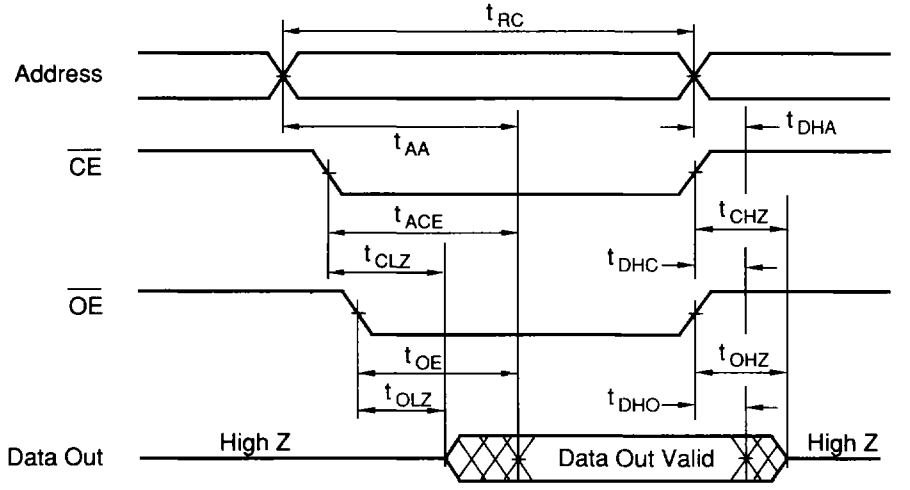
- Input pulse levels: 0.45 / 2.4V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

Item	Symbol	HN62444BN-12 Min.	HN62444BN-12 Max.	Test Unit
Read Cycle Time	t_{RC}	120	-	ns
Nibble Read Cycle Time	$+_{NC}$	70	-	ns
Address Access Time	t_{AA}	-	120	ns
Nibble Address Access Time	$+_{NA}$	-	70	ns
Chip Enable Access Time	t_{ACE}	-	120	ns
Output Enable Access Time	t_{OE}	-	55	ns
Output Hold Time from Address Change	t_{DHA}	0	-	ns
Output Hold Time from Chip Enable	t_{DHC}	0	-	ns
Output Hold Time from Output Enable	t_{DHO}	0	-	ns
Chip Enable to Output in High-Z [1]	t_{CHZ}	-	40	ns
Output Enable to Output in High-Z [1]	t_{OHZ}	-	40	ns
Chip Enable to Output in Low-Z	t_{CLZ}	5	-	ns
Output Enable to Output in Low-Z	t_{OLZ}	5	-	ns

Note: 1. t_{CHZ}, t_{OHZ}, are defined as the time at which the output becomes an open circuit and are not referred to output voltage levels.

■ READ TIMING WAVEFORM

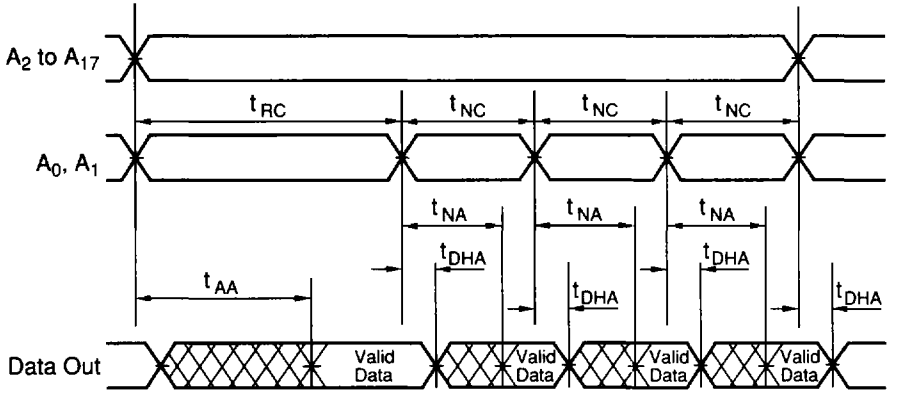
1) Normal Mode:



(TD.R.HN62444BN)

Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

2) Nibble Mode:



(TD.RN.HN62444BN)

Note: $\overline{CE}$ and $\overline{OE}$ are enabled.

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