

F10181 • F10581

4-BIT ALU/FUNCTION GENERATOR

F10K VOLTAGE COMPENSATED ECL

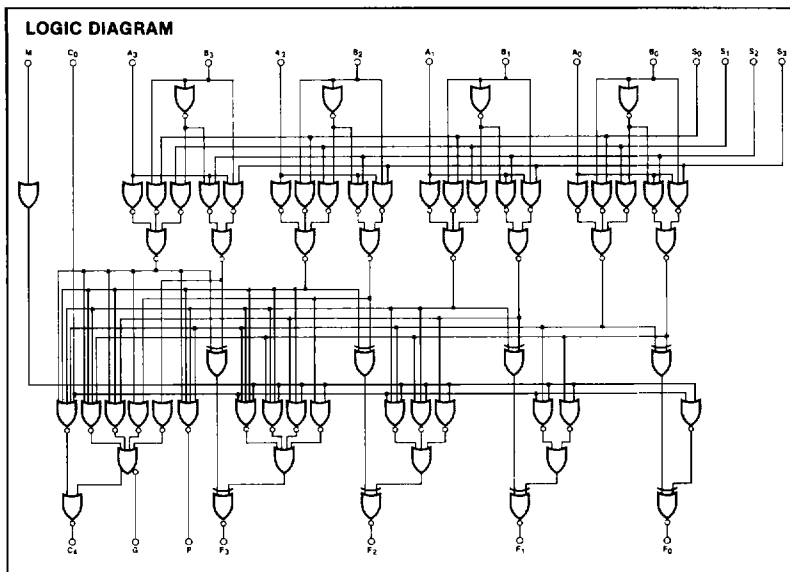
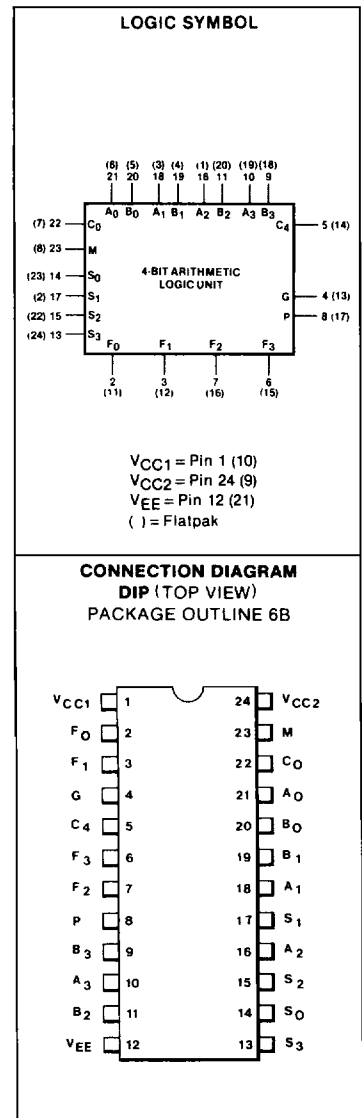
DESCRIPTION — The F10181 and F10581 are high-speed arithmetic logic units capable of performing 16 logic operations and 16 arithmetic operations on two 4-bit words. Full internal carry is incorporated for ripple through operation.

Arithmetic/logic operations are selected by applying the appropriate binary word to the select inputs (S_0 through S_3) as indicated in the tables of arithmetic/logic functions.

Group carry propagate (P) and carry generate (G) are provided to allow fast operations on very long words using a second order lookahead. The internal carry is enabled by applying a LOW level voltage to the Mode Control input (M).

When used with the F10179, full carry lookahead, as a second order lookahead block, the F10181 provides high speed arithmetic operations on very long words.

- VOLTAGE COMPENSATED—INSENSITIVE TO POWER SUPPLY VARIATIONS AND GRADIENTS
- OPEN EMITTER-FOLLOWER OUTPUTS
- SEPARATE V_{CC} PINS TO ELIMINATE NOISE COUPLING
- INTERNAL 50 k Ω (NOMINAL) INPUT PULL-DOWN RESISTORS—UNUSED INPUTS MAY BE LEFT OPEN



FAIRCHILD ECL • F10181 • F10581

PIN NAMES

A_n, B_n	Operand Inputs	M	Mode Control
F_n	Function Outputs	C_4	Carry Out
S_n	Select Inputs	G	Carry Generate
C_0	Carry In	P	Carry Propagate

LOGIC FUNCTIONS

FUNCTION SELECT				OUTPUT FUNCTION F		
				M = HIGH (Logic Mode)	M = LOW (Arithmetic Mode)	
S_3	S_2	S_1	S_0	$C_0 = H \text{ or } L$	$C_0 = \text{LOW}$	$C_0 = \text{HIGH}$
L	L	L	L	\bar{A}	A	A plus 1
L	L	L	H	$\bar{A} + \bar{B}$	A plus $\bar{A}\bar{B}$	A plus $\bar{A}\bar{B}$ plus 1
L	L	H	L	$\bar{A} + B$	A plus AB	A plus AB plus 1
L	L	H	H	HIGH	A plus A (2 times A)	A plus A plus 1
L	H	L	L	$\bar{A}\bar{B}$	A + B	(A + B) plus 1
L	H	L	H	\bar{B}	(A + B) plus $\bar{A}\bar{B}$	(A + B) plus $\bar{A}\bar{B}$ plus 1
L	H	H	L	$\bar{A}\oplus\bar{B}$	A plus B	A plus B plus 1
L	H	H	H	$A + \bar{B}$	(A + B) plus A	(A + B) plus A plus 1
H	L	L	L	$\bar{A}\bar{B}$	$A + \bar{B}$	(A + \bar{B}) plus 1
H	L	L	H	$A\oplus B$	A minus B minus 1	A minus B
H	L	H	L	B	(A + \bar{B}) plus AB	(A + \bar{B}) plus AB plus 1
H	L	H	H	A + B	(A + \bar{B}) plus A	(A + \bar{B}) plus A plus 1
H	H	L	L	LOW	minus 1 (2's complement)	Zero
H	H	L	H	$\bar{A}\bar{B}$	$\bar{A}\bar{B}$ minus 1	$\bar{A}\bar{B}$
H	H	H	L	AB	AB minus 1	AB
H	H	H	H	A	A minus 1	A

DC CHARACTERISTICS: $V_{EE} = -5.2 \text{ V}$, $V_{CC} = \text{GND}$

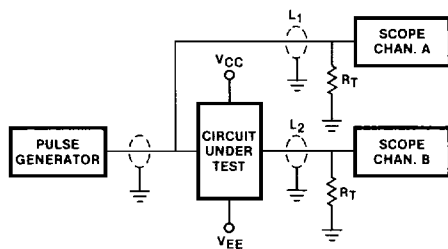
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS
		B	TYP	A			
I_{IH}	Input Current HIGH Pin M Pins A3, A2, A1, A0 Pins B3, B2, B1, B0 Pins S3, S2, S1, S0 Pin C0			200 220 245 265 290	μA	25°C	$V_{IN} = V_{IHA}$
I_{EE}	Power Supply Current	-145	-110		mA	25°C	Inputs Open

AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$

SYMBOL	CHARACTERISTIC	OUTPUT	LIMITS			UNITS	CONDITIONS See Figure 1
			B	TYP	A		
t_{PHL}, t_{PLH} t_{THL}, t_{TLH}	Propagation Delay, C – C ₄ Transition Time, C ₄	1 1	1.1 1.0	3.1 2.0	5.0 3.0	ns ns	A ₀ , A ₁ , A ₂ , A ₃ = +1.11 V Other Inputs = +0.31 V
t_{PHL}, t_{PLH} t_{THL}, t_{TLH}	Propagation Delay, C – F ₁ Transition Time, F ₁	1 1	2.0 1.5	4.5 3.0	7.0 5.0	ns ns	A ₀ = +1.11 V Other Inputs = +0.31 V
t_{PHL}, t_{PLH} t_{THL}, t_{TLH}	Propagation Delay, A ₁ – F ₁ Transition Time, F ₁	1 1	3.0 1.5	6.5 3.0	10.0 5.0	ns ns	All Inputs = +0.31 V
t_{PHL}, t_{PLH} t_{THL}, t_{TLH}	Propagation Delay, A ₁ – P Transition Time, P	1 1	2.0 1.1	5.0 2.0	6.5 3.5	ns ns	S ₀ , S ₃ = +1.11 V Other Inputs = +0.31 V
t_{PHL}, t_{PLH} t_{THL}, t_{TLH}	Propagation Delay, A ₁ – G Transition Time, G	1 1	2.0 1.5	4.5 4.0	7.0 5.0	ns ns	A ₀ , A ₂ , A ₃ , C = +1.11 V Other Inputs = +0.31 V
t_{PHL}, t_{PLH} t_{THL}, t_{TLH}	Propagation Delay, A ₁ – C ₄ Transition Time, C ₄	1 1	2.0 1.0	5.0 2.0	7.0 3.0	ns ns	A ₀ , A ₂ , A ₃ , C = +1.11 V Other Inputs = +0.31 V
t_{PHL}, t_{PLH} t_{THL}, t_{TLH}	Propagation Delay, B ₁ – F ₁ Transition Time, F ₁	1 1	3.0 1.5	8.0 3.5	11.0 5.0	ns ns	S ₃ , C = +1.11 V Other Inputs = +0.31 V
t_{PHL}, t_{PLH} t_{THL}, t_{TLH}	Propagation Delay, B ₁ – P Transition Time, P	1 1	2.0 1.1	6.0 2.0	7.5 3.5	ns ns	S ₁ , A ₁ = +1.11 V Other Inputs = +0.31 V
t_{PHL}, t_{PLH} t_{THL}, t_{TLH}	Propagation Delay, B ₁ – G Transition Time, G	2 2	2.0 1.5	6.0 3.0	8.0 5.0	ns ns	S ₃ , C = +1.11 V Other Inputs = +0.31 V
t_{PHL}, t_{PLH} t_{THL}, t_{TLH}	Propagation Delay, B ₁ – C ₄ Transition Time, C ₄	2 2	2.0 1.0	6.0 2.0	8.0 3.0	ns ns	S ₃ , C = +1.11 V Other Inputs = +0.31 V
t_{PHL}, t_{PLH} t_{THL}, t_{TLH}	Propagation Delay, M – F ₁ Transition Time, F ₁	1 1	3.0 1.5	6.5 4.0	10.0 5.0	ns ns	All Inputs = +0.31 V
t_{PHL}, t_{PLH} t_{THL}, t_{TLH}	Propagation Delay, S ₁ – F ₁ Transition Time, F ₁	2 2	3.0 1.5	6.5 3.0	10.0 5.0	ns ns	A ₁ , B ₁ = +1.11 V Other Inputs = +0.31 V
t_{PHL}, t_{PLH} t_{THL}, t_{TLH}	Propagation Delay, S ₁ – P Transition Time, P	1 1	2.0 1.1	6.0 3.0	8.0 5.0	ns ns	A ₃ , B ₃ = +1.11 V Other Inputs = +0.31 V
t_{PHL}, t_{PLH} t_{THL}, t_{TLH}	Propagation Delay, S ₁ – C ₄ Transition Time, C ₄	1 1	2.0 1.1	6.0 3.0	9.0 5.0	ns ns	A ₃ , B ₃ = +1.11 V Other Inputs = +0.31 V
t_{PHL}, t_{PLH} t_{THL}, t_{TLH}	Propagation Delay, S ₁ – G Transition Time, G	1 1	2.0 0.8	6.0 3.0	9.0 6.0	ns ns	A ₃ , B ₃ = +1.11 V Other Inputs = +0.31 V



AC TEST CIRCUIT AND WAVEFORMS



$V_{CC} = +2\text{ V}$, $V_{EE} = -3.2\text{ V}$
 $R_T = 50\ \Omega$ termination of scope
 $L_1 = L_2 = 50\ \Omega$ transmission lines
 Decoupling $0.1\ \mu\text{F}$ from V_{CC} and V_{EE} to gnd

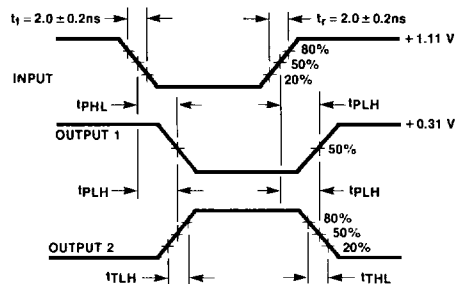


Fig. 1