

# SN54LS396, SN74LS396 OCTAL STORAGE REGISTERS

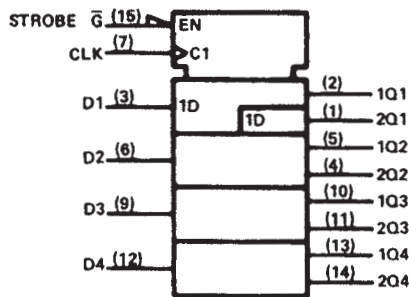
SDLS173 – MARCH 1977 – REVISED MARCH 1988

- Parallel Access
- Typical Propagation Delay Time . . . 20 ns
- Typical Power Dissipation . . . 120 mW
- Applications:  
N-Bit Storage Files  
Hex/BCD Serial-To-Parallel Converters

## description

These octal registers are organized as two 4-bit bytes of storage. Upon application of a positive-going clock signal, the information stored in byte 1 is transferred into byte 2 as a new 4-bit byte is loaded into the byte 1 location via the four data lines. The full 8-bit word is available at the outputs after two clock cycles. Both the clock and the strobe lines are fully buffered.

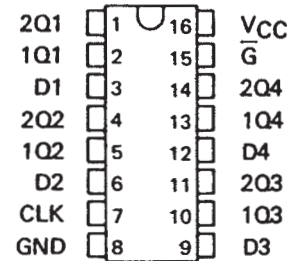
## logic symbol†



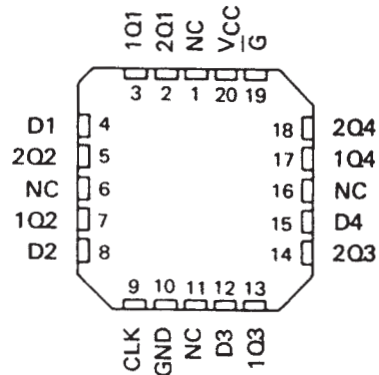
†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

SN54LS396 . . . J OR W PACKAGE  
SN74LS396 . . . D OR N PACKAGE  
(TOP VIEW)



SN54LS396 . . . FK PACKAGE  
(TOP VIEW)



NC - No internal connection

FUNCTION TABLE

INPUTS		OUTPUTS											
STROBE $\bar{G}$	CLOCK	DATA				BYTE 1				BYTE 2			
		D1	D2	D3	D4	1Q1	1Q2	1Q3	1Q4	2Q1	2Q2	2Q3	2Q4
H	X	X	X	X	X	L	L	L	L	L	L	L	L
L	↑	a	b	c	d	a	b	c	d	1Q1 <sub>n</sub>	1Q2 <sub>n</sub>	1Q3 <sub>n</sub>	1Q4 <sub>n</sub>

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)

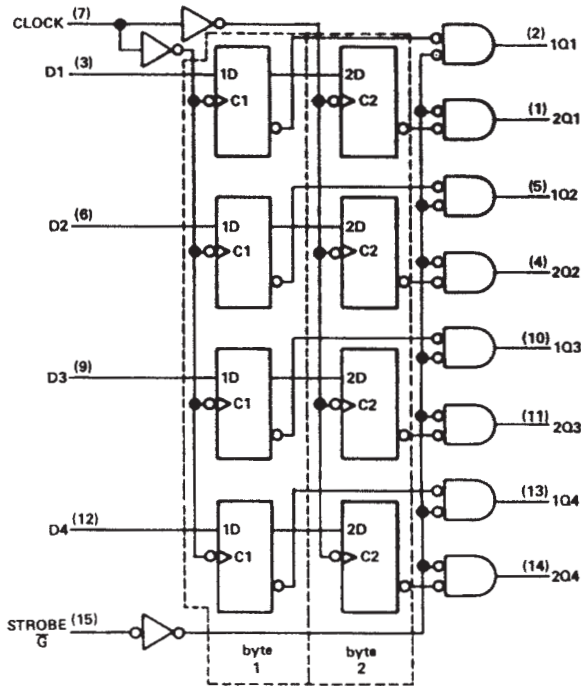
↑ = transition from low to high level

1Q1<sub>n</sub>, 1Q2<sub>n</sub>, 1Q3<sub>n</sub>, 1Q4<sub>n</sub> = the level of 1Q1, 1Q2, 1Q3, and 1Q4, respectively, before the most recent ↑ transition of the clock.

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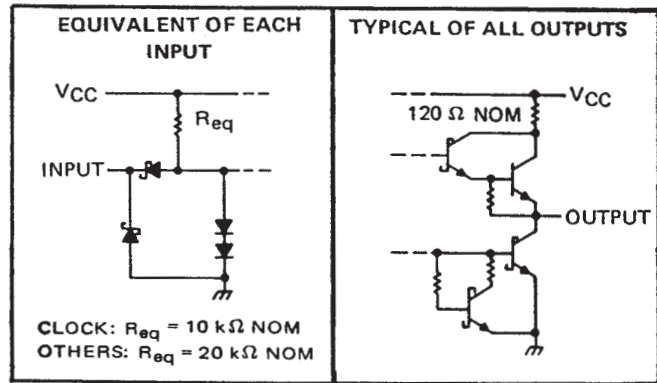
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## logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

## schematics of inputs and outputs



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS396	-55°C to 125°C
SN74LS396	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

	SN54LS396			SN74LS396			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-400			-400	$\mu A$
Low-level output current, $I_{OL}$			4			8	mA
Clock frequency, $f_{clock}$	0		30	0		30	MHz
Width of clock pulse, $t_w$	20			20			ns
Setup time, $t_{su}$	20			20			ns
Hold time, $t_h$	5			5			ns
Operating free-air temperature, $T_A$	-55		125	0		70	°C

# SN54LS396, SN74LS396 OCTAL STORAGE REGISTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS396			SN74LS396			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IH</sub>	High-level input voltage		2			2			V
V <sub>IL</sub>	Low-level input voltage		0.7			0.8			V
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA	-1.5			-1.5			V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX, I <sub>OH</sub> = -400 μA	2.5	3.4		2.7	3.4		V
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, I <sub>OL</sub> = 4 mA	0.25	0.4		0.25	0.4		V
		V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX, I <sub>OL</sub> = 8 mA				0.35	0.5		
I <sub>I</sub>	Input current at maximum input voltage	Clock input	0.2			0.2			mA
		Other inputs	0.1			0.1			
I <sub>IH</sub>	High-level input current	Clock input	40			40			μA
		Other inputs	20			20			
I <sub>IL</sub>	Low-level input current	Clock input	-0.8			-0.8			mA
		Other inputs	-0.4			-0.4			
I <sub>OS</sub>	Short-circuit output current§	V <sub>CC</sub> = MAX	-20	-100		-20	-100		mA
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = MAX, See Note 2	24	40		24	40		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTE 2: I<sub>CC</sub> is measured with 4.5 V applied to all inputs and all outputs open.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low-to-high-level output from clock	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ, See Note 3		20	30	ns
t <sub>PHL</sub>	Propagation delay time, high-to-low-level output from clock			20	30	
t <sub>PLH</sub>	Propagation delay time, low-to-high-level output from strobe			20	30	ns
t <sub>PHL</sub>	Propagation delay time, high-to-low-level output from strobe			20	30	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
5962-9050301EA	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	Samples Not Available
SN54LS396J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	Samples Not Available
SN54LS396J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	Samples Not Available
SN74LS396DR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	Samples Not Available
SN74LS396DR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	Samples Not Available
SN74LS396N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	Samples Not Available
SN74LS396N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	Samples Not Available
SNJ54LS396J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	Samples Not Available
SNJ54LS396J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	Samples Not Available

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF SN54LS396, SN74LS396 :**

- Catalog: [SN74LS396](#)
- Military: [SN54LS396](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

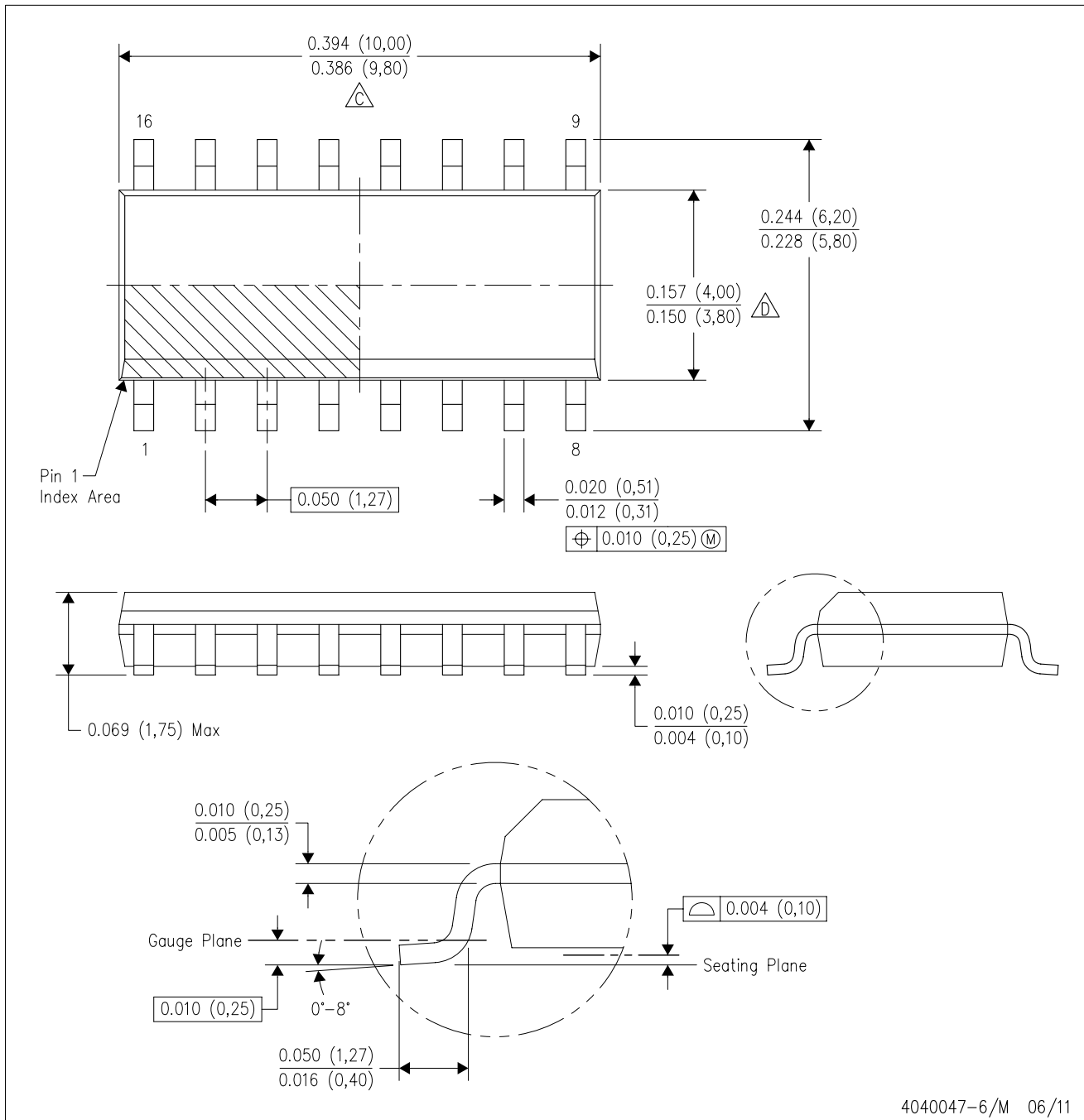


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

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