4096

4096×1 DYNAMIC RANDOM ACCESS MEMORY

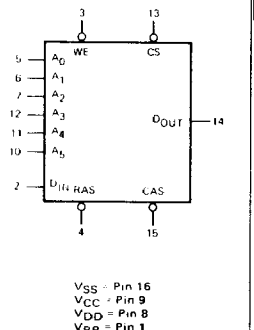
GENERAL DESCRIPTION – The 4096DC is a 4096-bit dynamic Random Access Memory organized as 4096 one-bit words. This device is designed utilizing the single transistor dynamic memory cell.

A unique address multiplexing and latching technique permits the packaging of the 4096DC in a standard 16-pin ceramic Dual In-line Package. The use of this package allows construction of highly dense memory systems utilizing widely available automated testing and insertion equipment.

The 4096DC features direct TTL compatibility, on-chip address, data input and data output latches, TTL-level clocks with extremely low capacitance and a range of access times from 200 ns (4096-2DC) to 350 ns (4096-5DC). The 4096DC is manufactured using the n-channel Isoplanar process.

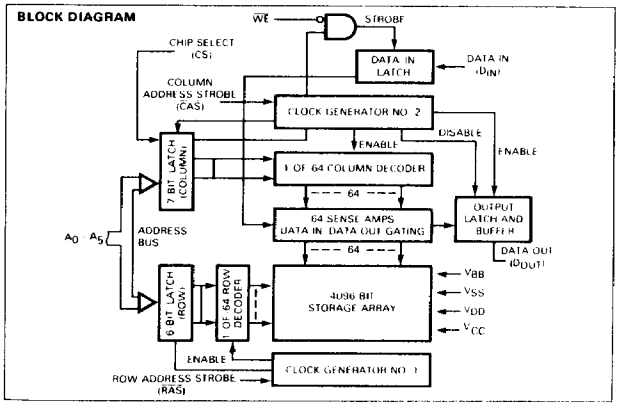
- **ALL INPUTS TTL-COMPATIBLE, INCLUDING CLOCKS**
- **ON-CHIP LATCHES FOR ADDRESSES, CHIP SELECT, DATA INPUT**
- **THREE-STATE TTL-COMPATIBLE OUTPUT**
- **CHIP SELECT DECODING DOES NOT ADD TO ACCESS TIME**
- **READ OR WRITE CYCLES: 4096-2: 300 ns, 4096-3: 360 ns, 4096-4: 420 ns, 4096-5: 500 ns**
- **ACTIVE POWER: 4096-2: <431 mW, 4096-3: <378 mW, 4096-4: <341 mW, 4096-5: <315 mW**
- **STANDBY POWER: <25 mW**
- **STANDARD 16-PIN CERAMIC PACKAGE**

LOGIC SYMBOL

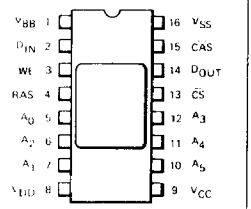


V_{SS} = Pin 16
V_{CC} = Pin 9
V_{DD} = Pin 8
V_{BB} = Pin 1

BLOCK DIAGRAM



CONNECTION DIAGRAM DIP (TOP VIEW)



PIN NAMES

An	Address Inputs	D_{OUT}	Data Output	
D_{IN}	Data Input	V_{CC}	+5 V	Power Supply
$\overline{CS}$	Chip Select Input	V_{SS}	0 V	Power Supply
$\overline{WE}$	Write Enable Input	V_{BB}	-5 V	Power Supply
$\overline{RAS}$	Row Address Strobe (Clock) Input	V_{DD}	+12 V	Power Supply
$\overline{CAS}$	Column Address Strobe (Clock) Input			

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage of any pin relative to V_{BB}	-0.5 V to +25.0 V
Operating Temperature	0°C to 70°C
Storage Temperature (Ambient)	-55°C to 150°C

ADDRESSING – The 12 address bits required to decode 1 of 4096 cell locations are multiplexed onto the 6 address pins and latched into the on-chip row and column address latches. The Row Address Strobe ($\overline{RAS}$) latches the 6 row address bits onto the chip. The Column Address Strobe ($\overline{CAS}$) latches the 6 column address bits plus Chip Select ($\overline{CS}$) onto the chip. Since the Chip Select signal is not required until well into the cycle, its decoding time does not add to the system access or cycle time.

DATA INPUT/OUTPUT – Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WE}$ and $\overline{CAS}$. The last of these signals making its negative transition is the strobe for the Data In register. This permits several options in the write timing. In a write cycle, if the $\overline{WE}$ input is activated prior to $\overline{CAS}$, the Data In is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to this signal. If the cycle is to be a read-write cycle or read-modify-write cycle, then the $\overline{WE}$ input will not go to a logic 0 until after the access time has elapsed. But now, because $\overline{CAS}$ is ready at a logic 0, the Data In is strobed in by $\overline{WE}$ and the set-up hold times are referenced to $\overline{WE}$.

At the beginning of a memory cycle the state of the Data Out Latch and buffer depend on the previous memory cycle. If during the previous cycle the chip was unselected, the output buffer will be in its open-circuit condition. If the previous cycle was a read, read-write, or read-modify-write cycle and the chip was selected, then the output latch and buffer will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the previous cycle was a write cycle ($\overline{WE}$ active low before access time) and the chip was selected, then the output latch and buffer will contain a logic 1. Regardless of the state of the output it will remain valid until $\overline{CAS}$ goes negative. At that time the output will unconditionally go to its open-circuit state. It will remain open circuit until after an access time has elapsed. At access time the output will assume the proper state for the type of cycle performed. If the chip is unselected, it will not accept a WRITE command and the output will remain in the open-circuit state.

INPUT/OUTPUT LEVELS – All inputs, including the two address strobes, will interface directly with TTL. The high impedance, low capacitance input characteristics simplify input driver selection by allowing use of standard logic elements rather than specially designed driver elements. Even though the inputs may be driven directly by TTL gates, pull-up or termination resistors are normally required in a system to prevent ringing of the input signals due to line inductance and reflections. In high speed memory systems, transmission line techniques must be employed on the signal lines to achieve optimum system speeds. Series rather than parallel terminations may be employed at some degradation of system speed.

The three-state output buffer is a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The resistance to V_{CC} is 500 ohms maximum and 150 ohms typically. The resistance to V_{SS} is 200 ohms maximum and 100 ohms typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which chips are interfaced. During battery standby operation, the V_{CC} pin may be unpowered without affecting the 4096 refresh operation. This allows all system logic except the $\overline{RAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

REFRESH – Refresh of the cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses every 2 milliseconds or less. Any read cycle refreshes the selected row, regardless of the state of the Chip Select. A write, read-write, or read-modify-write cycle also refreshes the selected row but the chip should be unselected to prevent writing data into the selected cell.

POWER DISSIPATION/STANDBY MODE – Most of the circuitry used in the 4096 is dynamic and draws power only as the result of an address strobe edge. Because the power is not drawn during the whole time the strobe is active, the dynamic power is a function of operating frequency. Typically, the power is 120mW at a 1 μS cycle time for the 4096DC with a worst case power of less than 341 mW at a 420 ns cycle time. To reduce the overall system power the Row Address Strobe ($\overline{RAS}$) must be decoded and supplied to only the selected chips. The $\overline{CAS}$ must be supplied to all chips (to turn off the unselected outputs). But those chips that did not receive a $\overline{RAS}$ will not dissipate any power on the $\overline{CAS}$ edges, except for that required to turn off the output. If the $\overline{RAS}$ is decoded and supplied to the selected chips, then the Chip Select input of all chips can be at a logic 0. The chips that receive a $\overline{CAS}$ but no $\overline{RAS}$ will be unselected (output open-circuited) regardless of the Chip Select input.

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	11.4	12.0	12.6	V	2
V_{CC}	Supply Voltage	4.5	5.0	V_{DD}	V	2
V_{SS}	Supply Voltage	0	0	0	V	2,12
V_{BB}	Supply Voltage	−5.5	5.0	4.5	V	2
V_{IH1}	Input HIGH Voltage Address Input	2.4	5.0	V_{GG}	V	2,14
V_{IL}	Input LOW Voltage, All Inputs	−1.0	0	0.6	V	2,14
V_{IH2}	Input HIGH Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{CS}$, $\overline{WE}$	2.7	5.0	V_{GG}	V	2,14

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) (V_{DD} = 12.0 V ± 5%, V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, V_{BB} = −5.0 V ± 10%)

SYMBOL	PARAMETER	PART NUMBER 4096-2 MIN	4096-2 MAX	4096-3 MIN	4096-3 MAX	4096-4 MIN	4096-4 MAX	4096-5 MIN	4096-5 MAX	UNITS	NOTES
I_{DD1}	Average V_{DD} Power Supply Current		35		30		27		25	mA	16
I_{CC}	V_{CC} Power Supply Current									mA	9
I_{BB}	Average V_{BB} Power Supply Current		75		75		75		75	µA	
I_{DD2}	Standby V_{DD} Power Supply Current		2		2		2		2	mA	
I_{IN}	Input Leakage Current (Any Input)		10		10		10		10	µA	10
I_{OUT}	Output Leakage Current		10		10		10		10	µA	11
V_{OH}	Output HIGH Voltage at I_{OUT} = −5 mA	2.4		2.4		2.4		2.4		V	
V_{OL}	Output LOW Voltage at I_{OUT} = 2 mA		0.4		0.4		0.4		0.4	V	
C_{IN1}	Input Capacitance (A_0 – A_5)		10		10		10		10	pF	
C_{IN2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, D_{IN}, $\overline{WE}$, $\overline{CS}$)		7		7		7		7	pF	
C_{OUT}	Output Capacitance (D_{OUT})		8		8		8		8	pF	

RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) (V_{DD} = 12.0 V ± 5%, V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, V_{BB} = −5.0 V ± 10%) (Note 17)

SYMBOL	PARAMETER	PART NUMBER 4096-2 MIN	4096-2 MAX	4096-3 MIN	4096-3 MAX	4096-4 MIN	4096-4 MAX	4096-5 MIN	4096-5 MAX	UNITS	NOTES
t_{RC}	Random Read or Write Cycle Time	300		365		425		500		ns	3
t_{RAC}	Access Time from ROW Address Strobe		200		250		300		350	ns	3, 15
t_{CAC}	Access Time from Column Address Strobe		120		150		175		200	ns	4
t_{OFF}	Output Buffer Turn-Off Delay	0	70	0	80	0	90	0	100	ns	4
t_{RP}	ROW Address Strobe Precharge Time	100		115		125		150		ns	
t_{RCL}	ROW to Column Strobe Lead Time	80		100		125		150		ns	3
t_{CPW}	Column Address Strobe Pulse Width	120		150		175		200		ns	
t_{AS}	Address Set-Up Time	0		0		0		0		ns	3, 4
t_{AH}	Address Hold Time	50		60		70		80		ns	3, 4
t_{CH}	Chip Select Hold Time	70		80		90		100		ns	
t_{RCS}	Read Command Set-Up Time	0		0		0		0		ns	4
t_{RCH}	Read Command Hold Time	30		35		40		45		ns	5
t_{WCH}	Write Command Hold Time	90		110		140		150		ns	4, 6
t_{WP}	Write Command Pulse Width	120		150		175		200		ns	
t_{CRL}	Column to ROW Strobe Lead Time	20		20		20		20		ns	7
t_{CWL}	Write Command to Column Strobe Lead Time	120		150		175		200		ns	13
t_{DS}	Data In Set-Up Time	0		0		0		0		ns	13
t_{DH}	Data In Hold Time	90		110		130		150		ns	13
t_{RFSH}	Refresh Period		2		2		2		2	ms	
t_{MOD}	Modify Time		10		10		10		10	µs	8

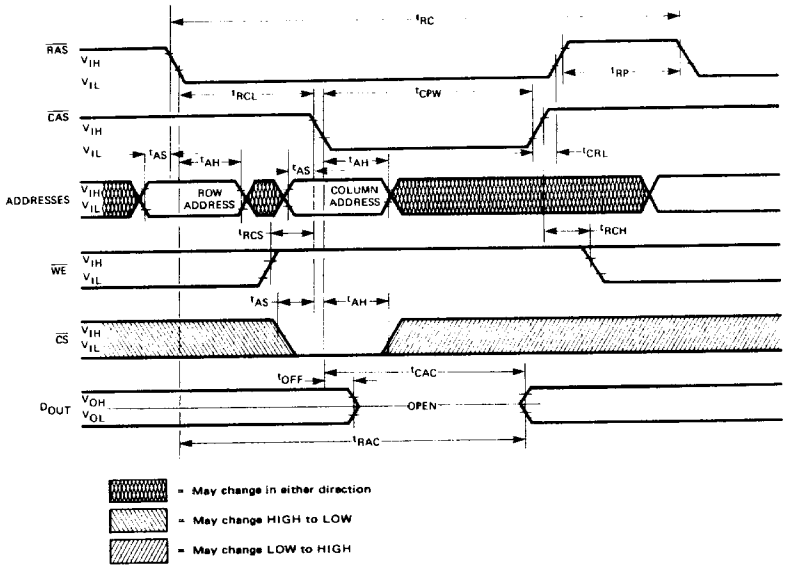
Notes on following page.

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages referenced to V_{SS}.
3. Referenced to $\overline{RAS}$ leading edge.
4. Referenced to $\overline{CAS}$ leading edge.
5. Referenced to $\overline{CAS}$ trailing edge.
6. Write Command Hold Time is important only when performing normal random write cycles. During read-write or read-modify-write cycles, the Write Command Pulse Width is the limiting parameter.
7. Referenced to the $\overline{RAS}$ trailing edge.
8. Referenced to access time.
9. Depends upon output loading. The V_{CC} supply is connected only to the output buffer.
10. All device pins at 0 volts except V_{BB} at −5 volts and pin under test which is at +10 volts.
11. Output disabled by chip select input.
12. Output voltage will swing from V_{SS} to V_{CC} independent of differential between V_{SS} and V_{CC}.
13. These parameters are referenced to the $\overline{CAS}$ leading edge in random write cycle operation and to the $\overline{WE}$ leading edge in read-write or read-modify-write cycles.
14. Input voltages greater than TTL levels (0 to 5 V) require device operation at reduced speed.
15. Assumes t_{RCL} minimum.
16. Current is proportional to speed with maximum current measured at fastest cycle rate.
17. AC measurements assume ≈10 ns rise and fall times.

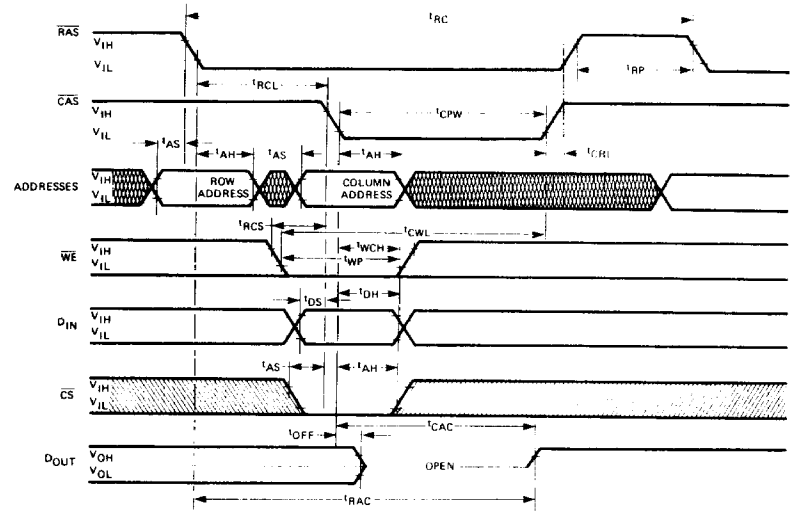
TIMING DIAGRAMS

READ CYCLE

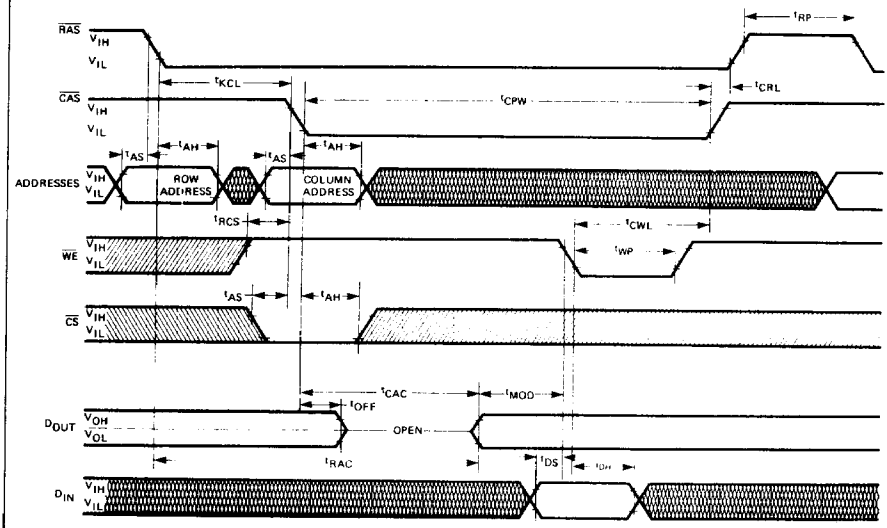


TIMING DIAGRAMS (Cont'd)

WRITE CYCLE



READ-MODIFY-WRITE CYCLE*



*Read-modify-write cycle time = $t_{RCL} + t_{CAC} + t_{MOD} + t_{CWL} + t_{CRL} + t_{RP} + 3\,t_f + t_r$.