

74AC/ACT11269

Synchronous Presettable 8-Bit Binary Up/Down Counter

Objective Specification

ACL Products

FEATURES

- Synchronous counting and loading
- Up/Down counting
- Two Count Enable Inputs for n-bit cascading
- Positive edge-triggered Clock
- Glitchless Terminal Count output
- Built-in look-ahead carry capability
- Presettable for programmable operation
- Output capability: $\pm 24\text{mA}$
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11269 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The AC/ACT11269 is a synchronous, presettable 8-bit up/down binary counter featuring an internal Carry look-ahead for

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS $T_A = 25^\circ\text{C}; \text{GND} = 0\text{V};$ $V_{CC} = 5.0\text{V}$	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay CP to Q_n ($\overline{PE} = \text{High}$)	$C_L = 50\text{pF}$	5.7	7.4	ns
C_{PD}	Power dissipation capacitance ¹	$f = 1\text{MHz}; C_L = 50\text{pF}$	215	200	pF
C_{IN}	Input capacitance	$V_i = 0\text{V}$ or V_{CC}	4.5	4.5	pF
I_{LATCH}	Latch-up current	Per Jeduc JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	$C_L = 50\text{pF}$	160	150	MHz

Note:

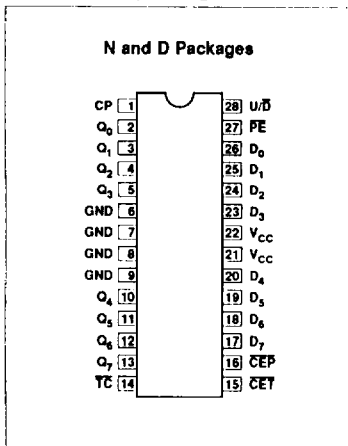
- C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:
 f_i = input frequency in MHz, C_L = output load capacitance in pF,
 f_o = output frequency in MHz, V_{CC} = supply voltage in V,
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

ORDERING INFORMATION

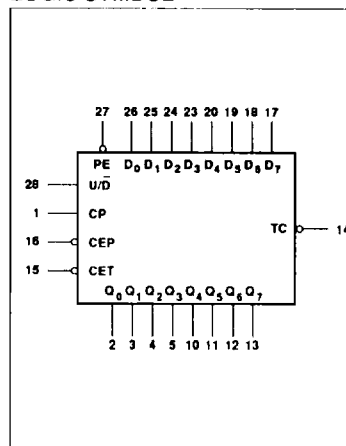
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11269N 74ACT11269N
28-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11269D 74ACT11269D

PIN CONFIGURATION



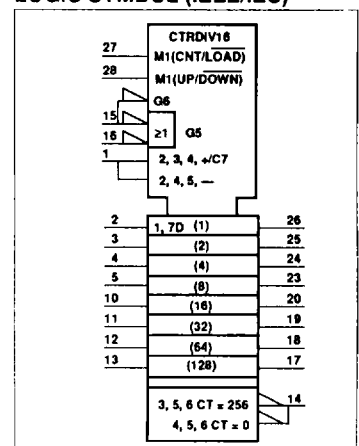
June 22, 1989

LOGIC SYMBOL



5-330

LOGIC SYMBOL (IEEE/IEC)



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applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the Count Enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered Clock input triggers the flip-flops on the Low-to-High transition of the clock.

The counter is fully programmable; that is, the outputs may be preset to either level.

Presetting is synchronous with the clock and takes place regardless of the level of the Count Enable inputs. A Low level on the Parallel Enable (\overline{PE}) input disables the counter and causes the data at the D_n input to be loaded into the counter on the next Low-to-High transition of the clock.

The direction of counting is controlled by the Up/Down (U/\overline{D}) input; a High will cause the count to increase, a Low will cause the count to decrease.

The Carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs (\overline{CET} - \overline{CEP}) and a Terminal Count (\overline{TC}) output. Both Count Enable inputs must be Low to count. The \overline{CET} input is fed forward to enable the \overline{TC} output. The \overline{TC} output thus enabled will produce a Low output pulse with a duration approximately equal to the High level portion of the Low level portion of the Q_0 output depending on the state of the U/\overline{D} input. This Low level \overline{TC} pulse is used to enable successive cascaded stages.

FUNCTIONAL DESCRIPTION

The AC/ACT11269 uses edge-triggered D-type flip-flops and has no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the Clock and remain valid for the recommended hold time thereafter. The parallel load

operation takes precedence over the other operations, as indicated in the Mode Select Table. When \overline{PE} is Low, the data on the $D_0 - D_7$ inputs enter the flip-flops on the next rising edge of the Clock. In order for counting to occur, both \overline{CEP} and \overline{CET} must be Low and \overline{PE} must be High; the U/\overline{D} input then determines the direction of counting. The Terminal Count (\overline{TC}) output is normally High and goes Low when a counter reaches zero in the Count Down mode or reaches 15 in the Count Up mode, provided that \overline{CET} is Low. The \overline{TC} output state is not a function of the Count Enable Parallel (\overline{CEP}) input level. The \overline{TC} signal is derived by decoding the D-input signals of the counter flip-flops and using this decoded signal as the D-input driving the \overline{TC} output. Use of this configuration gives a \overline{TC} output which is free of decoding spikes. The possibility exists that on power-up that the \overline{TC} output may not give a true indication of the state of the counter (i.e., \overline{TC} may be Low while the counter is not at terminal count or High when it is at terminal count.) Should this occur, \overline{TC} will always go to a correct state on the first Low-to-High transition of the clock.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
27	\overline{PE}	Parallel enable input
1	CP	Clock input
28	U/\overline{D}	Up-Down count control input
16	\overline{CEP}	Count enable parallel input (active-Low)
15	\overline{CET}	Count enable trickle input (active-Low)
26, 25, 24, 23, 20, 19, 18, 17	$D_0 - D_7$	Parallel data inputs
2, 3, 4, 5, 10, 11, 12, 13	$Q_0 - Q_7$	Flip-flop outputs
14	\overline{TC}	Terminal count output (active-Low)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

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MODE SELECT—FUNCTION TABLE

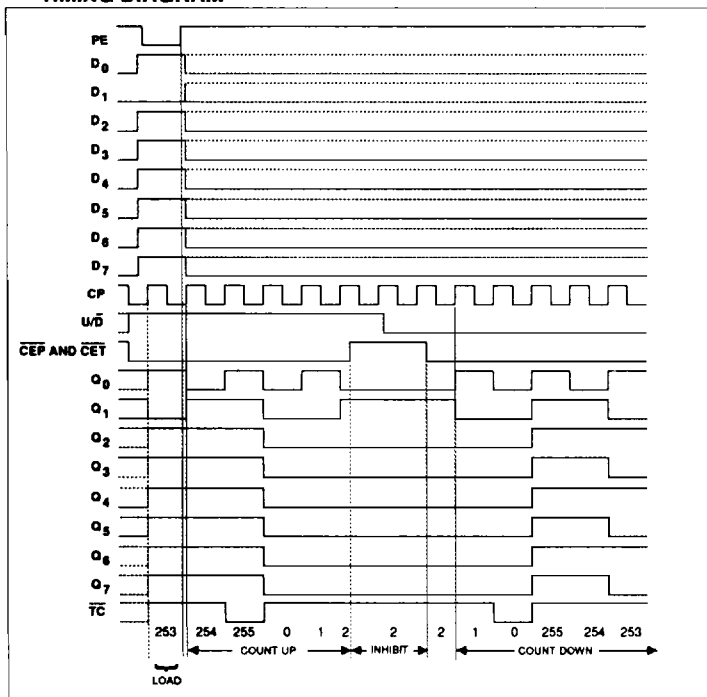
OPERATING MODE	INPUTS						OUTPUTS	
	CP	U/D	\overline{CEP}	\overline{CET}	\overline{PE}	D_n	Q_n	\overline{TC}
Parallel load	↑	X	X	X	l	l	L	(1)
	↑	X	X	X	l	h	H	(1)
Count up	↑	h	l	l	h	X	Count up	(1)
Count down	↑	l	l	l	h	X	Count down	(1)
Hold (do nothing)	↑	X	h	X	h	X	q_n	(1)
	↑	X	X	h	h	X	q_n	H

H = High voltage level steady state
 h = High voltage level one setup time prior to the Low-to-High clock transition
 L = Low voltage level steady state
 l = Low voltage level one setup time prior to the Low-to-High clock transition
 X = Don't care
 q_n = State of the referenced output prior to the Low-to-High clock transition
 ↑ = Low-to-High clock transition

NOTES:

1. \overline{TC} is Low when \overline{CET} is Low and the counter is at Terminal Count. Terminal Count Up is with all Q_n outputs High and Terminal Count Down is with all Q_n outputs Low.

TIMING DIAGRAM



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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11269			74ACT11269			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0 ¹	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta V/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

- No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK} or V_I	DC input diode current ²	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to $V_{CC} + 0.5$	V
I_{OK} or V_O	DC output diode current ²	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to $V_{CC} + 0.5$	V
I_O	DC output source or sink current per output pin	$V_O = 0$ to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±225	mA
	DC ground current		±225	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C: derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C: derate linearly by 6mW/K	400	mW

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	V _{CC}	74AC11269				74ACT11269				UNIT	
				T _A = +25°C		T _A = -40°C to +85°C		T _A = +25°C		T _A = -40°C to +85°C			
				Min	Max	Min	Max	Min	Max	Min	Max		
V _{IH}	High-level input voltage		3.0	2.10		2.10						V	
			4.5	3.15		3.15		2.0		2.0			
			5.5	3.85		3.85		2.0		2.0			
V _{IL}	Low-level input voltage		3.0		0.90		0.90					V	
			4.5		1.35		1.35		0.8		0.8		
			5.5		1.65		1.65		0.8		0.8		
V _{OH}	High-level output voltage	V _I = V _{IL} or V _{IH}	I _{OH} = -50μA	3.0	2.9		2.9					V	
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
				I _{OH} = -4mA	3.0	2.58		2.48					
					4.5	3.94		3.8		3.94			3.8
					5.5	4.94		4.8		4.94			4.8
I _{OH} = -75mA ¹	5.5			3.85				3.85					
V _{OL}	Low-level output voltage	V _I = V _{IL} or V _{IH}	I _{OL} = 50μA	3.0		0.1		0.1				V	
				4.5		0.1		0.1		0.1	0.1		
				5.5		0.1		0.1		0.1	0.1		
				I _{OL} = 12mA	3.0		0.36		0.44				
					4.5		0.36		0.44		0.36		0.44
					5.5		0.36		0.44		0.36		0.44
I _{OL} = 75mA ¹	5.5				1.65			1.65					
I _I	Input leakage current	V _I = V _{CC} or GND	5.5		±0.1		±1.0		±0.1	±1.0	μA		
I _{CC}	Quiescent supply current	V _I = V _{CC} or GND, I _O = 0	5.5		8.0		80		8.0	80	μA		
ΔI _{CC}	Supply current, TTL inputs High ²	One input at 3.4V, other inputs at V _{CC} or GND	5.5						0.9	1.0	mA		

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
- This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.