QUAD 2-INPUTS EXCLUSIVE-OR GATE — 54/74386

SPEED/PACKAGE AVAILABILITY

54LS F,W 74LS A

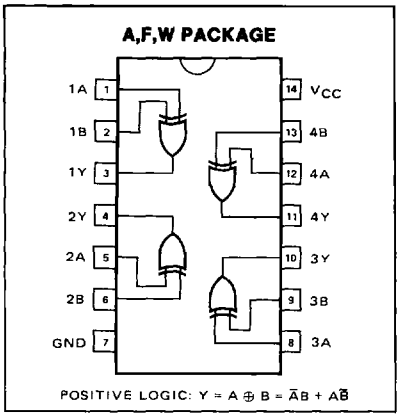
FUNCTION TABLE

(EACH GATE)

INPUTS		OUTPUT
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

H = high level
L = low level

PIN CONFIGURATION



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★	FROM (INPUT)	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	C_L = 15pF, R_L = 2kΩ		10	23	ns
t_{PHL}					10	17	
t_{PLH}	A or B	Other input high			10	30	ns
t_{PHL}					10	22	

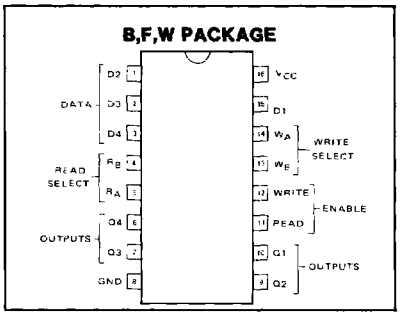
★t_{PLH} = propagation delay ti

4x4 REGISTER FILE WITH 3-STATE OUTPUTS — 54/74670

SPEED/PACKAGE AVAILABILITY

54LS F,W 74LS B

PIN CONFIGURATION



DESCRIPTION

The S54LS670 and N74LS670 MSI 16-bit TTL register files incorporate the equivalent of 98 gates. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, G_W, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, G_R, is high, the data outputs are inhibited and go into the high-impedance state.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appeaars at the four outputs.

This arrangement—data-entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (27 nanoseconds typical). The register file has a nondestructive readout in that data is not lost when addressed.

All inputs except read enable and write enable are buffered to lower the drive requirements to one Series 54LS/74LS standard load, and input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and have high-sink-current, three-state outputs. Up to 128 of these outputs may be wire-AND connected for increasing the capacity up to 512 words. Any number of these registers may be paralleled to provide n-bit word length.

WRITE FUNCTION TABLE

(See Notes A, B and C)

WRITE INPUTS			WORD			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q=D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q=D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q=D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q=D
X	X	H	Q_0	Q_0	Q_0	Q_0

READ FUNCTION TABLE

(See Notes A and D)

READ INPUTS			OUTPUTS			
R_B	R_A	G_R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

NOTES:

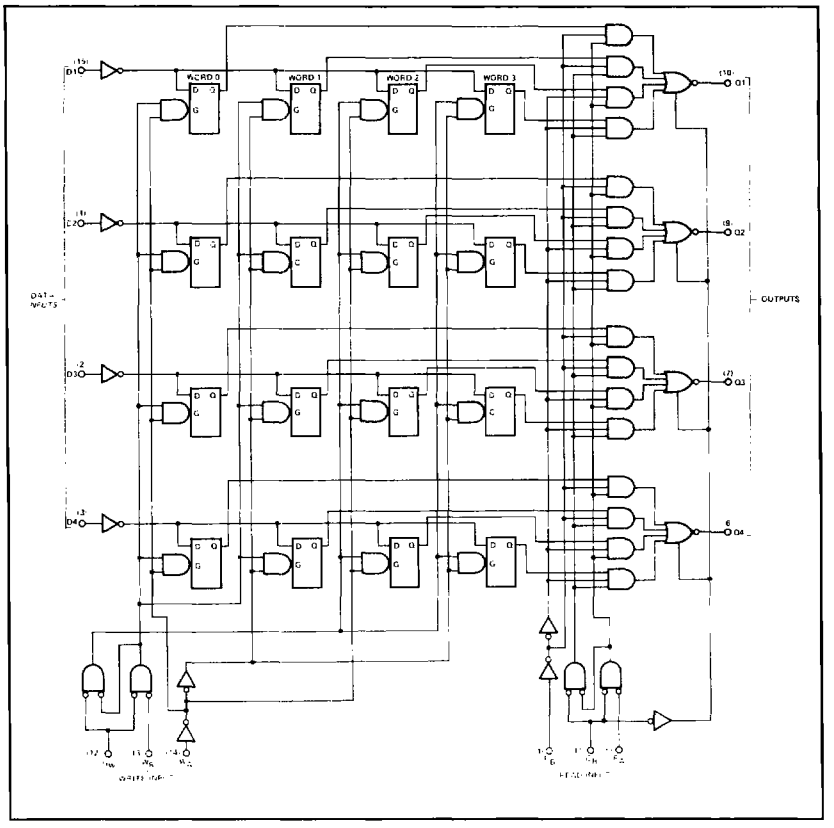
A. *H = high level, L = low level, X = irrelevant, Z = high impedance (off).*

B. *(Q = D) = The four selected internal flip-flop outputs will assume the inverse of the states applied to the four external data inputs.*

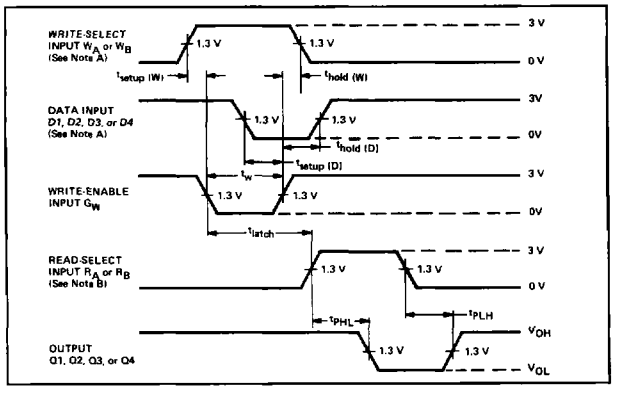
C. *Q_0 = the level of Q before the indicated input conditions were established.*

D. W0B1 = The first bit of word 0, etc.

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION



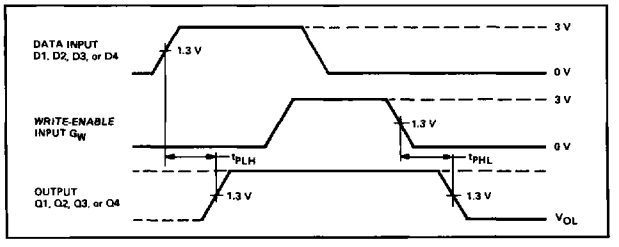
VOLTAGE WAVEFORMS (S1 AND S2 ARE CLOSED)

NOTES:

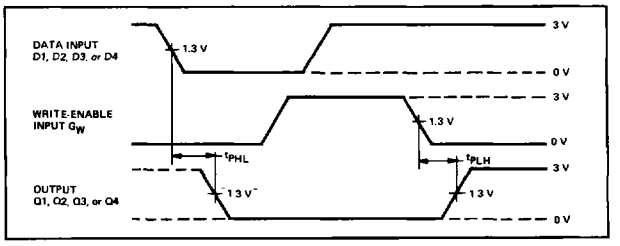
A. High-level input pulses at the select and data inputs are illustrated; however, times associated with low-level pulses are measured from the same reference points.

B. When measuring delay times from a read-select input, the read-enable input is low.

C. Input waveforms are supplied by generators having the following characteristics: PRR ≤ 2 MHz, Z_{out} ≈ 50 Ω, duty cycle ≤ 50%, t_r ≤ 15 ns, t_f ≤ 6 ns.



VOLTAGE WAVEFORM 1 (S1 AND S2 ARE CLOSED)



VOLTAGE WAVEFORM 2 (S1 AND S2 ARE CLOSED)

NOTES:

A. Each select address is tested. Prior to the start of each of the above tests both write and read address inputs are stabilized with W_A = R_A and W_B = R_B. During the test G_R is low.

B. Input waveforms are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} ≈ 50 Ω, duty cycle ≤ 50%, t_r ≤ 15 ns, t_f ≤ 6 ns.

Load circuit is shown at front of book (for three state outputs).

LOGIC

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_W	Width of write-enable or read-enable pulse				25			ns
t_{Setup}	Input setup time (See fig. 2)	Data input	Write-enable		10			ns
		Write-select	Write-enable		15			
t_{Hold}	Input hold time (See note 2 & fig. 2)	Data input	Write-enable		15			ns
		Write-select	Write-enable		5			
t_{Latch}	Latch time for new data (Note 3)				25			ns
Propagation delay time								
t_{PLH}	Low-to-high	Read select	Any Q			23	40	ns
t_{PHL}	High-to-low					25	45	
t_{PLH}	Low-to-high	Write enable	Any Q	C_L = 15pF, R_L = 2kΩ		26	45	ns
t_{PHL}	High-to-low					28	50	
t_{PLH}	Low-to-high	Data	Any Q			25	45	ns
t_{PHL}	High-to-low					23	40	
t_{ZH}	Output enable time to high level					15	35	ns
t_{ZL}	Output enable time to low level		Any Q			22	40	
t_{HZ}	Output disable time from high level	Read enable				30	50	ns
t_{LZ}	Output disable time from low level					16	35	

NOTES:
1. Voltage values are with respect to network ground terminal.
2. Write-select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{Setup(w)}$ can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during $t_{Hold(w)}$ will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.
3. Latch time is the time allowed for the internal output of the latch to assume the state of new data. See Figure 2. This is important only when attempting to read from a location immediately after that location has received new data.

SPEED/PACKAGE AVAILABILITY

S9300 F,W N9300 B

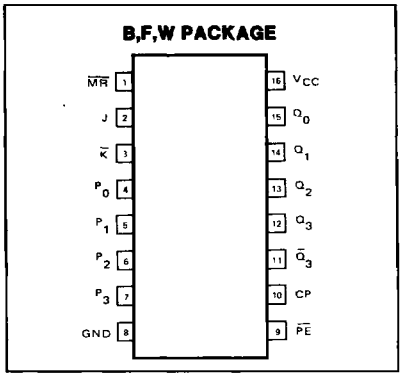
TRUTH TABLE

J	$\overline{K}$	Q at t
L	L	L
L	H	Q at t (no change)
H	L	$\overline{Q}$ at t (toggles)
H	H	H

$\overline{PE}$ = High, $\overline{MR}$ = High. (n + 1) indicates state after next clock.

PIN CONFIGURATION

B,F,W PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS		9300 C_L = 15pf			
PARAMETER		MIN	TYP	MAX	UNIT
t_{PD+}	Turn off delay		20	35	ns
t_{PD-}	Turn on delay		25	45	ns
f_{SR}	Shift right register	15	25		MHz
CP_{pw}	Clock pulse width	35	15		ns
t_s	Setup time	35	17		ns
t_r	Release time		16	0	ns
$t_{s(\overline{PE})}$	Setup time for $\overline{PE}$	45	26		ns
$t_{r(\overline{PE})}$	Release time for $\overline{PE}$		25	10	ns
$t_{PD-(\overline{MR})}$	Reset time for $\overline{MR}$		35		ns
$t_{rec\ (\overline{MR})}$	Recovery time for $\overline{MR}$		20		ns
$\overline{MR}_{pw}$	Min reset pulse width		15		ns

NOTE:
For electrical specifications, refer to 54/74195 data sheet.
Load circuit and typical waveforms shown in 54/74195 section.

SPEED/PACKAGE AVAILABILITY

S9301 F,W N9301 B

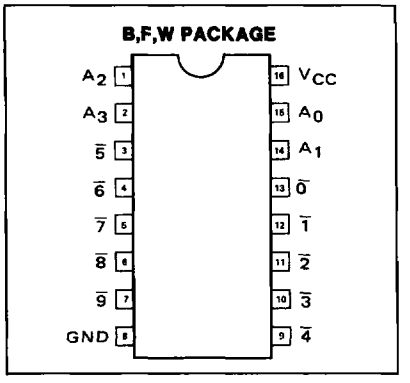
TRUTH TABLE

A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

NOTES:
For electrical characteristics, refer to 8252 data sheet.
H = High voltage level
L = Low voltage level

PIN CONFIGURATION

B,F,W PACKAGE



LOGIC DIAGRAM