

54AC/74AC299 • 54ACT/74ACT299 8-Input Universal Shift/Storage Register with Common Parallel I/O Pins

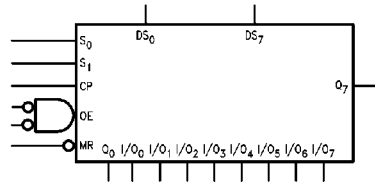
General Description

The 'AC/'ACT299 is an 8-bit universal shift/storage register with TRI-STATE® outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q₀, Q₇ to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

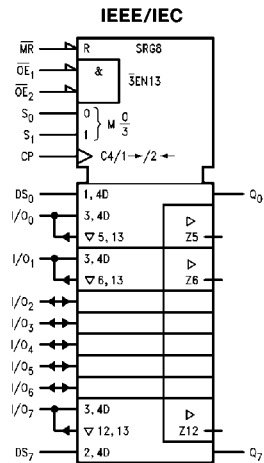
Features

- I_{CC} and I_{OZ} reduced by 50%
- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: shift left, shift right, load and store
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- 'ACT299 has TTL-compatible inputs
- Standard Military Drawing (SMD)
 - 'AC299: 5962-88754
 - 'ACT299: 5962-88771

Logic Symbols



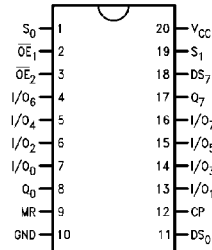
TL/F/9893-1



TL/F/9893-4

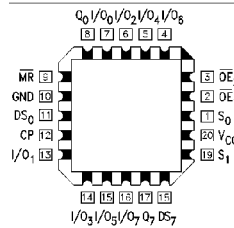
Connection Diagrams

Pin Assignment
for DIP, Flatpak and SOIC



TL/F/9893-2

Pin Assignment
for LCC



TL/F/9893-3

TRI-STATE® is a registered trademark of National Semiconductor Corporation.
FACT™ is a trademark of National Semiconductor Corporation.

Pin Names	Description
CP	Clock Pulse Input
DS ₀	Serial Data Input for Right Shift
DS ₇	Serial Data Input for Left Shift
S ₀ , S ₁	Mode Select Inputs
MR	Asynchronous Master Reset
\overline{OE}_1 , \overline{OE}_2	TRI-STATE Output Enable Inputs
I/O ₀ -I/O ₇	Parallel Data Inputs or TRI-STATE Parallel Outputs
Q ₀ , Q ₇	Serial Outputs




Functional Description


The 'AC/'ACT299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S₀ and S₁, as shown in the Truth Table. All flip-flop outputs are brought out through TRI-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q₀ and Q₇ are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on \overline{MR} overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

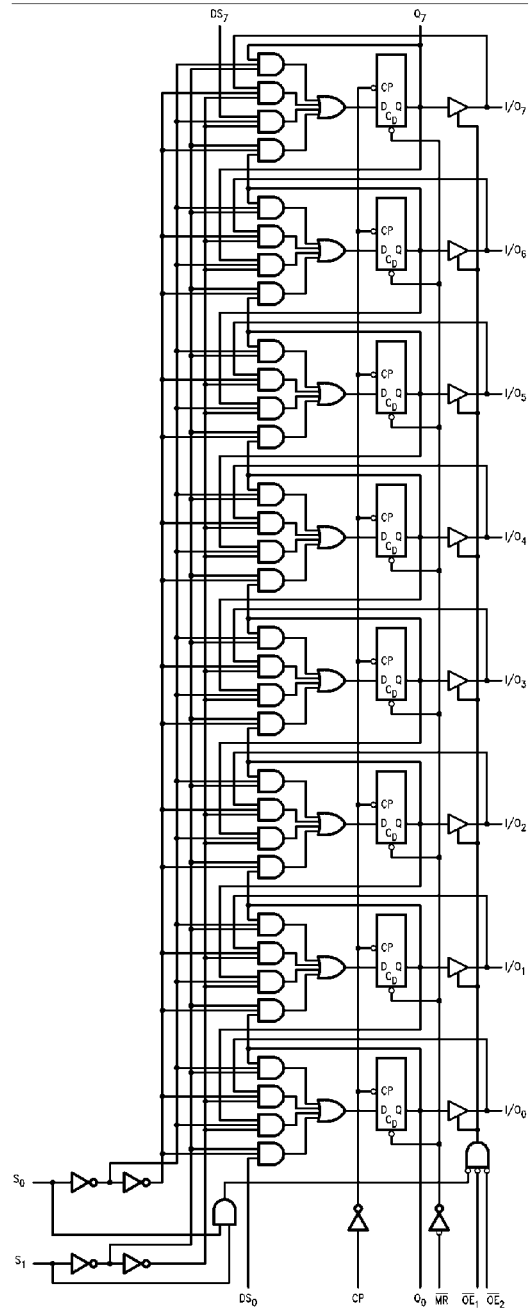
A HIGH signal on either \overline{OE}_1 or \overline{OE}_2 disables the TRI-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The TRI-STATE buffers are also disabled by HIGH signals on both S₀ and S₁ in preparation for a parallel load operation.

Truth Table

Inputs				Response
MR	S ₁	S ₀	CP	
L	X	X	X	Asynchronous Reset; Q ₀ -Q ₇ = LOW
H	H	H		Parallel Load; I/O _n → Q _n
H	L	H		Shift Right; DS ₀ → Q ₀ , Q ₀ → Q ₁ , etc.
H	H	L		Shift Left; DS ₇ → Q ₇ , Q ₇ → Q ₆ , etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
 = LOW-to-HIGH Transition

Logic Diagram



TL/F/9893-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	-20 mA
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	-20 mA
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
Per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Obviously the databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC}) (Unless Otherwise Specified)	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.0V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	-40°C to +85°C
54AC/ACT	-55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Electrical Characteristics For 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC			54AC		74AC		Units	Conditions
			$T_A = 25^\circ\text{C}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			
			Typ	Guaranteed Limits							
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1		2.1		V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	3.15	3.15		3.15				
		5.5	2.75	3.85	3.85		3.85				
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9		0.9		V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	1.35	1.35		1.35				
		5.5	2.75	1.65	1.65		1.65				
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9		2.9		V	$I_{OUT} = -50 \mu\text{A}$	
		4.5	4.49	4.4	4.4		4.4				
		5.5	5.49	5.4	5.4		5.4				
			3.0		2.56	2.4		2.46		V	* $V_{IN} = V_{IL}$ or V_{IH} -12 mA I_{OH} -24 mA -24 mA
			4.5		3.86	3.7		3.76			
			5.5		4.86	4.7		4.76			
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1		0.1		V	$I_{OUT} = 50 \mu\text{A}$	
		4.5	0.001	0.1	0.1		0.1				
		5.5	0.001	0.1	0.1		0.1				
			3.0		0.36	0.50		0.44		V	* $V_{IN} = V_{IL}$ or V_{IH} 12 mA I_{OH} 24 mA 24 mA
			4.5		0.36	0.50		0.44			
			5.5		0.36	0.50		0.44			
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0		±1.0		μA	$V_I = V_{CC}, \text{GND}$	

*All outputs loaded; threshold on input associated with output under test.

DC Electrical Characteristics For 'AC Family Devices

Symbol	Parameter	V _{CC} (V)	74AC		54AC	74AC		Units	Conditions
			T _A = 25°C		T _A = -55°C to +125°C	T _A = -40°C to +85°C			
			Typ	Guaranteed Limits					
I _{OLD}	† Minimum Dynamic Output Current	5.5			50		86	mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5			-50		-75	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0		40.0	μA	V _{IN} = V _{CC} or GND
I _{OZT}	Maximum I/O Leakage Current	5.5		±0.3	±5.5		±3.0	μA	V _{I(OE)} = V _{IL} , V _{IH} V _I = V _{CC} , GND V _O = V _{CC} , GND

*All outputs loaded; threshold on input associated with output under test.

†Maximum test duration 20 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Electrical Characteristics For 'ACT Family Devices

Symbol	Parameter	V _{CC} (V)	74ACT		54ACT	74ACT		Units	Conditions
			T _A = 25°C		T _A = -55°C to +125°C	T _A = -40°C to +85°C			
			Typ	Guaranteed Limits					
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0		2.0	V	V _{OUT} = 0.1V or V _{CC} - 0.1V
		5.5	1.5	2.0	2.0		2.0		
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8		0.8		V _{OUT} = 0.1V or V _{CC} - 0.1V
		4.5	1.5	0.8	0.8		0.8		
V _{OH}	Minimum High Level	4.5	4.49	4.4	4.4		4.4	V	I _{OUT} = -50 μA
		5.5	5.49	5.4	5.4		5.4		
		4.5	0.0001	3.86	3.70		3.76	V	*V _{IN} = V _{IL} or V _{IH} I _{OH} = -24 mA -24 mA
		5.5		4.86	4.70		4.76		
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1		0.1	V	I _{OUT} = 50 μA
		5.5	0.001	0.1	0.1		0.1		
		4.5		0.36	0.50		0.44	V	*V _{IN} = V _{IL} or V _{IH} I _{OL} = 24 mA 24 mA
		5.5		0.36	0.50		0.44		
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0		±1.0	μA	V _I = V _{CC} , GND
I _{CCT}	Maximum I _{CC} /Input	5.5	0.6		1.6		1.5	mA	V _I = V _{CC} - 2.1V
I _{OLD}	† Minimum Dynamic Output Current	5.5			50		75	mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5			-50		-75	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0		40.0	μA	V _{IN} = V _{CC} or GND
I _{OZT}	Maximum I/O Leakage Current	5.5		±0.3	±5.5		±3.0	μA	V _{I(OE)} = V _{IL} , V _{IH} V _I = V _{CC} , GND V _O = V _{CC} , GND

Note: I_{CC} limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0V
C _{PD}	Power Dissipation Capacitance	170	pF	V _{CC} = 5.5V

AC Electrical Characteristics

Symbol	Parameter	V _{CC} * (V)	74AC			54AC		74AC		Units
			T _A = +25°C C _L = 50 pF			T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	Min	Max	
f _{max}	Maximum Input Frequency	3.3 5.0	90 130	124 173		70 80		80 105	MHz	
t _{PLH}	Propagation Delay CP to Q ₀ or Q ₇ (Shift Left or Right)	3.3 5.0	8.5 5.5	14.0 9.5	20.5 14.0	1.0 1.0	25.5 17.5	7.0 4.5	22.0 15.0	ns
t _{PHL}	Propagation Delay CP to Q ₀ or Q ₇ (Shift Left or Right)	3.3 5.0	8.5 5.5	14.5 10.0	21.5 14.5	1.0 1.0	26.5 18.0	7.0 5.0	23.0 16.0	ns
t _{PLH}	Propagation Delay CP to I/O _n	3.3 5.0	9.0 6.0	14.5 10.0	20.5 14.5	1.0 1.0	24.5 17.0	7.5 5.0	22.5 16.0	ns
t _{PHL}	Propagation Delay CP to I/O _n	3.3 5.0	10.0 6.5	16.0 11.0	23.0 16.0	1.0 1.0	26.5 18.5	8.5 6.0	24.5 17.5	ns
t _{PHL}	Propagation Delay MR to Q ₀ or Q ₇	3.3 5.0	9.0 5.5	15.5 10.5	22.5 15.5	1.0 1.0	27.0 18.5	7.5 5.0	25.0 17.0	ns
t _{PHL}	Propagation Delay MR to I/O _n	3.3 5.0	9.0 5.5	15.0 10.0	21.5 15.0	1.0 1.0	26.5 18.0	7.5 5.0	24.0 16.5	ns
t _{pZH}	Output Enable Time OE to I/O _n	3.3 5.0	7.0 4.5	12.0 8.5	18.0 12.5	1.0 1.0	22.0 15.0	6.0 4.0	19.5 13.5	ns
t _{pZL}	Output Enable Time OE to I/O _n	3.3 5.0	7.0 5.0	12.5 8.0	18.0 12.5	1.0 1.0	23.5 16.0	6.0 4.0	20.5 14.0	ns
t _{PHZ}	Output Disable Time OE to I/O _n	3.3 5.0	6.5 3.5	13.0 9.5	18.5 14.0	1.0 1.0	22.5 17.0	5.5 3.0	19.5 15.0	ns
t _{PLZ}	Output Disable Time OE to I/O _n	3.3 5.0	5.5 3.5	11.5 8.0	17.0 12.5	1.0 1.0	21.5 16.0	4.5 2.0	19.0 13.5	ns

*Voltage Range 3.3 is 3.3V ±0.3V.
Voltage Range 5.0 is 5.0V ±0.5V.

AC Operating Requirements

Symbol	Parameter	V _{CC} * (V)	74AC		54AC	74AC	Units
			T _A = +25°C C _L = 50 pF		T _A = -55°C to +125°C C _L = 50 pF	T _A = -40°C to +85°C C _L = 50 pF	
			Typ	Guaranteed Minimum			
t _s	Setup Time, HIGH or LOW S ₀ or S ₁ to CP	3.3 5.0	3.0 2.0	8.0 5.0	9.5 7.0	8.5 5.5	ns
t _h	Hold Time, HIGH or LOW S ₀ or S ₁ to CP	3.3 5.0	-3.0 -1.5	0.5 1.0	2.0 2.5	0.5 1.0	ns
t _s	Setup Time, HIGH or LOW I/O _n to CP	3.3 5.0	2.0 1.0	5.5 3.5	6.0 4.0	6.0 4.0	ns
t _h	Hold Time, HIGH or LOW I/O _n to CP	3.3 5.0	-2.0 -1.0	0 1.0	1.5 2.0	0 1.0	ns
t _s	Setup Time, HIGH or LOW DS ₀ or DS ₇ to CP	3.3 5.0	2.5 1.5	6.5 4.0	7.5 5.0	7.0 4.5	ns
t _h	Hold Time, HIGH or LOW DS ₀ or DS ₇ to CP	3.3 5.0	-2.0 -1.0	0 1.0	1.5 1.5	0.5 1.0	ns
t _w	CP Pulse Width, LOW	3.3 5.0	3.5 2.0	4.5 3.5	5.5 5.0	5.0 3.5	ns
t _w	MR Pulse Width, LOW	3.3 5.0	4.0 2.0	4.5 3.5	5.5 5.0	5.0 3.5	ns
t _{rec}	Recovery Time MR to CP	3.3 5.0	0 0.5	1.5 1.5	2.5 2.5	1.5 1.5	ns

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V _{CC} * (V)	74ACT			54ACT		74ACT		Units
			T _A = +25°C C _L = 50 pF			T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	Min	Max	
f _{max}	Maximum Input Frequency	5.0	120	170		70		110	MHz	
t _{PLH}	Propagation Delay CP to Q ₀ or Q ₇ (Shift Left or Right)	5.0	4.0	8.5	12.5	1.0	15.5	3.0	14.0	ns
t _{PHL}	Propagation Delay CP to Q ₀ or Q ₇ (Shift Left or Right)	5.0	4.0	9.0	13.5	1.0	16.0	3.5	15.0	ns
t _{PLH}	Propagation Delay CP to I/O _n	5.0	4.5	8.5	12.5	1.0	15.0	4.5	13.5	ns
t _{PHL}	Propagation Delay CP to I/O _n	5.0	5.0	9.5	15.0	1.0	18.0	4.5	16.5	ns
t _{PHL}	Propagation Delay MR to Q ₀ or Q ₇	5.0	4.0	14.0	15.0	1.0	18.0	4.0	18.0	ns
t _{PHL}	Propagation Delay MR to I/O _n	5.0	4.0	13.0	14.5	1.0	17.5	3.5	17.5	ns
t _{PZH}	Output Enable Time OE to I/O _n	5.0	2.5	8.0	12.0	1.0	14.0	1.5	13.0	ns
t _{PZL}	Output Enable Time OE to I/O _n	5.0	2.0	8.0	12.0	1.0	14.5	1.5	13.5	ns
t _{PHZ}	Output Disable Time OE to I/O _n	5.0	2.0	8.5	12.5	1.0	14.5	2.0	13.5	ns
t _{PLZ}	Output Disable Time OE to I/O _n	5.0	2.5	8.0	11.5	1.0	14.0	2.0	12.5	ns

*Voltage Range 5.0 is 5.0V ±0.5V

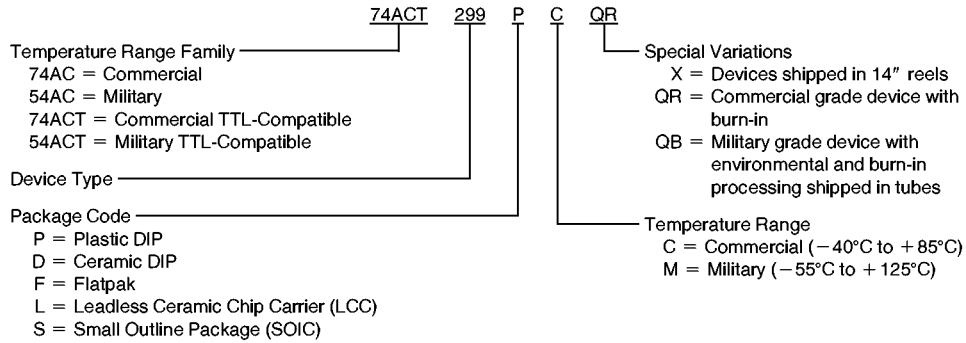
AC Operating Requirements

Symbol	Parameter	V _{CC} * (V)	74ACT		54ACT		74ACT		Units
			T _A = +25°C C _L = 50 pF		T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum					
t _s	Setup Time, HIGH or LOW S ₀ or S ₁ to CP	5.0	2.0	5.0	6.5	5.5			ns
t _h	Hold Time, HIGH or LOW S ₀ or S ₁ to CP	5.0	-2.0	1.0	1.5	1.0			ns
t _s	Setup Time, HIGH or LOW I/O _n to CP	5.0	1.5	4.0	4.5	4.5			ns
t _h	Hold Time, HIGH or LOW I/O _n to CP	5.0	-1.0	1.0	1.5	1.0			ns
t _s	Setup Time, HIGH or LOW DS ₀ or DS ₇ to CP	5.0	1.5	4.5	5.5	5.0			ns
t _h	Hold Time, HIGH or LOW DS ₀ or DS ₇ to CP	5.0	-1.0	1.0	1.5	1.0			ns
t _w	CP Pulse Width HIGH or LOW	5.0	2.0	4.0	5.0	4.5			ns
t _w	MR Pulse Width, LOW	5.0	2.0	3.5	5.0	3.5			ns
t _{rec}	Recovery Time MR to CP	5.0	0	1.5	1.5	1.5			ns

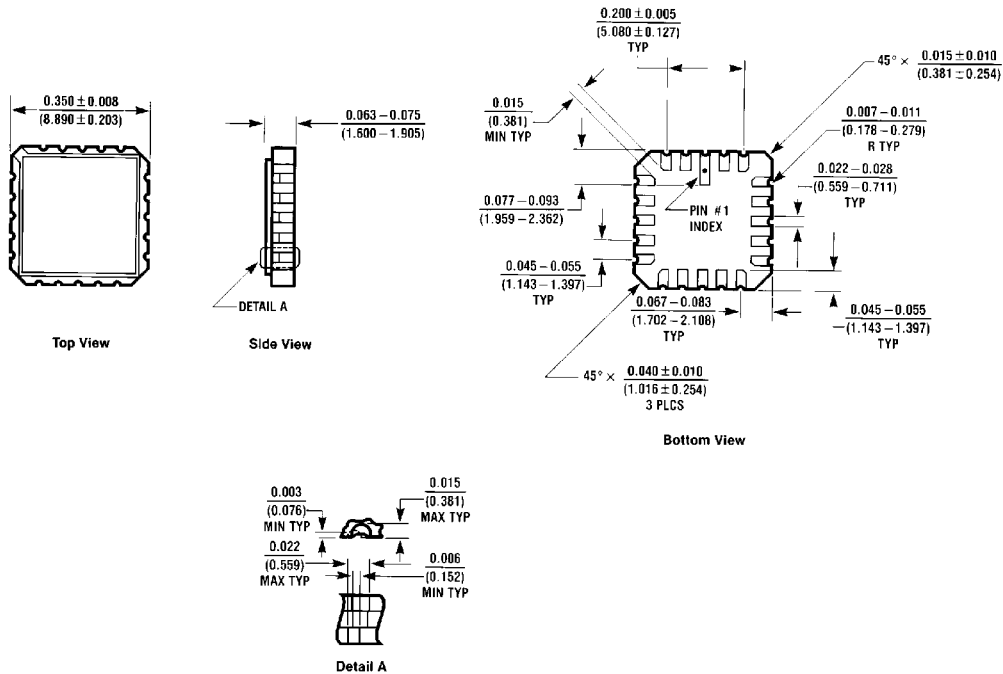
*Voltage Range 5.0 is 5.0V ±0.5V.

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



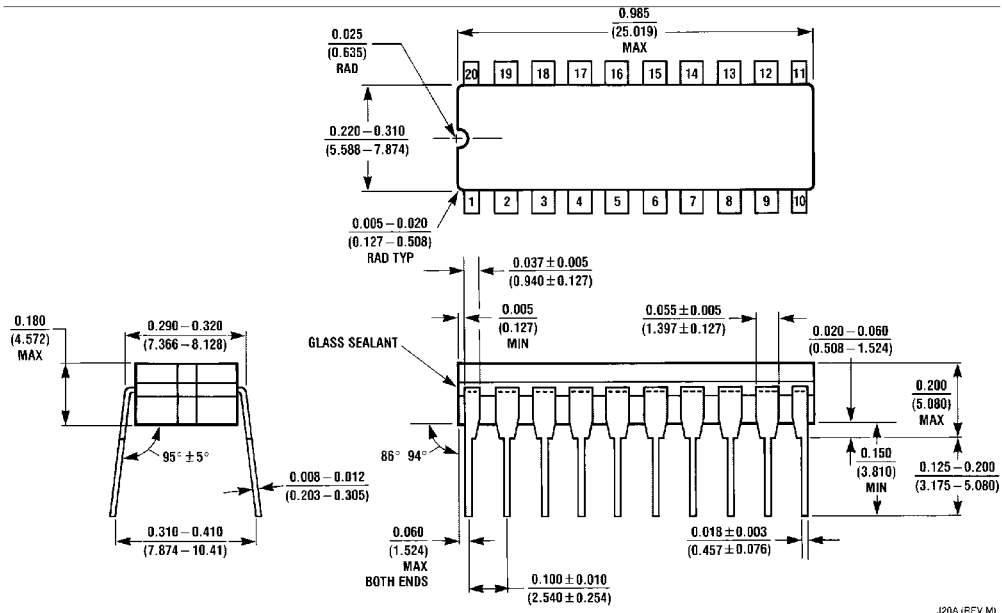
Physical Dimensions inches (millimeters)



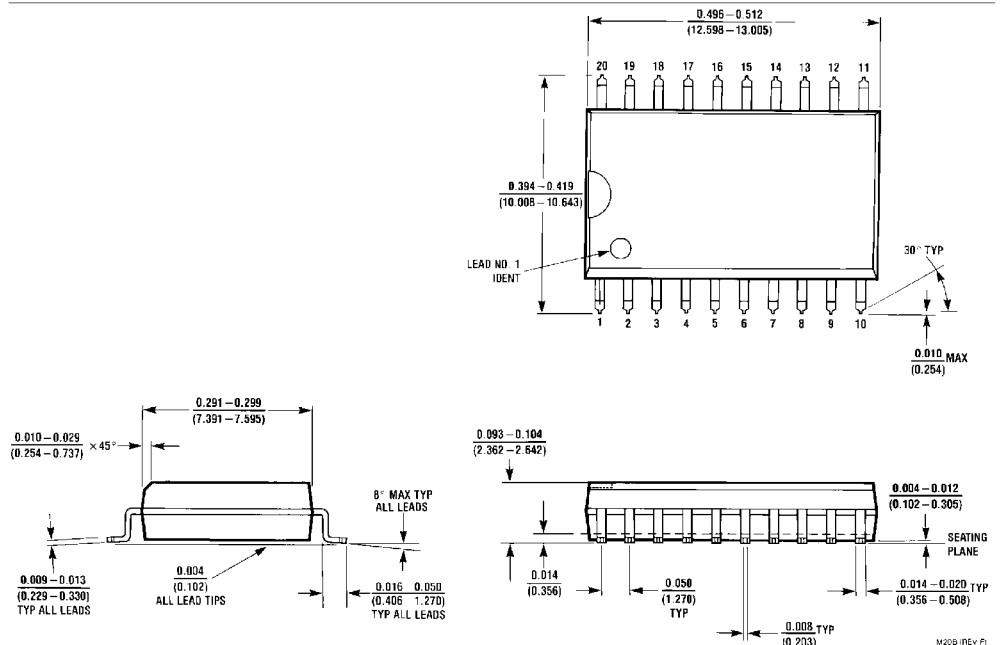
20 Terminal Ceramic Leadless Chip Carrier (LCC)
NS Package Number E20A

E20A (REV D)

Physical Dimensions inches (millimeters) (Continued)



20 Lead Ceramic Dual-In-Line Package (J)
NS Package Number J20A

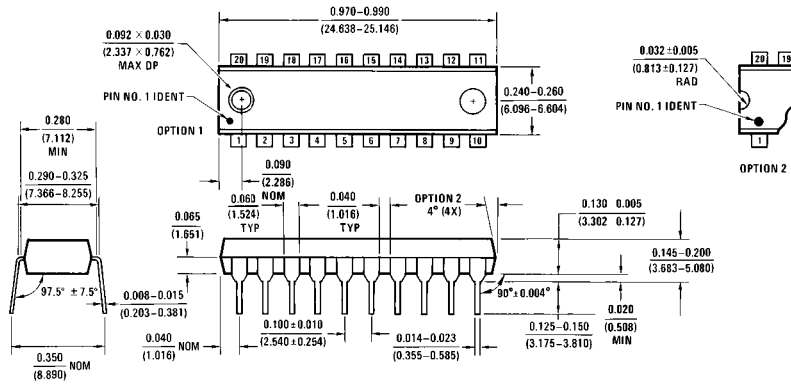


20 Lead Small Outline Integrated Circuit (SOIC)
NS Package Number M20B

**54AC/74ACT299 • 54ACT/74ACT299 8-Input Universal Shift/
Storage Register with Common Parallel I/O Pins**

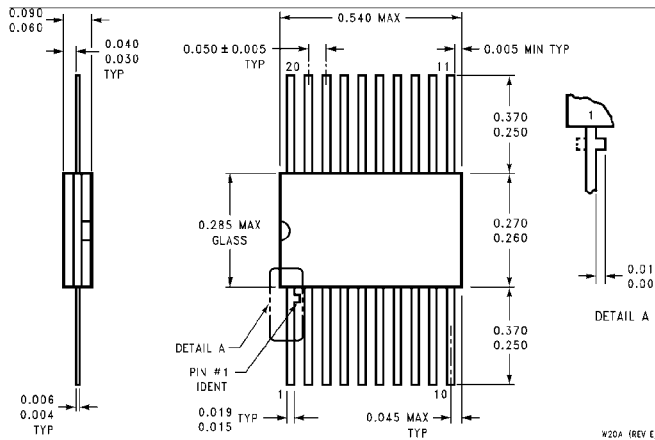
Physical Dimensions inches (millimeters) (Continued)

Lit. # 114631-1



**20 Lead Molded Dual-In-Line Package (N)
NS Package Number N20B**

N20B (REV A)



**20 Lead Ceramic FLATPAK
NS Package Number W20A**

W20A (REV C)

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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