# RLL (2,7) Data Separator

## GENERAL DESCRIPTION

The XR-532A is high speed, low power, single +5V supply data separator for disk drive applications. Data Synchronization and RLL (2,7) encoding and decoding are provided. The XR-532A, combined with an Exar Read/Write Preamplifier and Pulse detector, provides a complete Read/Write electronics channel for magnetic storage systems.

The XR-532A is manufactured with a BiCMOS process, providing high speed, accurate timing, and low power consumption. It operates with a single +5V power supply and is available in 3 packaging configurations:

28 Pin PLCC
28 Pin SOIC
32 Pin PQFP

## FEATURES

Low Noise, Low Jitter Data Synchronizer
High Speed RLL (2,7) ENDEC
Low Power Operation
Easily Adapted to Zoned Recording Applications
Hard or Soft Sector Compatible
Single +5V Supply
Advanced BiCMOS Technology

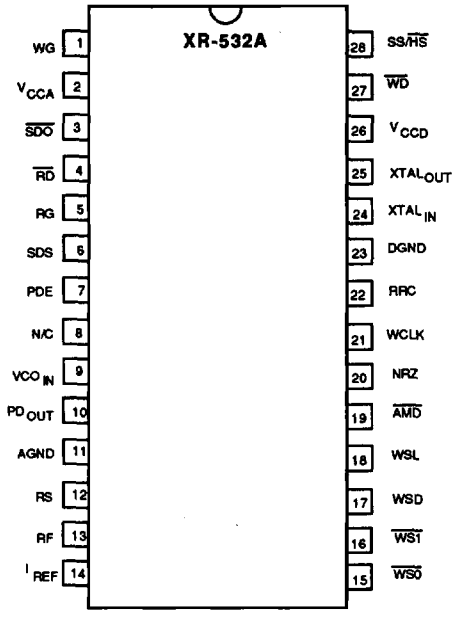
## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $V_{CCA}$, $V_{CCD}$ | 7V |
| Digital Inputs | -0.3V to $V_{CCD}$ +0.3V |
| Junction Temperature | 150°C |
| Storage Temperature | -65°C to 150°C |

## ORDERING INFORMATION

| Part Number | Package | Operating Temperature |
|---|---|---|
| XR-532ACJ | 28 Pin PLCC | 0°C to 70°C |
| XR-532ACD | 28 Pin SOIC | 0°C to 70°C |
| XR-532ACQ | 32 Pin PQFP | 0°C to 70°C |

## PIN ASSIGNMENT (SOIC)




## SYSTEM DESCRIPTION

The XR-532A is a 7.5 to 15 Mb/sec RLL (2,7) Data Synchronizer and ENDEC implemented in a low power BiCMOS process. This process allows independent optimization of the linear VCO and charge pump in high performance bipolar technology, while using fine geometry, low power CMOS for the numerous logic functions. The resulting device is faster than similar bipolar-only versions while dissipating less power. Only about 150mW of power is used during read operations.

Either hard sector or soft sector operation is supported.

The XR-532A data rate is adjusted with a single resistor. All necessary internal timings will track each other as this resistor value is changed, accommodating zoned recording applications.

## ELECTRICAL CHARACTERISTICS

**Test Conditions:** $T_A$ = 25°C to 70°C, $V_{CC}$ = 5.0V, 1/ TORC between 7.5 & 15MHz; 1/TVCO between 15 & 30 MHz.

Digital load capacitance limited to 15pF, 4.75 < $V_{CC}$ < 5.25V, unless otherwise specified.

Typicals are measured with $T_A$ = 25°C, $V_{CCA}$ = $V_{CCD}$ = 5.0V, 1/ TORC = 10MHz, 1/ TVCO = 20MHz.

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| ICC | Supply Current | | 30 | 50 | mA | |
| PD | Power Dissipation | | 150 | | mW | |
| **DIGITAL SIGNALS** | | | | | | |
| VIL | Input "Low" Voltage | | | 0.8 | V | |
| VIH | Input "High" Voltage | 2.0 | | | V | |
| IIL | Input "Low" Current | -0.4 | | | mA | VIL = 0.4V |
| IIH | Input "High" Current | | | 10 | µA | VIH = 2.7V |
| VOL | Output "Low" Voltage | | | 0.4 | V | IOL = 4mA |
| VOH | Output "High Voltage | 2.8 | 4.8 | | V | IOH = -0.4mA |
| **READ MODE** | | | | | | |
| | Maximum data rate | 15 | 20 | | Mbit/sec | Host NRZ Data Rate |
| TRD | Read Pulse Width (Data) | 20 | | TORC -40 | ns | |
| TFRD | Read Data Fall Time | | | 15 | ns | 2.0V to 0.8V |
| TRRC | Read Clock Rise Time | | | 8 | ns | 0.8V to 2.0V |
| TFRC | Read Clock Fall Time | | | 5 | ns | 2.0V to 0.8V |
| TPNRZ | NRZ Read Data Prop. Delay | -15 | | 15 | ns | |
| TPAMD | AMD Propagation Delay | -15 | | 15 | ns | |
| | 1/4 Cell Delay + Timer | -4 | | 4 | % | |
| | 1/4 Cell + Timer Delay Stability | 0.91 TD | TD | 1.09 TD | ns | See Note 1 @ $T_A$ = 25°C $V_{CC}$ = 5V |
| | 1/4 Cell + Timer Delay | 0.89 TD | | 1.11 TD | ns | |
| **WRITE MODE** | | | | | | |
| TWD | Write Data Pulse Width | TORO/2 -12 | TORO/2 | TORO/2 +12 | ns | |
| TFWD | Write Data Pulse Fall Time | | | 8 | ns | 2.4V to 0.8V |
| TOWC | Write Clock Repetition | TORO -12 | TORO | TORO +12 | ns | |
| TRWC | Write Clock Rise Time | | | 10 | ns | 0.8V to 2.4V |
| TFWC | Write Clock Fall Time | | | 8 | ns | 2.4V to 0.8V |
| | NRZ Set-Up Time | 20 | | | ns | |
| | NRZ Hold Time | 7 | | | ns | |

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| **DATA SYNCHRONIZER** | | | | | | |
| TVCO | VCO Center Frequency Period | 0.8TO | TO | 1.2TO | sec | VCC = 5.0V Note 2 |
| | VCO Frequency Dynamic Range | ±25 | | ±40 | % | VCC = 5.0V Note 3 |
| KVCO | VCO Control Gain | 0.14 $\omega_o$ | | 0.23 $\omega_o$ | rad/sec/V | $\omega_o = 2\pi$ / TO Note 3 |
| KD | Phase Detector Gain | 0.83KD | | 1.17KD | A/rad | VCC = 5.0V Note 4 |
| | KVCO x KD Product Accuracy | -28 | | +28 | % | |
| | VCO Phase Restart Error | -0.5 | | +0.5 | rad | |
| | Decode Window Centering Accuracy | | | ±(0.01* TORC +2) | ns | |
| | Decode Window | (TORC/2)-2 | | | ns | |
| TS1 | Decode Window Time Shift Magnitude | 0.60*TS1 | | 1.4*TS1 | sec | TS1 = 0.015 TORC |
| TS2 | Decode Window Time Shift Magnitude | 0.80 TS2 | | 1.2*TS2 | sec | TS2 = 0.06 TORC |
| TS3 | Decode Window Time Shift Magnitude | 0.80*TS3 | | 1.2*TS3 | sec | TS3 = 0.075 TORC |
| TSA | Decode Window Time Shift Magnitude | 0.65*TSA | | 1.35*TSA | sec | Note 5 |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| | TSWS, $\overline{WS0}$, $\overline{WS1}$, WSD Set-Up Time | 50 | | | ns | |
| | THWS, $\overline{WS0}$, $\overline{WS1}$, WSD Hold Time | 20 | | | ns | |
| | RG, WG, SS/$\overline{HS}$ Time Delay | | | 100 | ns | |

Notes:

1) TD = 6.14 ($R_{REF}$ + 0.5 KΩ) + 0.170 Rd (Cd +11.5) with Cd from 65pF to 100pF. $R_d$ & $R_{REF}$ in KΩ.
   $C_d$ = 82pf (7.5 ~11MB) and $C_d$ = 65pf (10~15MB).
2) VCO In = 2.7V, TO = 11.3 ($R_{REF}$ +500Ω) x $10^{-12}$.
3) VCO In from 1V to VCC -0.5V.
4) KD = 0.409 / (RREF + 500Ω)
5) TSA = 0.125 TORC $\left[ 1- \left[ \frac{R + 680}{R + 1180} \right] \right]$ R in Ohms, connected between RF/RS and AGND

## PIN DESCRIPTION

*(Pin # refers toPLCC /SOIC Packages)*

| Pin # | Name | Description |
|---|---|---|
| ***POWER PINS*** | | |
| 2 | $V_{CCA}$ | +5V for Analog Circuitry |
| 26 | $V_{CCD}$ | +5V for Digital Circuitry |
| 11 | AGND | Analog Ground |
| 23 | DGND | Digital Ground |
| ***CONTROL PINS*** | | |
| 1 | WG | Write Gate Control. Enables write mode. Internal pull-up resistor provided. |
| 5 | RG | Read Gate Control. Enables read mode. When low, the internal VCO is locked to the crystal oscillator. When high, the PLL synchronizes to Read Data (RD). Internal pull-up resistor provided. |
| 6 | SDS | Sync Detect Set. The R/C node here determines the one-shot timer period used for synchronization detection. |
| 7 | PDE | Phase Detector Enable. When low, the VCO free-runs. When high, the VCO receives the phase detector control voltage. Internal pull-up resistor provided. |
| 9 | VCO IN | VCO Input Control Voltage. Phase Detector control voltage applied here, determines VCO frequency. |
| 12 | RS | Symmetry Adjust Slow Resistor. Resistor from here to AGND (Pin 11) can eliminate window symmetry offset and maximize window margin. |
| 13 | RF | Symmetry Adjust Fast Resistor. Resistor from here to AGND (Pin 11) can eliminate window symmetry offset and maximize window margin. |
| 14 | IREF | Reference Current Set. A resistor from here to VCCA determines reference current, which sets VCO center frequency and anticipator (1/4 cell) delay. |
| 15 | $\overline{WS0}$ | When low, this pin digitally provides a 1.5% TORC window shift. Internal pull-up resistor. |
| 16 | $\overline{WS1}$ | When low, this pin digitally provides a 6% TORC window shift. Internal pull-up resistor. |
| 17 | WSD | Window Shift Direction. When low, shifts the window early by an amount determined by $\overline{WS0}$ (Pin 15), and $\overline{WS1}$ (Pin 16). When high, the window is shifted late. Internal pull-up resistor provided. |
| 18 | WSL | Window Shift Latch. When high, latches the window shift in the mode determined by WSD (Pin 17), $\overline{WS0}$ (Pin 15), and $\overline{WS1}$ (Pin 16). When window shift is not needed, this pin should be tied low. Internal pull-up resistor provided. |

| Pin # | Name | Description |
|---|---|---|
| 24 | XTAL IN | Crystal Oscillator Input. Also used as the external clock input (TTL compatible). |
| 25 | XTAL OUT | Crystal Oscillator Driver. When an external clock is employed, this pin must remain open. |
| 28 | SS/$\overline{HS}$ | Soft Sector / Hard Sector Select. When low, hard sector mode is selected. High chooses soft sector mode. Internal pull-up resistor provided. |

***INPUT/OUTPUT PINS***

| | | |
|---|---|---|
| 3 | $\overline{SDO}$ | Sync Detect Output. Goes low when 3T preamble sync field is detected. |
| 4 | $\overline{RD}$ | Read Data Input. TTL level, asserts low. Composite read data from the pulse detector enters here. |
| 10 | PDOUT | Phase Detector Output. The PLL filter placed here conditions the phase detector output before application to VCO IN. |
| 19 | $\overline{AMD}$ | Address Mark Detect Output. In the soft sector mode, successful address mark detection is signaled by a latched low AMD output. |
| 20 | NRZ | NRZ Data Input/Output Pin. This bidirectional I/O pin inputs write data and outputs read data, depending on device mode. CMOS compatible. |
| 21 | WC | Write Clock Input. Clock input for NRZ write data. |
| 22 | RRC | Read Reference Clock Output. In read mode, this is the NRZ read data clock. In the write mode, this output is the crystal reference divided by two. |
| 27 | $\overline{WD}$ | Write Data Output. Active low encoded RLL write data, directly compatible with all Exar read/write amplifiers. |

4

| RG | WG | Mode |
|---|---|---|
| 0 | 0 | Idle |
| 0 | 1 | Write |
| 1 | 0 | Read |
| 1 | 1 | Illegal |

**Table 1. Digital Control Modes**

| WSD | WS1 | WS0 | Window Shift |
|---|---|---|---|
| 0 | 0 | 0 | +TS3 |
| 0 | 0 | 1 | +TS2 |
| 0 | 1 | 0 | +TS1 |
| 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | -TS1 |
| 1 | 0 | 1 | -TS2 |
| 1 | 0 | 0 | -TS3 |

**Table 2. Delayed Data Shift Control**

| RLL (2,7) | NRZ |
|---|---|
| 0100 | 10 |
| 1000 | 11 |
| 000100 | 000 |
| 100100 | 010 |
| 001000 | 011 |
| 00100100 | 0010 |
| 00001000 | 0011 |

**Table 3. (2,7) RLL Conversion**

## GENERAL OPERATION

The XR-532A is designed to perform data recovery and data encoding in disk drives using 2,7 RLL encoding. In the Read Mode the XR-532A performs: Data Synchronization, Clock Recovery, Sync Field Search and Detect, Address Mark Detect and Data Decoding. In the Write Mode, the XR-532A converts NRZ data into 2,7 RLL, generates the Preamble Field, and inserts Address Marks (as requested).

The XR-532A can operate with data rates ranging from 7.5 to 20 Mbits/sec. This data rate is established by a single external resistor, RREF, connected from IREF to $V_{CCA}$. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/4 cell delay. The value of this resistor is given by:

$$R_{REF} = \frac{40670}{D} - 500\ (\Omega)$$

with RREF is in Ohms,
where: D = Data Rate in Mbits/sec.

An internal reference oscillator, operating at twice the data rate, generates the standby reference for the PLL. A series resonant crystal between XTALIN and XTALOUT should operate at twice the data rate. Alternatively, an external TTL compatible reference clock may be applied to XTALIN, leaving XTALOUT open.

The XR-532A employs a dual mode phase detector: its operation is harmonic in the read mode and non-harmonic in write and idle modes. In the read mode the harmonic phase detector updates the PLL with each occurrence of a DLYD DATA pulse. In the write and idle modes the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the crystal reference oscillator and utilizing a zero phase restart technique, false frequency locking to DLYD DATA in read acquisition is eliminated.

The phase detector incorporates a charge pump that drives the loop filter. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error. Figure 1 shows average output current as a function of the input phase error (relative to the VCO period).

The READ GATE (RG), and WRITE GATE (WG), inputs control the device mode as described in Table 1. RG is an asynchronous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output Write Data pulse.

## WRITE MODE

In the Write Mode the XR-532A converts NRZ data from the controller to 2,7 RLL formatted data for writing to disk. The XR-532A can operate with a soft or hard sectored disk drive. In the Soft Sector Mode, (SS/$\overline{HS}$ = 1) the device generates a 3T Preamble Field and can insert a N7V Address Mark. The N7V Address Mark is a valid 2,7 RLL pattern which is not contained in the code set. In the Hard Sector Mode, (SS/$\overline{HS}$ = 0) the device generates a 4T Preamble Field and no Address Mark. Serial NRZ data is clocked into the XR-532A and latched on defined cell boundaries. The NRZ input data must be synchronous with the rising edges of the WCLK input. In many configurations, WCLK can be connected directly to the RRC output.

## SOFT SECTOR MODE

In the Soft Sector Mode, when WRITE GATE (WG), transitions high and the NRZ input is held low, the XR-532A automatically generates the 3T (100) Preamble Field at the WRITE DATA ($\overline{WD}$), output. The 3T Preamble Field will continue to be generated until the first low to high transition on the NRZ line. As shown in Figure 8, the first low to high transition occurs with the second bit '1' of the $5_{16}$ (0101) in the $5EAx_{16}$ Address Mark, the XR-532A changes the '1' in the eleventh position of the 2,7 RLL encoded sequence, to a '0'. This generates a pattern of seven zero's followed by two zero's. This unique pattern satisfies the 2,7 RLL constraints, but will never occur during a normal encoding sequence. The $x_{16}$ of the $5EAx_{16}$ Address Mark generation pattern can be selected, a '$C_{16}$' (1100) was utilized in this example.

## HARD SECTOR MODE

In the Hard Sector Mode, when WG goes high and the NRZ input is held low, the XR-532A automatically generates the 4T (1000) Preamble Field at the Write Data, $\overline{WD}$, output. Note that in the Hard Sector mode, the NRZ input is inverted, therefore a constant low is equivalent to an '11...' input which generates the 4T

'1000...' Preamble Field. The 4T Preamble Field will be generated between the time WG goes high and the first low to high transition on the NRZ line. The XR-532A needs at least 32 4T (1000) bit groups prior to the data field.

**READ MODE**

The Data Synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read Gate, RG, initiates the PLL locking sequence and selects the PLL reference input; a high level (Read Mode) selects the RD input and a low level selects the crystal reference oscillator.

In Read Mode the rising edge of the internal signal DLYD DATA enables the Phase Detector while the falling edge is phase compared to the rising edge of the VCO. As depicted in Figure 2, DLYD DATA is a nominal 1/4 cell wide (TVCO/2) pulse whose leading edge is defined by the leading edge of RD. An accurate and symmetrical decode window is developed from the VCO clock. The decode window is generated from the falling edges of the VCO clock. By utilizing a symmetrical VCO running at twice the data rate, the decode window is insured to be accurate and centered symmetrically about the falling edges of DLYD DATA. The accuracy of the 1/4 cell delay does not influence the accuracy of the decode window.

The relative position of the DYLD DATA pulse can be shifted within the decode window. This powerful capability easily facilitates defect mapping, automatic calibration, window margin testing, error recovery, and systematic error cancellation. For enhanced disk drive testability and error recovery, decode window control is provided via a µP port (WSL, WSD, $\overline{WS0}$, $\overline{WS1}$) as described in Table 2. In applications not utilizing this feature, WSL should be connected to ground, while WSD, $\overline{WS0}$, and $\overline{WS1}$ can be left open.

Window shifts of ±1.5%, ±6, or ±7.5% of TORC are easily programmed by latching the appropriate control word into the Window Shift Register with the WSL pin. Shifts in the positive or negative directions result in early or late data bit positions within the decode windows respectively, as depicted in Figure 3. If window shifts are selected, the trailing edge of DLYD DATA will not appear phase locked to the falling edge of the VCO clock. See figure 3. Additionally, for small systematic error cancellation, a resistor, R, connected from either RS (Early) or RF (Late) to ground will provide analog control over the decode window. The magnitude of this shift, TSA is determined by:

$$TSA = 0.125\ TORC \left[ 1 - \left[ \frac{680 + R}{1180 + R} \right] \right]$$

where: R is in Ohms.

Pins RF and RS are intended to be used as a trim and should be restricted to ±1.5% window shifts. They can be used in conjunction with the digital control port.

In non-read modes, the PLL is locked to the crystal reference oscillator. This tunes the VCO at a frequency which is very close to that required for read back of actual data and thus minimizes the associated frequency step during acquisition. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment. In this manner (phase error ≤0.5 rads), the acquisition time is substantially reduced.

The XR-532A provides two sync modes for controlling the PLL locking sequence; Soft Sector and Hard Sector.

**SOFT SECTOR MODE**

The Soft Sector Mode activates the Preamble Search and Address Mark detection circuitry. When RG transitions high, the counter is reset and the XR-532A requires 10 high to low transitions (Preamble '1' bits) before switching the reference input to the PLL, 48 high to low transitions before switching the Read Reference Clock to the VCO clock divided by two and activating the Address Mark Detect circuitry; then it must detect the Address Mark prior to 80 high to low transitions in order to enter the Read Mode. This sequence repeats after 95 input '1' bits until the read mode is successfully entered or until RG is cancelled. See Figure 4.

**a). PREAMBLE SEARCH:**

After RG is enabled the 3T detect circuitry initiates the PLL locking sequence once it has detected 10 consecutive '100' bit groups. The 3T detect timing is set by the sum of the 1/4 cell delay and the retriggerable one-shot delay. The 1/4 cell timing

capacitor is included on-chip and its timing is externally set by resistor $R_{REF}$. The retriggerable one-shot timing is externally set by resistor Rd and capacitor Cd. The sum of their delays is set to 3.5 bit cell times. Therefore, a continuous stream of input pulses with a 3T bit cell time pulse rate keeps the one-shot reset, and a 4T or longer bit cell time input period allows the one-shot to time-out producing a 4T detect pulse. The 4T detect pulse resets the Input Counter and the search is started over.

**b) PLL LOCKING:**

Once 10 consecutive '100' bit groups are detected, the reference input to the PLL is switched from the crystal reference oscillator to the DLYD DATA, the VCO is phase reset to the next DLYD DATA pulse, and PLL acquisition begins. When an additional 38 '100' bit groups are detected, the Read Reference Clock output (RRC) is switched to the VCO clock divided by 2, the 4T Detect circuitry is inhibited, and the Address Mark Detection circuitry is enabled. If a 4T detect pulse occurs before 48 Preamble '1' bits are detected, then the PLL is locked back to the crystal reference oscillator, the RRC output is switched to the crystal reference oscillator divided by 2, the Input Counter reset, and the sequence is restarted. No short duration glitches will occur at the RRC output during this switching.

**c) ADDRESS MARK DETECTION:**

The circuit searches for the occurrence of the 5EAx16 Address Mark. If an Address Mark is detected prior to the Input Counter reaching count 80, the correct phase of the RRC is ensured by resetting the n/2 divider, the AMD output is latched low, the PLL acquisition sequence is terminated, and the Read Mode is entered allowing the data field to be read. If the Input Counter reaches count 80 before the Address Mark is detected, the PLL input is put back to the crystal reference oscillator, and the RRC output is switched to the crystal reference oscillator divided by 2. PLL acquisition sequence is restarted when the Input Counter reaches count 96. See Figure 4 and 5.

Additionally, if a non-3T pattern is detected during the Address Mark, search another part of the circuit is activated. This circuit expects to find an Address Mark within 24 VCO clocks after detecting the non-3T pattern. If an Address Mark is not detected during this period, the search for AM is aborted and the PLL acquisition sequence is restarted as described above, within three VCO cycles.

**HARD SECTOR MODE**

In the Hard Sector mode ($SS/\overline{HS} = 0$) the XR-532A utilizes a 4T (1000) Preamble Field and disables the Preamble Search and Address Mark detection circuitry. It allows the PLL to be controlled directly by RG for Hard Sector format operation. With the absence of an Address Mark, the 4T Preamble Field is utilized to properly set the bit cell alignment boundaries for proper decoding.

When RG transitions high, reference input to the PLL is switched from the crystal reference oscillator to DLYD DATA, the VCO is phase reset to the next DLYD DATA pulse, and the PLL acquisition begins. When 32 '1' Preamble bits are detected, the RRC output is switched to the VCO clock divided by 2, and the Read Mode is entered allowing the data field to be read. See Figure 6.



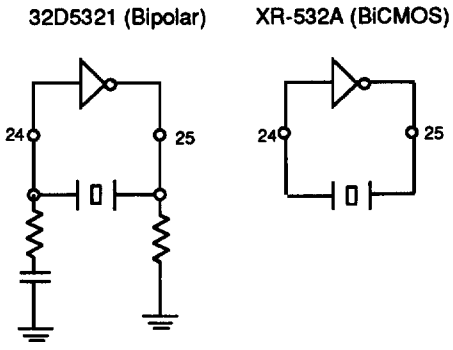
In the Hard Sector Mode, the NRZ output is inverted and will remain low until the data field is read, as shown in Figure 7. Since the Preamble Search circuitry is not utilized, the external one-shot timing components (Cd, Rd) are not required and the SDS pin can be left open.

**APPLICATION COMPARISON**

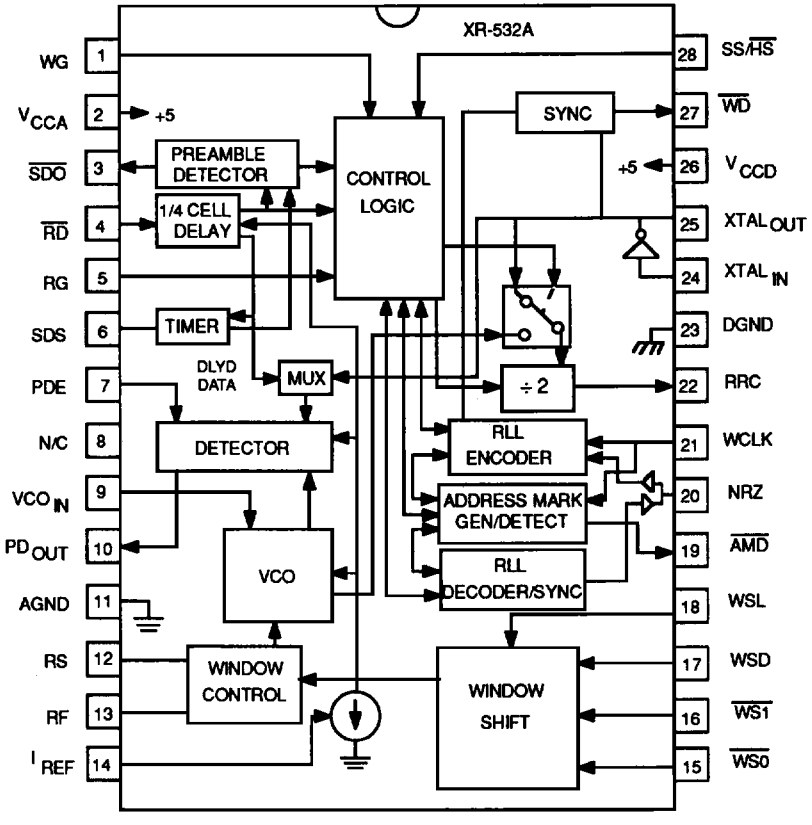
The XR-532A is pin-for-pin compatible with the SSI 32D5321. In most applications, improved performance will result when the XR-532A is employed, without any circuit changes. The XR-532A is a BiCMOS device and the SSI 32D5321 is a bipolar device. Application differences will include:

- XR-532A power consumption is only 150mW at 10MB/sec., compared to the approximately 750mW burned by the 32D5321.

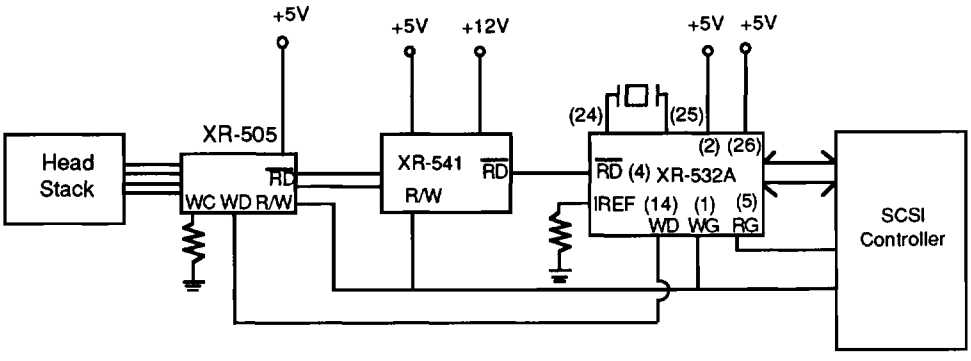
- XR-532A eliminates the need for the two resistor, one capacitor crystal oscillator start-up circuit required for 10MB/sec and faster operation with the 32D5321. This reduces circuit complexity and cost. In fact, these components, if used will cause problems with the higher impedance CMOS inverter, and should be removed (see drawing below). If an external clock is supplied, no change is required (see diagram next page).



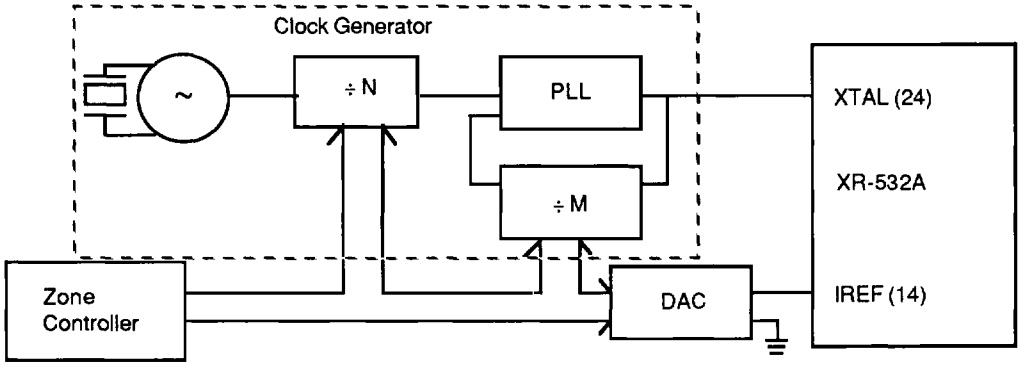

**Crystal Oscillator Circuits**



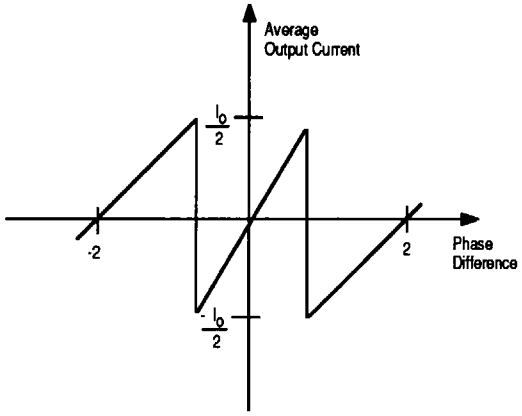

**XR-532A Functional Block Diagram**



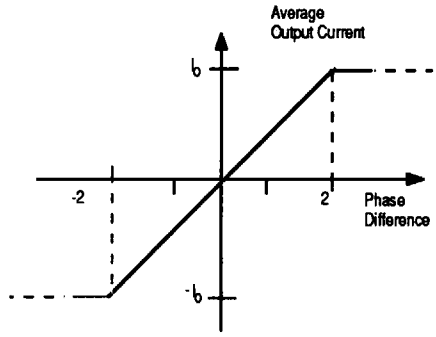

**Simple SCSI Disk Drive Read/Write channel with the XR-532A**




**Zoned Recording Implementation**




Harmonic Mode




Non-Harmonic Mode

Notes: 1. Io is the magnitude of the charge pump current
2. Phase error is relative to the VCO period

**Figure 1. Phase Detector Transfer Characteristics**

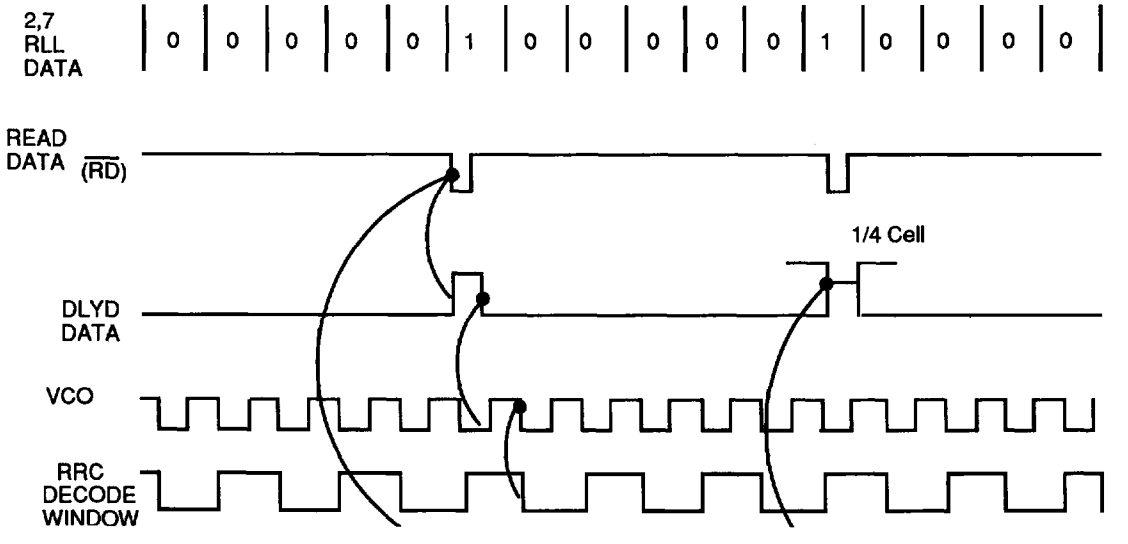
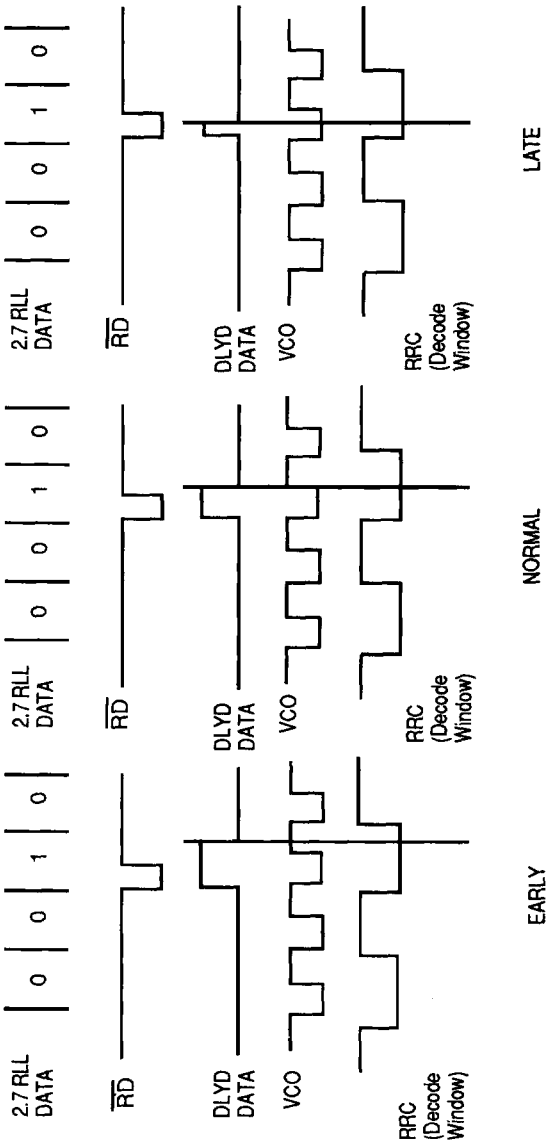
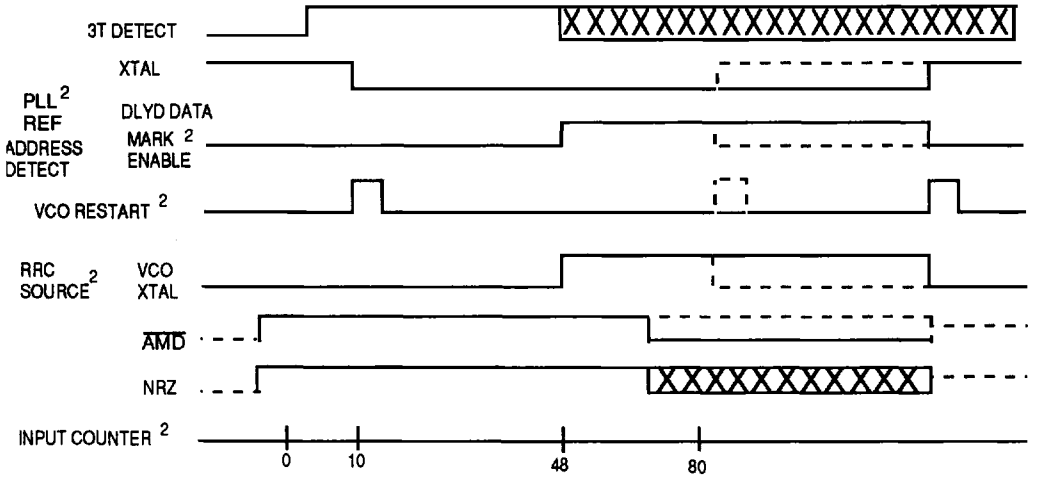



**Figure 2. Read Mode Delayed Data / VCO Phase Comparison**



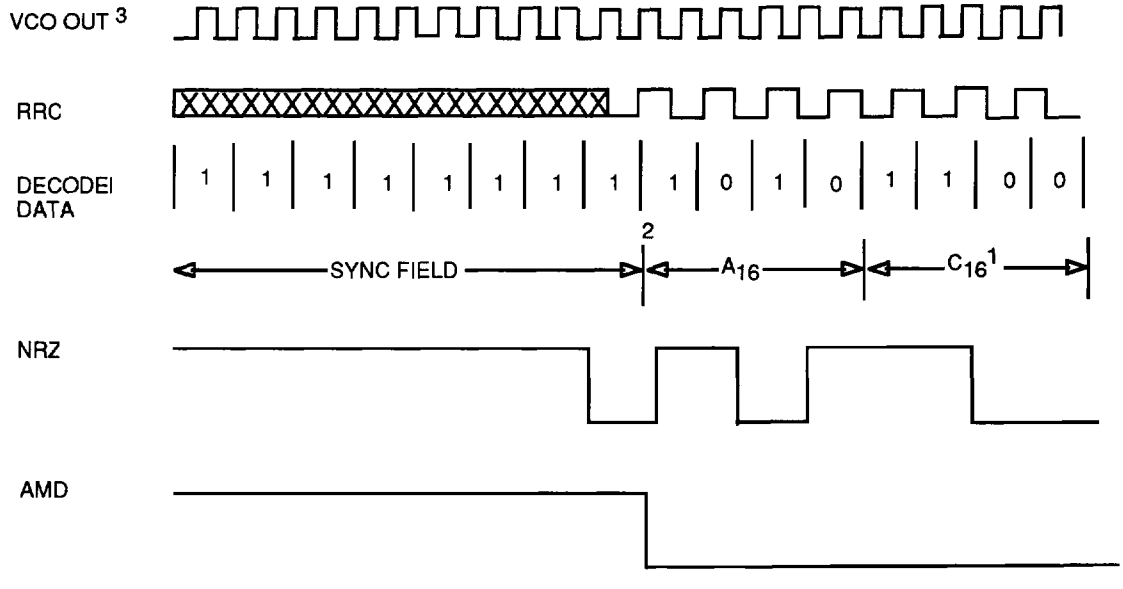

DLYD DATA width is adjusted by Window Shifting.
Width adjustment is exaggerated for clarity.

**Figure 3. Decode Window Shifting Using WS* Controls**



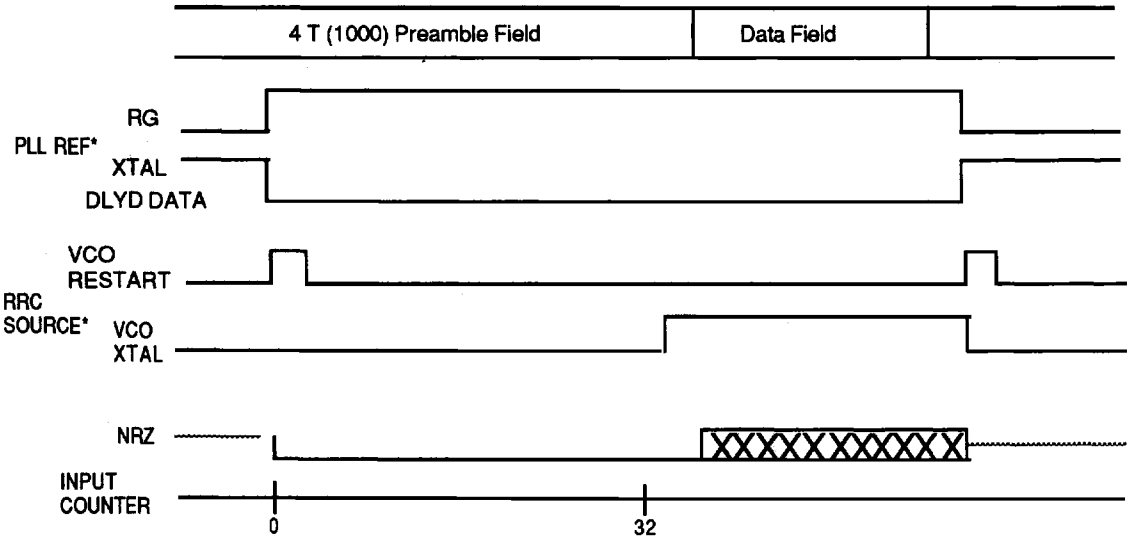

Notes:
1. Dashed lines represent conditions where the Address Mark was not found.
2. Representations of internal signals
3. Dotted lines represent a high impedance output state

**Figure 4. Read Mode Soft Sector Preamble Search and Address Mark Detection**



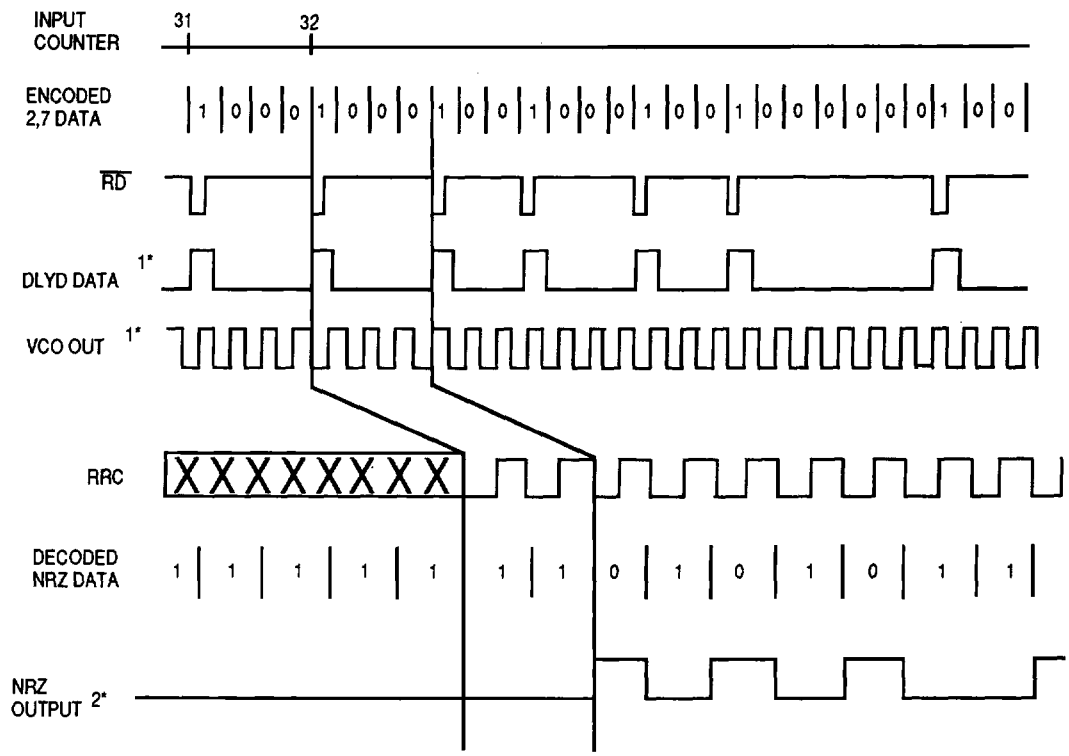

Notes: 1. These four bits can be any combination. C (1100) was selected in this example.
2. The $5E_{16}$ of the $5EAx_{16}$ Address Mark is not read back.
3. Internal signal

**Figure 5. Read Mode, Soft Sector Address Mark Detection**



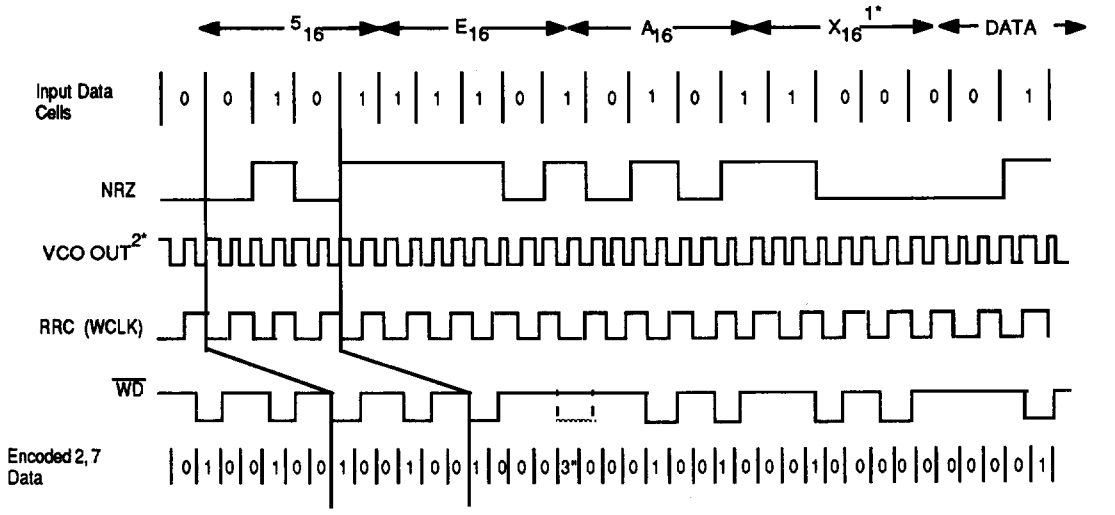

Note: Dashed lines represent a high impedance output state.
* - internal signal

**Figure 6. Read Mode Hard Sector PLL Acquisition Sequence**




Notes: *1. Representations of internal signals
*2. In hard sector mode the NRZ output is inverted

**Figure 7. Read Mode Hard Sector Read Reference Clock Switching**




Notes: *1. X16 can be any combination, C16 (1100) was selected in this example
*2. Representations of internal signals
*3. Deleted output pulse to encode Address Mark

**Figure 8 Write Mode Soft Sector Address Mark Write Data Encoding**

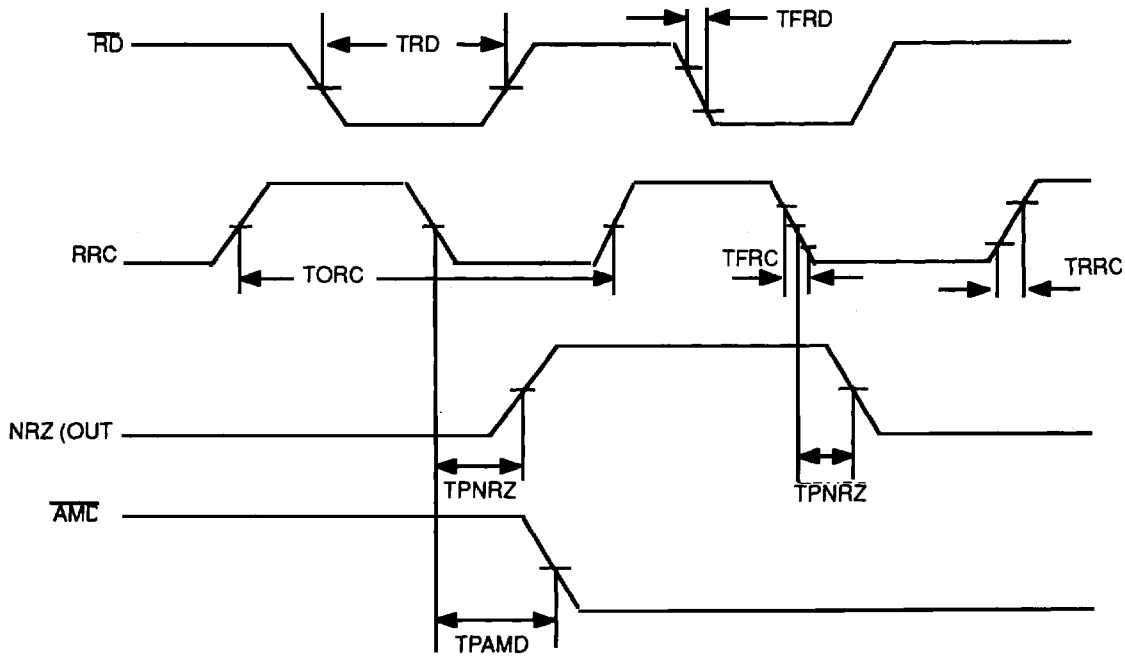



**Figure 9. Read Timing Definition**

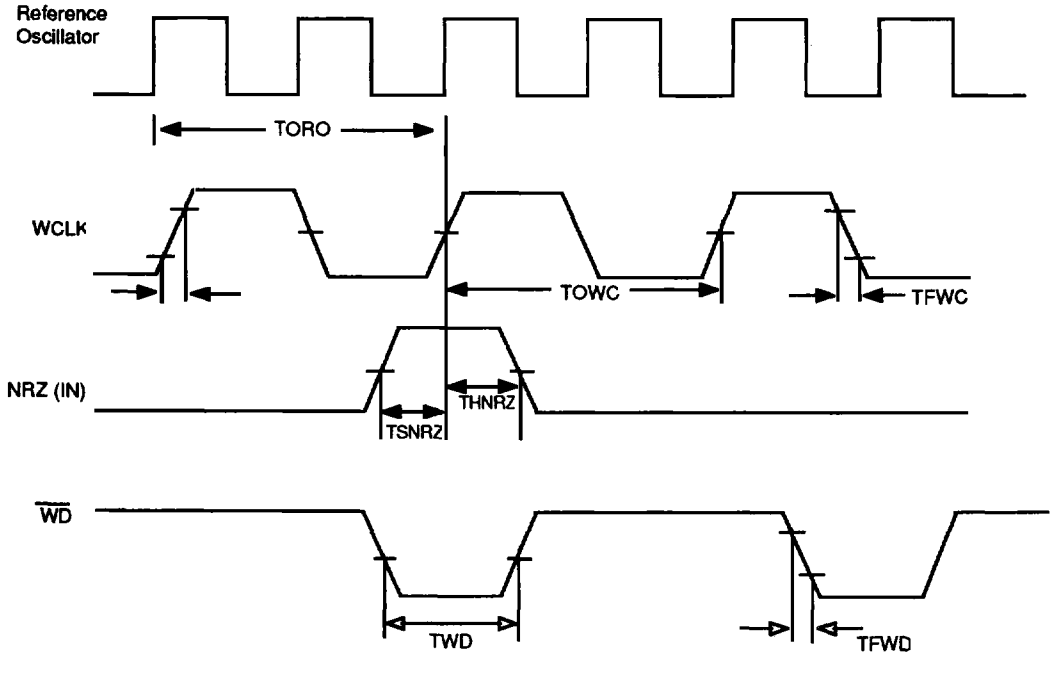



**Figure 10. Write Timing Definitions**

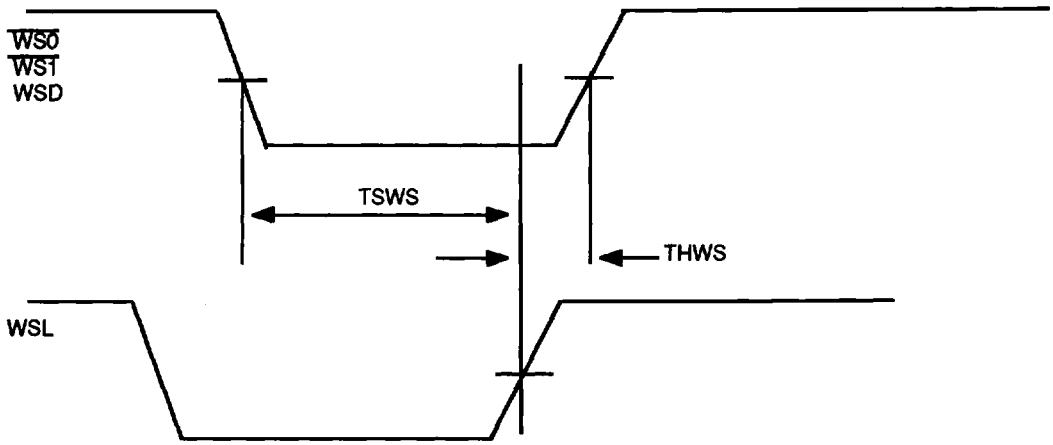
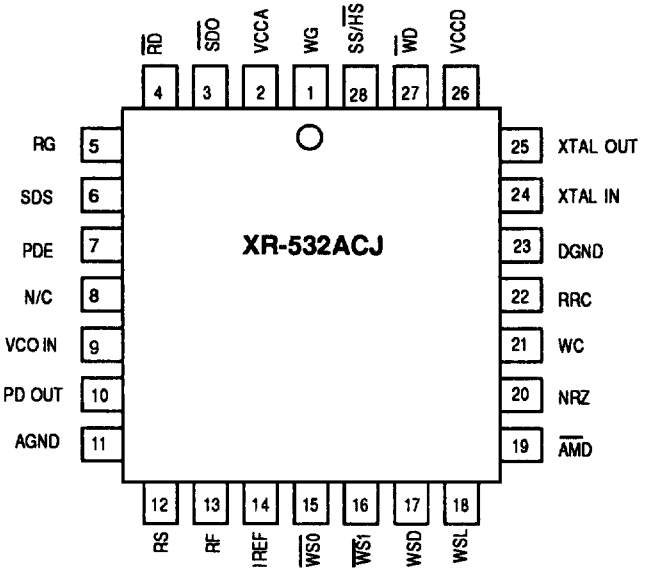
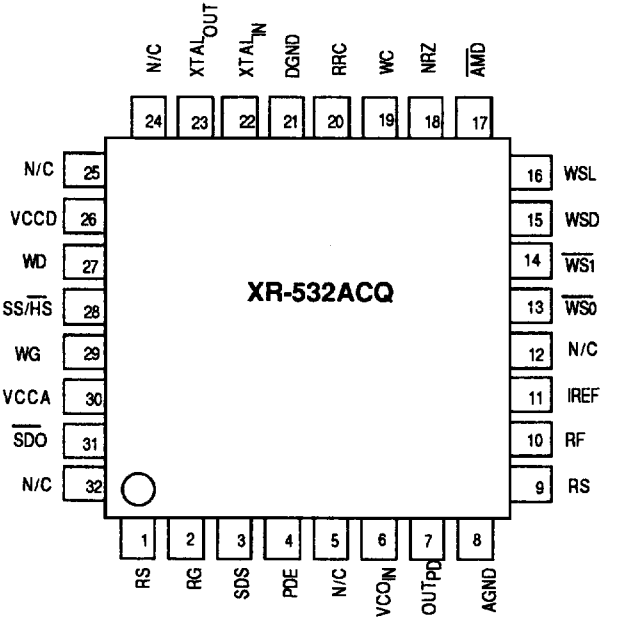



**Figure 11. Window Shift Controls Timing Definitions**


RD
SDO
VCCA
WG
SS/HS
WD
VCCD
4
3
2
1
28
27
26
RG 5
SDS 6
PDE 7
N/C 8
VCO IN 9
PD OUT 10
AGND 11
25 XTAL OUT
24 XTAL IN
23 DGND
22 RRC
21 WC
20 NRZ
19 AMD
XR-532ACJ
12
13
14
15
16
17
18
RS
RF
IREF
WS0
WS1
WSD
WSL


N/C
XTAL OUT
XTAL IN
DGND
RRC
WC
NRZ
AMD
24
23
22
21
20
19
18
17
N/C 25
VCCD 26
WD 27
SS/HS 28
WG 29
VCCA 30
SDO 31
N/C 32
16 WSL
15 WSD
14 WS1
13 WS0
12 N/C
11 IREF
10 RF
9 RS
XR-532ACQ
1
2
3
4
5
6
7
8
RS
RG
SDS
PDE
N/C
VCO IN
OUT PD
AGND