



**MOTOROLA**

**MC75461  
MC75462  
MC75463  
MC75464**

#### DUAL HIGH-VOLTAGE PERIPHERAL DRIVERS

The MC75461 thru MC75464 series is similar to the MC75451 thru MC75454 series peripheral drivers; however, the MC75461 series features greater voltage capability allowing operation with higher output voltages or with inductive loads. These devices are useful as lamp drivers, relay drivers, logic buffers, line drivers, or MOS drivers.

Each of these devices consists of a pair of MTTL gates with the output of each gate internally connected to the base of a transistor.

- MC75461 provides the AND function
- MC75462 provides the NAND function
- MC75463 provides the OR function
- MC75464 provides the NOR function

- 300 mA Output Current Capability
- No Output Latch-up at 30 V
- MTTL compatible Inputs

**DUAL HIGH-VOLTAGE  
PERIPHERAL DRIVERS  
SILICON MONOLITHIC  
INTEGRATED CIRCUITS**



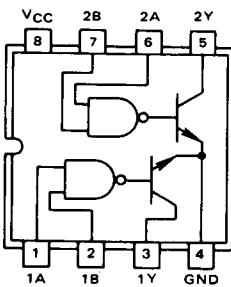
**U SUFFIX**  
CERAMIC PACKAGE  
CASE 693



**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626

**5**

**MC75461 – Positive AND**



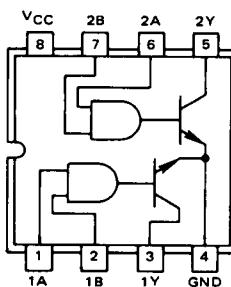
**TRUTH TABLE**

A	B	Y
L	L	L ("on" state)
L	H	L ("on" state)
H	L	L ("on" state)
H	H	H ("off" state)

H = high level, L = low level.

Positive Logic: Y = AB

**MC75462 – Positive NAND**



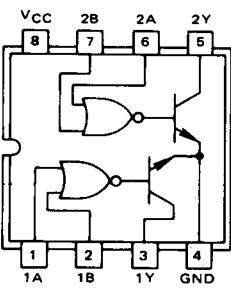
**TRUTH TABLE**

A	B	Y
L	L	H ("off" state)
L	H	H ("off" state)
H	L	H ("off" state)
H	H	L ("on" state)

H = high level, L = low level.

Positive Logic: Y =  $\overline{AB}$

**MC75463 – Positive OR**



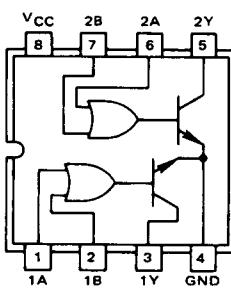
**TRUTH TABLE**

A	B	Y
L	L	L ("on" state)
L	H	H ("off" state)
H	L	H ("off" state)
H	H	H ("off" state)

H = high level, L = low level.

Positive Logic: Y = A + B

**MC75464 – Positive NOR**



**TRUTH TABLE**

A	B	Y
L	L	H ("off" state)
L	H	L ("on" state)
H	L	L ("on" state)
H	H	L ("on" state)

H = high level, L = low level.

Positive Logic: Y =  $\overline{A + B}$

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**MAXIMUM RATINGS ( $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  unless otherwise noted.)**

Rating	Symbol	Value	Unit
Power Supply Voltage(1)	$V_{CC}$	7.0	Vdc
Input Voltage	$V_I$	5.5	Vdc
Interemitter Voltage(2)	—	5.5	Vdc
Output Voltage(3)	$V_O$	35	Vdc
Output Current(4)	$I_O$	300	mA
Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $T_A = +25^\circ\text{C}$	$P_D$	830 6.6	mW mW/ $^\circ\text{C}$
Operating Ambient Temperature Range	$T_A$	0 to $+70$	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to $+150$	$^\circ\text{C}$

(1) Voltage values are with respect to network ground terminal.

(2) This is the voltage between two emitters of a multiple-emitter transistor.

(3) This is the maximum voltage which should be applied to any output when it is in the "off" state.

(4) Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

**ELECTRICAL CHARACTERISTICS** (Unless otherwise noted, specifications apply for  $4.75 \geq V_{CC} \geq 5.25$  V and  $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ )

Characteristic	Figure	Symbol	Min	Typ <sup>(1)</sup>	Max	Unit
Input Voltage - High Logic State	1,2	$V_{IH}$	2.0	—	—	Vdc
Input Voltage - Low Logic State	1,2	$V_{IL}$	—	—	0.8	Vdc
Input Clamp Voltage ( $V_{CC} = 4.75$ V, $I_I = -12$ mA)	4	$V_I$	—	-1.2	-1.5	Vdc
Output Current - High Logic State ( $V_{CC} = 4.75$ V, $V_{OH} = 35$ V, $V_{IH} = 2.0$ V) ( $V_{CC} = 4.75$ V, $V_{OH} = 35$ V, $V_{IL} = 0.8$ V)	2	$I_{OH}$	—	—	100	$\mu\text{A}$
Output Voltage - Low Logic State ( $V_{CC} = 4.75$ V, $V_{IL} = 0.8$ V) ( $V_{CC} = 4.75$ V, $V_{IH} = 2.0$ V) $I_{OL} = 100$ mA $I_{OL} = 300$ mA	1	$V_{OL}$	—	0.15 0.35	0.4 0.7	Vdc
Input Current - High Logic State ( $V_{CC} = 5.25$ V, $V_I = 2.4$ V) ( $V_{CC} = 5.25$ V, $V_I = 5.5$ V)	3	$I_{IH}$	—	—	40 1.0	$\mu\text{A}$ mA
Input Current - Low Logic State ( $V_{CC} = 5.25$ V, $V_I = 0.4$ V)	4	$I_{IL}$	—	-1.0	-1.6	mA
Power Supply Current - Output High Logic State ( $V_{CC} = 5.25$ V, $V_{IH} = 5.0$ V) ( $V_{CC} = 5.25$ V, $V_{IL} = 0$ ) ( $V_{CC} = 5.25$ V, $V_{IH} = 5.0$ V) ( $V_{CC} = 5.25$ V, $V_{IL} = 0$ )	5	$I_{CCH}$	—	8.0 13 8.0 14	11 17 11 19	mA
Power Supply Current - Output Low Logic State ( $V_{CC} = 5.25$ V, $V_{IL} = 0$ ) ( $V_{CC} = 5.25$ V, $V_{IH} = 5.0$ V) ( $V_{CC} = 5.25$ V, $V_{IL} = 0$ ) ( $V_{CC} = 5.25$ V, $V_{IH} = 5.0$ V)	5	$I_{CCL}$	—	61 65 63 72	76 76 76 85	mA

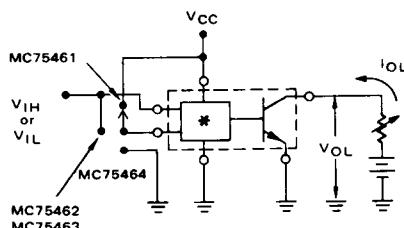
(1) Typical Values Measured with  $V_{CC} = 5.0$  V,  $T_A = 25^\circ\text{C}$

## TEST CIRCUITS

(Current into terminal is shown as a positive value.

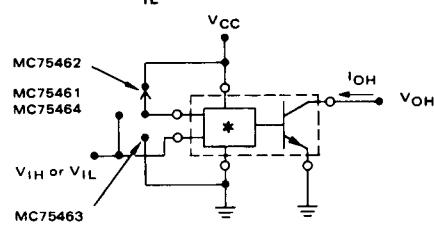
Arrows indicate actual direction of current flow.)

**FIGURE 1 -  $V_{OL}$**   
 **$V_{IH}$  - MC75462 and MC75464**  
 **$V_{IL}$  - MC75461 and MC75463**



\*See Page 1 for specific gate type.

**FIGURE 2 -  $I_{OH}$ ,  
 $V_{IH}$  - MC75461 and MC75463  
 $V_{IL}$  - MC75462 and MC75464**



Each input is tested separately.

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**SWITCHING CHARACTERISTICS** ( $V_{CC} = 5.0$  V,  $T_A = +25^\circ\text{C}$  unless otherwise noted.)

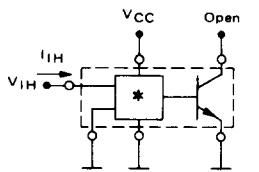
Characteristic	Symbol	Test Fig.	Min	Typ	Max	Unit
Propagation Delay Time ( $I_O \approx 200$ mA, $C_L = 15$ pF, $R_L = 50$ ohms) MC75461 Low-to-High-Level Output High-to-Low-Level Output	$t_{PLH}$ $t_{PHL}$	6	— —	45 30	55 40	ns
MC75462 Low-to-High-Level Output High-to-Low-Level Output	$t_{PLH}$ $t_{PHL}$	6	— —	50 40	65 50	ns
MC75463 Low-to-High-Level Output High-to-Low-Level Output	$t_{PLH}$ $t_{PHL}$	6	— —	45 30	55 40	ns
MC75464 Low-to-High-Level Output High-to-Low-Level Output	$t_{PLH}$ $t_{PHL}$	6	— —	50 40	65 50	ns
Transition Time ( $I_O \approx 200$ mA, $C_L = 15$ pF, $R_L = 50$ ohms) MC75461 Low-to-High-Level Output High-to-Low-Level Output	$t_{TLH}$ $t_{THL}$	6	— —	8.0 10	20	ns
MC75462 Low-to-High-Level Output High-to-Low-Level Output	$t_{TLH}$ $t_{THL}$	6	— —	12 15	25	ns
MC75463 Low-to-High-Level Output High-to-Low-Level Output	$t_{TLH}$ $t_{THL}$	6	— —	8.0 10	25	ns
MC75464 Low-to-High-Level Output High-to-Low-Level Output	$t_{TLH}$ $t_{THL}$	6	— —	12 15	20	ns
Output Voltage - High Logic Level after Switching (Latch-up Test) ( $V_S = 30$ V, $I_O \approx 300$ mA)	$V_{OH}$	7	$V_S-10$	—	—	mV

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## TEST CIRCUITS (Continued)

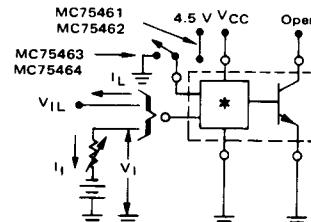
(Current into terminal is shown as a positive value.  
Arrows indicate actual direction of current flow.)

FIGURE 3 –  $I_{IH}$   
(ALL DEVICE TYPES)



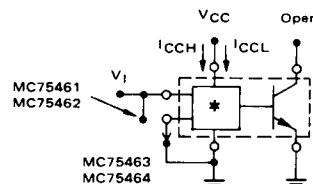
Each input is tested separately.

FIGURE 4 –  $I_{IL}, V_I$   
(ALL DEVICE TYPES)



Each input is tested separately.

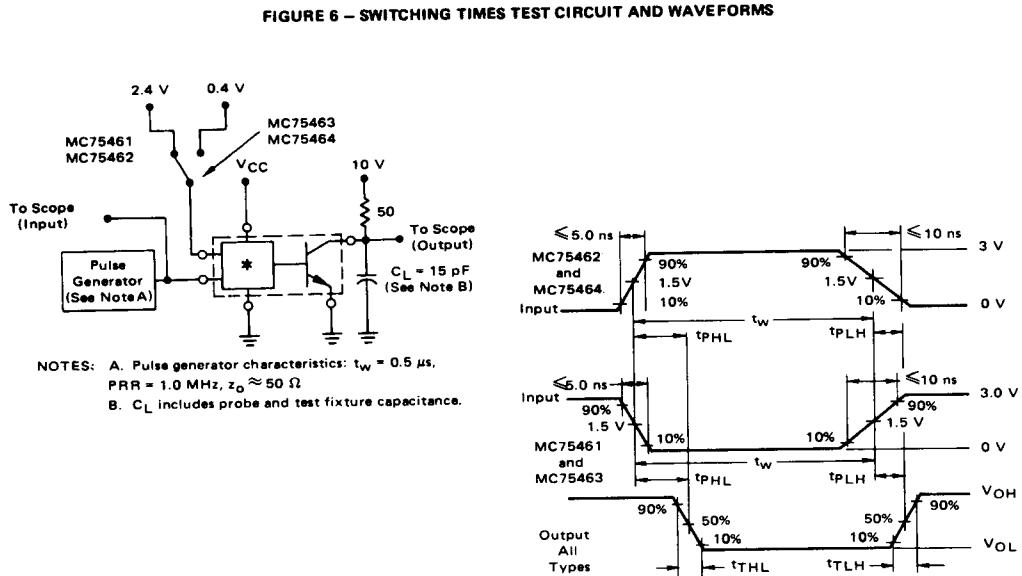
FIGURE 5 –  $I_{CCH}, I_{CCL}$   
(ALL DEVICE TYPES)



\*See page 1 for specific gate type.

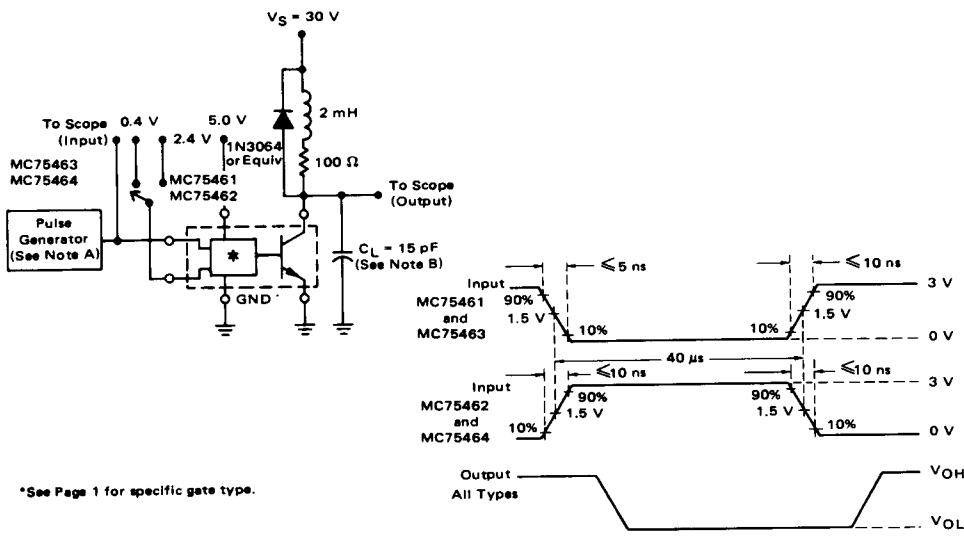
Both gates are tested simultaneously.

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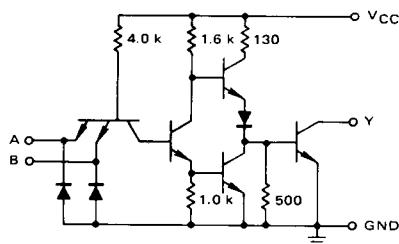
FIGURE 7 – OUTPUT VOLTAGE AFTER SWITCHING TEST CIRCUIT AND WAVEFORMS  
(LATCH-UP TEST)



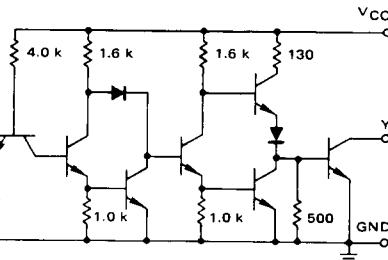
# MC75461, MC75462, MC75463, MC75464

## REPRESENTATIVE SCHEMATIC DIAGRAMS (1/2 Circuits Shown)

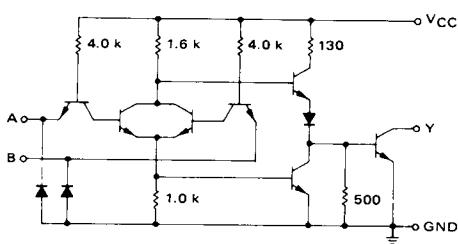
MC75461



MC75462



MC75463



MC75464

