XR-2900 Fax/Data Modem Chip Set

GENERAL DESCRIPTION

The XR-2900 is a two chip set that provides the modem data pump function for 9600 BPS half duplex / 2400 BPS full duplex applications. The XR-2900 supplies all the functions for implementing a modem for facsimile or V.29 applications. Also included is a complete V.22 bis data modem.

The XR-2901 is a digital signal processor-based chip supporting primarily the modulation/demodulation function. The XR-2902 is a combination analog and digital chip. Its analog portions support the transmit and receive filters, A/D and D/A functions, transmit level attenuator, and programmable gain amplifier.

The digital portion of the XR-2902 supports the transmit clock, and async/sync converter, interface circuit between XR-2901 and host controller, and a receive clock digital phase locked loop.

Both chips utilize CMOS technology for low power operation. The XR-2901 and XR-2902 are available in 40 and 48 pin dip, 44 and 52 pin PLCC and 44 and 52 pin QFP packages respectively. Power required is a single +5 volt for the XR-2901 and ±5 volts for the XR-2902.

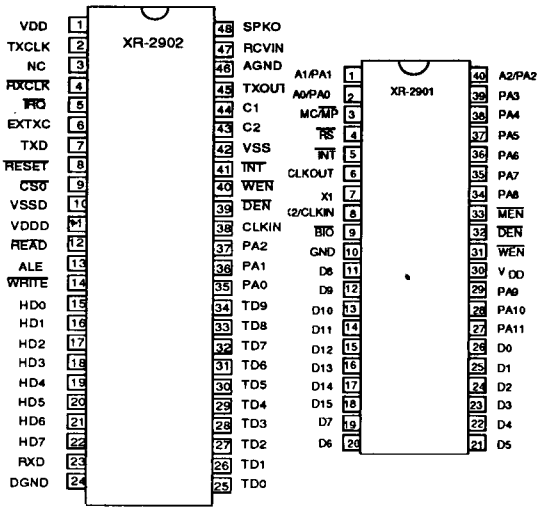
FEATURES

V.29 / V.27ter / V.21 Ch. 2 Fax Modes
V.22bis / V.22 / 212A / 103 Data Modes
Standard Microcontroller Interface
Analog, Remote and Local Digital Test Facilities
DTMF Generator
9600 / 7200 / 4800 / 2400 / 300 BPS Half Duplex Operation
2400 / 1200 / 300 BPS Full Duplex DATA Mode
CMOS Technology
Automatic Adaptive Equalization
Guard Tone Generators
Call Progress Monitor Mode

APPLICATIONS

V.29 Modems
Fax Machine Modem
PC Fax/Data Modem
Hayes Compatible Modems

PIN ASSIGNMENT



(For other pin assignments refer to the end of this datasheet)

ORDERING INFORMATION

Part Number.	Package	Operating Temperature
XR-2901CP	Plastic DIP	0°C to 70°C
XR-2901CJ	PLCC	0°C to 70°C
XR-2901CQ	QFP	0°C to 70°C
XR-2902CP	Plastic DIP	0°C to 70°C
XR-2902CJ	PLCC	0°C to 70°C
XR-2902CQ	QFP	0°C to 70°C

ABSOLUTE MAXIMUM RATINGS

V_{DD}	-0.3 to 7V
V_{SS}	0.3 to -7V
Input Voltage	V_{SS} -0.7V to V_{DD} +0.3V
Power Dissipation *(package limitation)*	
Plastic	1 watt
Derate above +25°C	5 mw/°C
Storage Temperature Range	-65°C to 150°C

ELECTRICAL CHARACTERISTICS: XR-2901 Test Conditions: T_A = 25°C, V_{DD} = 5V ± 5%, GND =0VDC, CLKIN = 20.2752MHz ±0.01%, unless otherwise specified

DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
I_{DD}	Positive Supply Current		45	70	mA	
V_{IL}	Low Level Input Voltage			0.8	V	All inputs except MC/$\overline{MP}$
				0.6	V	MC/$\overline{MP}$ input
V_{IH}	High Level Input Voltage	2.0			V	All inputs except X2/CLKIN
		3.0			V	X2/CLKIN
I_I	Input Current			±20	µA	All inputs except X2/CLKIN
				±50	µA	X2/CLKIN
V_{OH}	High Level Output Voltage	2.4	3.0		V	I_{OH} = 300µA
V_{OL}	Output Logic Low voltage		0.3	0.5	V	I_{OL} = 2mA
I_{OH}	High Level Output Current			-300	µA	
I_{OL}	Low Level Output Current			2	mA	

ELECTRICAL CHARACTERISTICS : XR-2902 Test Conditions: V_{DD} = 5 VDC ± 5%. V_{SS} =-5 VDC ± 5%, T_A = 25°C, CLKIN = 5.0688MHz ±0.01% unless otherwise specified.

DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
I_{DD}	Positive Supply Current		15	25	mA	
	PWRD Mode			5	mA	
I_{SS}	Negative Supply Ciurrent		-15	25	V	
V_{IL}	Low Level Input Voltage			0.8	V	
V_{IH}	High Level Input Voltage	2.0			V	
I_I	Input Current			10	µA	
V_{OH}	Output Logic High Voltage	3.0			V	I_{OH} = 300µA
V_{OL}	Output Logic Low Voltage			0.4	mA	I_{OH} = 2mA
I_{OH}	Logic High Output Current		-300		µA	
I_{OL}	Logic Low Output Current		1.6		mA	

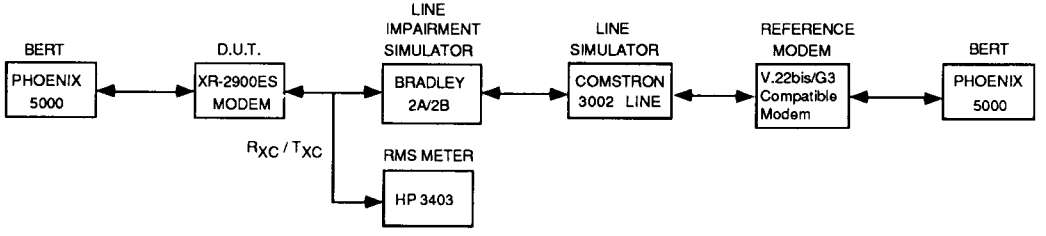
SYSTEM DESCRIPTION

The XR-2901/2902 chip set provides the complete data pump function for both G3 9600 BPS fax, as well as V.22bis data modes of operation. A complete microcontroller interface for popular devices such as 8031 types, is also included.

For fax modes of operation, fallback from 9600 BPS to 7200 BPS, 4800 BPS, or 2400 BPS is provided for poor line quality conditions. Data mode operation provides high compatibility with 2400 BPS, as well as 1200 BPS and 300 BPS modems.

AC CHARACTERISTICS *Refer to Figure 1, (ADD = Address)*

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
T_{ALE}	Address Latch Enable Pulse Width	100			ns	
T_{LCM}	Minimum Latch to READ/WRITE Control	60			ns	
T_{READ}	Read Pulse	0		160	ns	
T_{RWL}	READ/WRITE Control to Latch	20			ns	
T_{WRITE}	Write Pulse Width	.140		25	µs	
T_{AL}	ADD/CS Set-up Before ALE	40			ns	
T_{LAH}	ADD/CS Hold After Latch	40			ns	
T_{DRD}	Valid Data From READ	0		140	ns	
T_{DAR}	Data Held After READ	0		200	ns	
T_{WS}	Write Data Set-up After WRITE	150			ns	
T_{DHAW}	Data Hold After WRITE	40			ns	
TRANSMITTER POWER LEVELS						
TX_{CAR}	Transmit Carrier Power	-.6			dBm	QAM, DPSK, FSK Modulation
$TX_{CAR\ 550}$	550 Hz Guard Tone Power	-1.7		-.4	dBm	GTE=1, GTS=0
$TX_{CAR1800}$	1800Hz Guard Tone Power	-5.2		-3.4	dBm	GTE=1, GTS=1
SYSTEMS SPECIFICATIONS *See Performance Test Set-Up*						
DYNMC	Dynamic Range Min Limits	-43			dBm	
S/N V.22bis	Signal-to-Noise Ratio for V.22bis		17		dB	2400BPS operation BER ≤ $1/10^{-5}$
S/N V.29	Signal-to-Noise Ratio for V.29 (9600BPS)		23		dB	9600BPS operation BER ≤ $1/10^{-5}$
PCD	Carrier Detect Level		-43		dBm	
CDHYT	Carrier Detect Hysteresis		3		dB	



Performance Test Set-Up

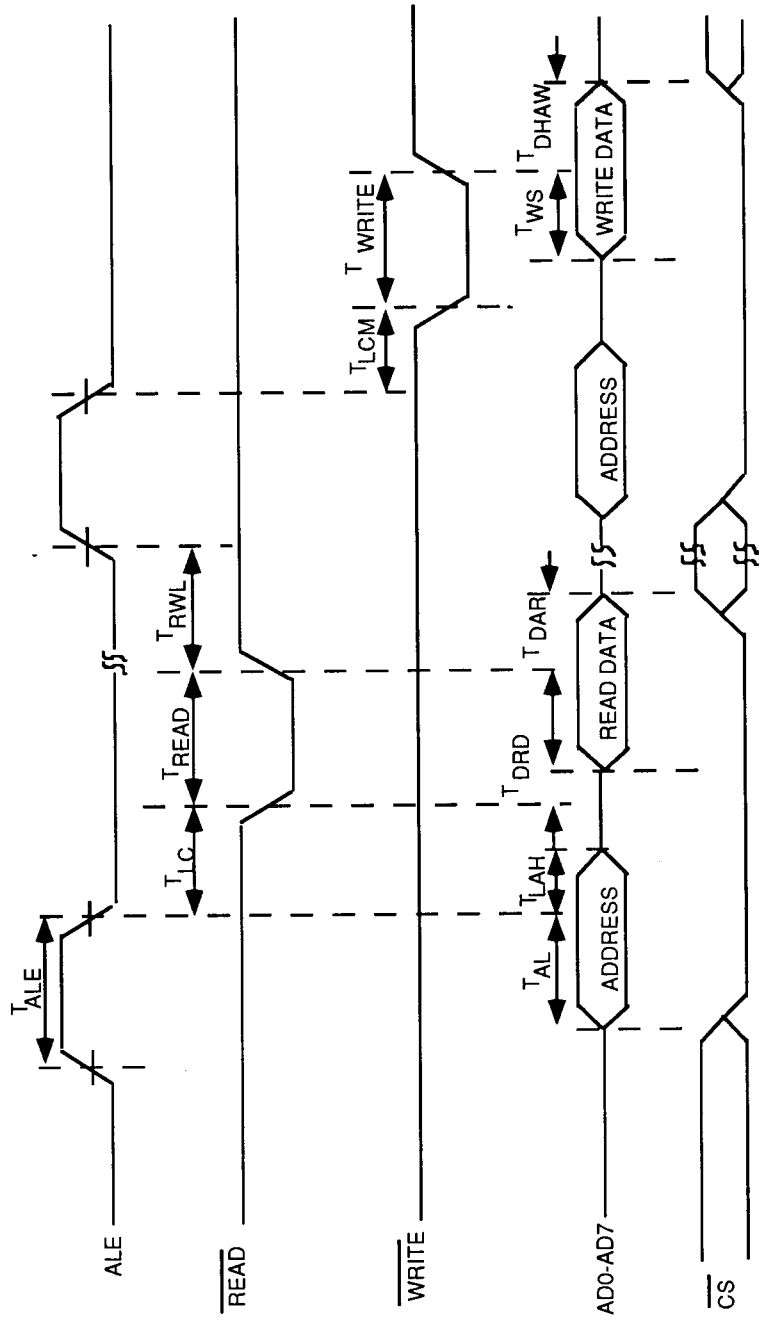
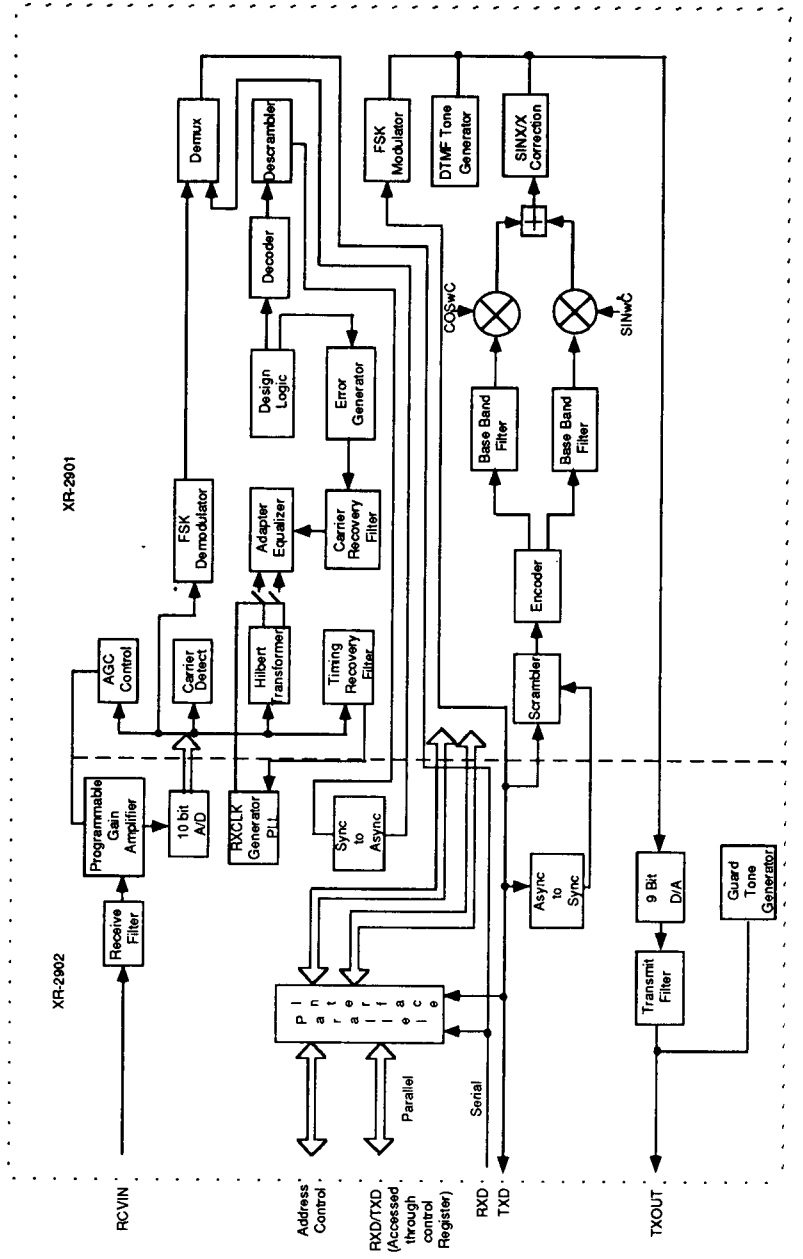


Figure 1. A.C. Timing Diagram



*Actually in XR-2902, shown in XR-2901 for Simplicity

Figure 2. Equivalent Block Diagram

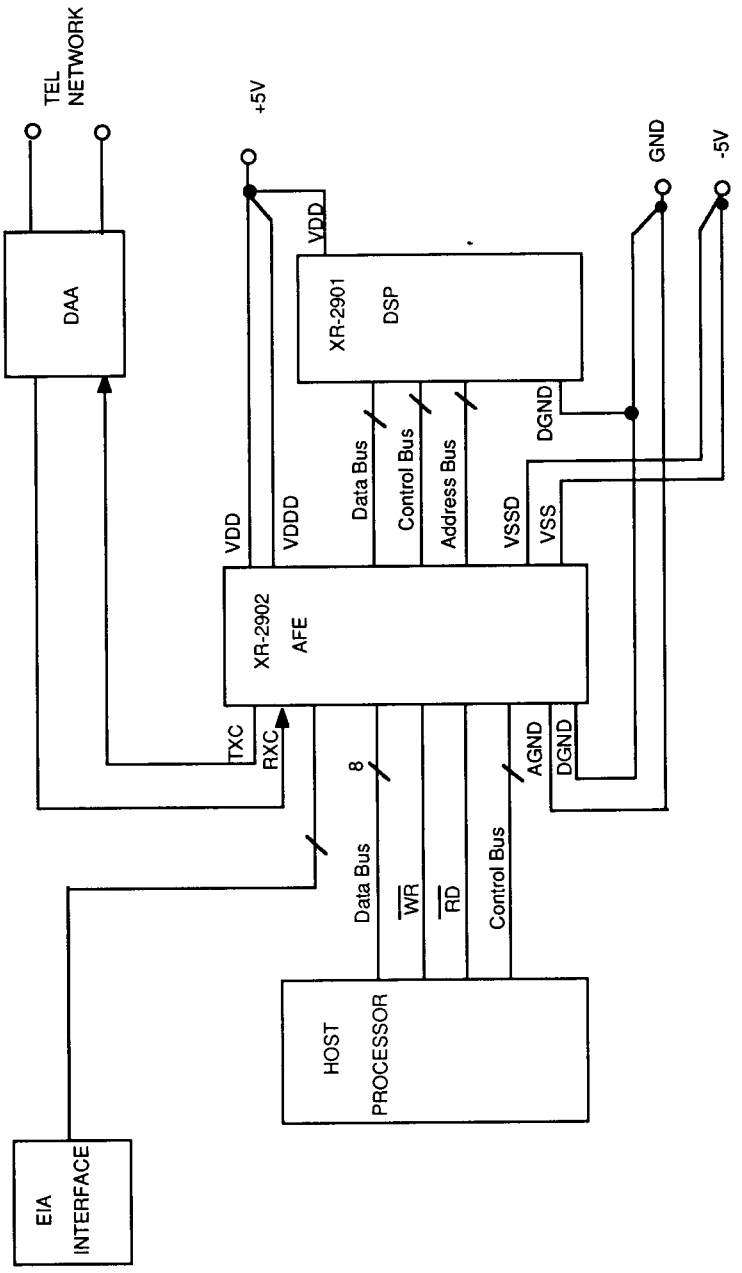


Figure 3. XR-2900 Generalized system Connection

PIN DESCRIPTIONS: XR-2901 *(DIP Package Pin Numbers)*

Pin #	Symbol	I/O	Description
1,2,40	A0/PA0-A2/PA2	I/O	Input/Output Port Address
3	MC/$\overline{MP}$	I	Micro-controller/Micro-processor control input
4	$\overline{RS}$	I	$\overline{RESET}$, used to initialize the device.
5	$\overline{INT}$	I	External Interrupt Input
6	CLKOUT	O	Clock Output equal to 1/4 of master 20.2752MHz clock (5.0688MHz)
7	X1	O	Crystal Oscillator Output
8	X2/CLKIN	I	Crystal Oscillator Input / External Clock Input
9	$\overline{BIO}$	I	Polling Input
10	GND	I	Ground
11-18	D8-D15	I/O	Data Lines 8-15
19-26	D7-D0	I/O	Data Lines 7-0
27-29	A11-A9	O	Address Lines 11-9
30	VDD	I	Positive Power Supply Input (+5 Volt)
31	$\overline{WEN}$	O	$\overline{Write\ Enable}$ Output
32	$\overline{DEN}$	O	$\overline{Data\ Enable}$ Output
33	$\overline{MEN}$	O	$\overline{Memory\ Enable}$ Output
34-39	A8-A3	O	Address Lines 8-3

PIN DESCRIPTIONS: XR-2902 *(DIP Package Pin Numbers)*

Pin #	Symbol	I/O	Description
1	VDD	I	Positive Analog Power Supply Input (+5 V)
2	TXCLK	O	Transmit Clock Output
3	NC		
4	$\overline{RXCLK}$	O	Receive Clock Output
5	$\overline{IRQ}$	O	Interrupt Request. Open collector type output
6	EXTXC	I	External Transmit Clock Input
7	$\overline{TXD}$	I	$\overline{Serial\ Transmit\ Data\ Input}$
8	$\overline{RESET}$	I	$\overline{Reset\ Input}$
9	$\overline{CS0}$	I	$\overline{Chip\ Select\ Input}$
10	VSSD	I	Negative Digital Power Supply Input (-5Volt)
11	VDDD	I	Positive Digital Power $\underline{Supply\ Input}$ (+5 Volt)
12	$\overline{READ}$	I	$\overline{Read\ Enable\ Input}$
13	ALE	I	Address Latch Enable Input
14	$\overline{WRITE}$	I	$\overline{Write\ Enable\ Input}$
15-22	HD0-HD7	I/O	Address/Data Bus Input / Output
23	RXD	O	Serial Receive Data Output, Open Collector
24	DGND	I	Digital Ground
25-34	TD0-TD9	I/O	DSP Data Bus
35-37	PA0-PA2	I/O	Port Address Input / Output
38	CLKIN	I	Master Clock Input. 5.0688MHz
39	$\overline{DEN}$	I	$\overline{Data\ Enable\ Input}$
40	$\overline{WEN}$	I	$\overline{Write\ Enable\ Input}$
41	$\overline{INT}$	O	Interrupt Output
42	VSS	I	Negative Analog Power Supply Input (-5 Volt)
43	C2	I	AGC Input
44	C1	O	AGC Output
45	TXOUT	O	Transmit Carrier Output
46	AGND	I	Analog (Signal) Ground
47	RCVIN	I	Receive Carrier Input
48	SPKO	O	Speaker Output

MODES OF OPERATION

The XR-2900 supports various modes of operation for both fax and data standards, as shown in figure 4.

FAX (Half Duplex)		DATA (Full Duplex)	
Standard	Data Rate (BPS)	Standard	Data Rate (BPS)
V.29	9600	V.22bis	2400
	7200	V.22	1200
		*212A	1200
V.27ter	4800	*103	300
	2400		
**V.21 Ch.2	300		

**Bell Standard, all others are CCITT.*
***Used only for signalling, not a data mode.*

Figure 4. XR-2900 Fax/Data Modes

To support the various standards and speeds, as shown in Figure 5, three different modulation schemes are utilized:

- FSK Frequency Shift Keying
  -Two discrete frequencies are used to represent binary data.
- PSK Phase Shift Keying
  -Phase changes in a constant fre quency carrier represent data to be transmitted.
- QAM Quadrature Amplitude Modulation
  -Both phase and amplitude modula tion of a constant frequency carrier are used to represent data to be transmitted.

These different modulation schemes are necessary due to phone line bandwidth limitations. As data rates increase, each discrete change (frequency/phase/amplitude) is used to represent groups of data. The changes are known as baud, the rate of change being the modems baud rate. Figure 5 shows the relationship between the actual data transfer rate in bits per second (BPS) and baud rate. The data encoding indicates how many bits of data are represented by each baud change.

Mode	Data Rate (BPS)	Baud Rate	Data Encoding	Modulation Scheme	Carrier Frequency (Hz)	*Transmit CarrierShaping
V.29	9600	2400	Quadbit	QAM	1700	20%
V.29	7200	2400	Tribit	QAM	1700	20%
V.29	4800	2400	Dibit	QAM	1700	20%
V.27ter	4800	1600	Tribit	PSK	1800	50%
V.27ter	2400	1200	Dibit	PSK	1800	90%
V.22bis	2400	600	Quadbit	QAM	1200/2400	75%
V.22	1200	600	Dibit	PSK	1200/2400	75%
212A	1200	600	Dibit	PSK	1200/2400	75%
103	300	300	-	FSK	1070/1270 2025/2225	-
V.21	300	300	-	FSK	980/1180 1650/1850	-

**Square root raised cosine shaping*

Figure 5. Data/Baud Rate Relationships

Modem baud changes may be shown as a signal constellation, illustrating possible combinations. Figure 6 illustrates the constellations for various modes of operation (not to scale).

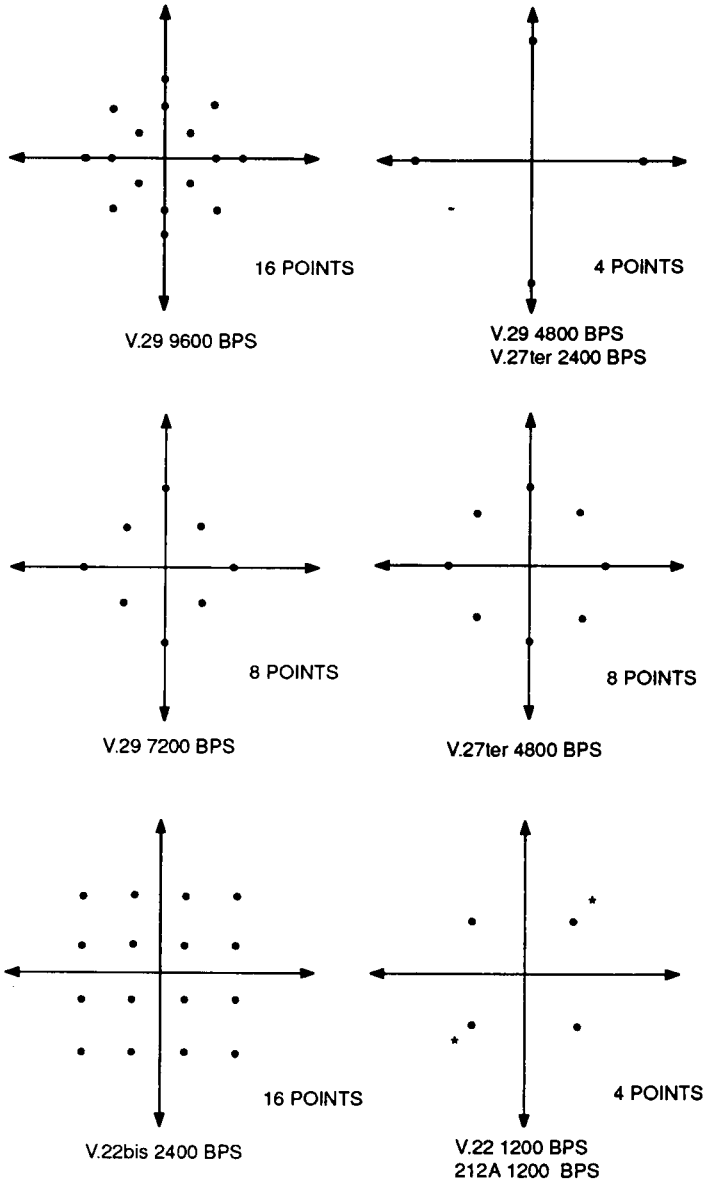


Figure 6. Signal Constellations
(FSK constellation will be two point, not to scale)*

The XR-2900 must generate several different tones to provide the necessary handshaking, guard tones, and other functions. Figure 7 lists these tones and related accuracy.

TONE (Hz)	FUNCTION	ACCURACY (%)
462	Procedure Interrupt	0.01
550/1800	Guard Tones	0.1
1100	Line Conditioning Signal/Calling Tone	0.01
2100	Answer Tone	0.1

Figure 7. Tone Generator Frequencies/Accuracy

REGISTER DESCRIPTION

The XR-2900 utilizes a set of 32, 8 bit, registers for controlling fax or data functions. A register plane is selected and then various modes/functions within that plane are programmed for fax or data operation. The MCFN bit is used for programming fax or data mode. A reset input will automatically default to the data plane.

REGISTERS FOR FAX OPERATION - INTERFACE MEMORY *(Refer to Figure 9)*

REGISTER	BIT(S)	SYMBOL	R/W	DESCRIPTION
0:0	0-7	TXRXD	R/W	**TRANSCEIVER DATA:** Provides input for transmit data or output for receive data.
0:1	0-7	RESERVED		
0:2	0-7	FREQL	R/W	**RAM DATA/FREQUENCY SELECT LOW ORDER BYTE:** Low order byte of tone generator select.
0:3	0-7	FREQM	R/W	**RAM DATA/FREQUENCY SELECT HIGH ORDER BYTE:** High order byte of tone generator select. To enable the tone transmit mode, register 4, modem configuration must be set to Hex 80. The tone generator is controlled by a 16 bit, two byte, word written to the FREQL and FREQM reg isters from the host processor. The control word, N, repre sents the desired frequency by the relationship: $$N = \frac{\text{Frequency}}{0.14648}$$ Below commonly used tones and the Hexadecimal num bers which are written to the FREQL/FREQM registers are listed.

Frequency (Hz)	FREQM	FREQL
462	0C	52
1100	1D	55
1650	2C	00
1850	31	55
2100	38	00

REGISTER	BIT(S)	SYMBOL	R/W	DESCRIPTION

DTMF tone generation mode is selected by setting the modem configuration register to Hex 81. Tone pairs are then controlled by bits 0-3 of register 2, as shown below:

Dial Digit	Register Value D3	D2	D1	D0	Tone Pairs fLow(Hz)	fHigh(Hz)
0	0	1	1	1	941	1336
1	0	0	0	0	697	1209
2	0	1	0	0	697	1336
3	1	0	0	0	697	1477
4	0	0	0	1	770	1209
5	0	1	0	1	770	1336
6	1	0	0	1	852	1477
7	0	0	1	0	852	1209
8	0	1	1	0	852	1336
9	1	0	1	0	852	1477
*	0	0	1	1	941	1209
#	1	0	1	1	941	1477
A	1	1	0	0	697	1633
B	1	1	0	1	770	1633
C	1	1	1	0	852	1633
D	1	1	1	1	941	1633

0:4 0-7 MCFN R/W **MODEM CONFIGURATION:** This register provides mode control. This value, when the set up bit is set, controls the XR-2900 mode of operation. Figure 8 shows the mode/ register value relationship.

MCFN, Register 4, Bits 7	6	5	4	3	2	1	0	Hex	Mode
0	0	0	1	0	1	0	0	14	V.29 9600 BPS
0	0	0	1	0	0	1	0	12	V.29 7200 BPS
0	0	0	1	0	0	0	0	11	V.29 4800 BPS
0	0	0	0	1	0	1	1	0A	V.27ter 4800 BPS
0	0	0	0	1	0	0	1	09	V.27ter 2400 BPS
0	0	1	0	0	0	0	0	20	V.21 300 BPS
1	0	0	0	0	0	0	0	80	Tone Transmit
1	0	0	0	0	0	0	1	81	DTMF Tones Transmit
0	1	1	0	0	0	0	1	61	Bell 103 300 BPS
0	1	1	0	0	0	1	0	62	V.22bis/Bell 212A

Figure 8. Mode Programming

0:5 0-1 RESERVED

2 SQEXT R/W **SQUELCH EXTEND:** When set, receive carriers are gated out for 130mS after the transmitter is turned off.

3 EPT R/W **ECHO PROTECTION TONE:** When set, an unmodulated carrier (frequency determined by modem configuration register) is transmitted for 185mS, followed by 20mS of quiet, and then the normal training sequence.

4 RESERVED

REGISTER	BIT(S)	SYMBOL	R/W	DESCRIPTION
	5	RAMW	R/W	**RAM WRITE:** This bit is set when a write routine to the diagnostic RAM is needed. This bit will be reset when a diagnostic read routine is executed.
	6	TDIS	R/W	**TRAINING DISABLED:** When set, the modem goes directly to receive mode, bypassing the training sequence. If the modem is transmitting the training sequence will not occur at the start of transmission.
	7	RTS	R/W	**REQUEST TO SEND:** When set, the transmit sequence is initiated.
0:6	0-7	RESERVED		
0:7	0-3	RESERVED		
	4	RCVG	R/W	**RECEIVE FILTER GAIN CONTROL:** An additional 10dB of receive path gain (13dB for fax) can be selected by reset ting this bit. When set, fax 3dB of gain is selected for high receive level applications, such as leased line.
	5-7	RESERVED		
0:8	0-5	RESERVED		
	6	CTS	R	**CLEAR TO SEND:** When low, indicates the XR-2900 is ready to send (transmit) data.
	7	RESERVED		
0:9	0-7	RESERVED		
0:A	0-3	RESERVED		
	4	SPC	R/W	**SPEAKER CONTROL:** When set, the speaker output is enabled.
	5	VOL 1	R/W	**VOLUME CONTROL 1:** See Volume Control 2 for description.
	6	VOL 2	R/W	**VOLUME CONTROL 2:** These two bits, Vol 1/Vol 2, con trol the signal amplitude at the speaker output, as shown below:

Vol 1	Vol 2	Relative Level
0	0	Low
0	1	Low
1	0	Medium
1	1	Maximum

	7	RESERVED		
0:B	0-7	RESERVED		
0:C	0-7	RESERVED		
0:D	0-3	TXL 1-4	R/W	**TRANSMIT LEVEL CONTROL:** These four bits control the transmit carrier level, as shown below. The values list ed are attenuations from nominal transmitter output.

TXL4	TXL3	TXL2	TXL1	TXOUT Attenuation(dB)
0	0	0	0	-15
0	0	0	1	-14
0	0	1	0	-13
0	0	1	1	-12
0	1	0	0	-11
0	1	0	1	-10
0	1	1	0	-9

REGISTER	BIT(S)	SYMBOL	R/W	DESCRIPTION
				0 1 1 1 -8 1 0 0 0 -7 1 0 0 1 -6 1 0 1 0 -5 1 0 1 1 -4 1 1 0 0 -3 1 1 0 1 -2 1 1 1 0 -1 1 1 1 1 -0
	4	RDEQ	R/W	**DELAY EQUALIZER ENABLE:** When set, a delay equalizer is enabled for compensating the telephone line characteristics.
	5	CAB 1	R/W	**CABLE EQUALIZER CONTROL 1:** See CAB 2.
	6	CAB 2	R/W	**CABLE EQUALIZER CONTROL 2:** CAB 1/CAB 2 control the cable equalizer amplitude compensation, as shown below:

CAB 1	CAB2	Length
0	0	0.0 Meters
0	1	1.8 Km
1	0	3.6 Km
1	1	7.2 Km

	7	RESERVED		
0:E	0	MDAO	R	**MODEM DATA AVAILABLE:** When high, data is ready for host processor to read or write data to register 0, during parallel data mode.
	1	RESERVED		
	2	IEO	R/W	**INTERRUPT ENABLE:** When set, the IRQ output will be set low, assuming MDA0 bit is set to a high.
	3	SETUP	R/W	**SETUP:** This bit must be set whenever a change is made to register 4. After configuration change is complete, this bit will be reset automatically.
	4-6	RESERVED		
	7	IAO	R	**INTERRUPT ACTIVE:** This bit will be set when IRQ is active
0:F	0-6	RMAA	W	**RAM ACCESS ARRANGEMENT:** This register is used to read various diagnostic functions from the XR-2901. The process of reading the functions is described in data plane, register 0:F (Bits 0-6).
	7	PDM	R/W	**PARALLEL DATA MODE:** When set, the modem is put in parallel data mode and the diagnostic RAM cannot be read.
1:0	0-7	RESERVED		
1:1	0-7	RESERVED		
1:2	0-7	RESERVED		
1:3	0-7	RESERVED		
1:4	0-1	RESERVED		
	2	$\overline{\text{P2DET}}$	R	**P2 DETECTION:** This bit, when low, indicates that the P2 pattern has been received.
	3-7	RESERVED		
1:5	0-5	RESERVED		
	6	$\overline{\text{FED}}$		True Energy Detect
	7	RESERVED		

REGISTER	BIT(S)	SYMBOL	R/W	DESCRIPTION
1:6	0-7	RESERVED		
1:7	0	$\overline{\text{CDET}}$	R	**CARRIER DETECT:** When low, indicates the presence of a received signal within the passband of the received filters. $\overline{\text{CDET}}$ will remain high during a training sequence. CDET will go low at the start of data state and return to a one at the end of the receive signal.
	1-5	RESERVED		
	6	$\overline{\text{PNDET}}$	R	**PN DETECT:** When low, the PN sequence has been detected during the training sequence.
	7	RESERVED		
1:8	0-7	RESERVED		
1:9	0-7	RESERVED		
1:A	0-7	RESERVED		
1:B	0-4	RESERVED		
	5	FR1	R	**FREQUENCY 1 DETECT:** When high, a 2100 Hz tone has been detected. This register is only active if V.21 mode has been set.
	6	FR2	R	**FREQUENCY 2 DETECT:** When high, a 1100 Hz tone has been detected.
	7	FR3	R	**FREQUENCY 3 DETECT:** When high, a 462 Hz tone has been detected.
1:C	0-7	RESERVED		
1:D	1	$\overline{\text{FRT}}$	R/W	**FREEZE TAPWEIGHTS:** This bit, when reset, freezes the last positions of the tapweights of the adaptive equalizer. This bit can be used to compensate for a momentary loss of receive carrier in fax reception.
	0,2-7	RESERVED		
1:E	0-7	RESERVED		
1:F	0-7	RESERVED		

REGISTERS FOR DATA MODE OPERATION - Modem Register Plane.
Refer to Figure 10. NOTE 1: See fax register for description.

REGISTER	BIT(S)	SYMBOL	R/W	DESCRIPTION
0:0	0-7	PRXD	R	**PARALLEL RECEIVER DATA:** In parallel mode, the received data is read from this register, when PDM bit (register 0F, Bit 7) is set.
0:1	0-7	PTXD	W	**PARALLEL TRANSMIT DATA:** Data to be transmitted, in parallel mode is written to this register, when PDM bit (register0 F, Bit 7) is set.
0:1	0	STXD	W	**SERIAL TRANSMIT DATA:** When the PDM bit is set and the SPDM bit is set, this bit can be used to send data in serial/parallel mode. This serial/parallel mode is data input into a parallel register, but bit by bit (one bit at a time).
0:2	0-7	FREQL	R/W	NOTE 1
0:3	0-7	FREQM	R/W	NOTE 1
0:4	0-7	MCFN	R/W	NOTE 1
0:5	0	REQ	R/W	**RESET EQUALIZER:** The setting of this bit sets the adaptive equalizer of the XR-2901.
	1	UNDEFINED		

REGISTER	BIT(S)	SYMBOL	R/W	DESCRIPTION
	2	SCR	R/W	**SCRAMBLER ENABLE:** When this bit is set, the scrambler for the transmitter and descrambler for the receiver are enabled.
	3	RXSP	R/W	**RECEIVER SPEED SELECT:** This bit, when set, selects 2400 BPS and when low, 1200 BPS modes of operation.
	4	TXSP	R/W	**TRANSMITTER SPEED SELECT:** This bit, when set selects 2400 BPS and when low, 1200 BPS modes of operation.
	5	UNDEFINED		
	6	UNDEFINED		
	7	RTS	R/W	**REQUEST TO SEND:** This bit controls the XR-2900 transmitter. When set, the transmitter is on. A low level stops the transmitter carrier.
0:6	0-7	UNDEFINED		
0:7	0	UNDEFINED		
	1	MOD	W	**MODE SELECT:** When set, answer mode and when reset, originate modes of operation are selected.
	2	GTE	R/W	**GUARD TONE ENABLE:** This bit, when set, enables either a 550 Hz or 1800 Hz tone to be transmitted.
	3	GTS	R/W	**GUARD TONE SELECT:** This bit, when set, selects an 1800 Hz tone, and when reset, a 550 Hz tone.
	4	RCVG	R/W	**RECEIVE FILTER GAIN CONTROL:** When set, 16dB of receive gain is selected. Resetting this bit lowers the gain to 6dB.
	5	PWRD	R/W	**POWER DOWN:** Setting this bit puts the XR-2902 into a low power mode. (See Electrical Characteristics for supply current values.)
	6	CPM	R/W	**CALL PROGRESS MONITORING:** When set, call progress mode of operation will be selected.
	7	ALB	R/W	**ANALOG LOOP BACK:** This bit, when set, enables the analog loop back mode of the XR-2900. The transmitted signal bypasses the receive filter and is applied to the demodulator input. Originate/Answer modes are selected by the Mode bit.
0:8	0	RXD	R	**RECEIVE DATA OUTPUT:** This bit represents the receive data in a serial format. The data at this point has not yet passed through the data buffer (sync-to-async converter.)
	1	URXD	R	**UNSCRAMBLED RECEIVE DATA OUTPUT:** The data available at this location is directly from the demodulator output, prior to the demodulator. This signal is used during handshaking and DLB initiation.
	2	CD	R	**CARRIER DETECT:** this bit is the output of the energy detect circuit, and is the logical inversion of FED.
	3	SGQ	R	**SIGNAL QUALITY:** When high, this bit indicates a degradation of signal quality and increased chance for errors. Less severe signal degradations will cause this output to 'chatter', and an averaging may be necessary.
	4	S1D	R	**S1 SIGNAL DETECT:** This bit, when high, indicates the detection of an S1 pattern.
	5	DOT	R	**DOTTING PATTERN DETECTORS:** A high at this bit indicates the reception of a dotting pattern, as used in a request for remote digital loopback.

REGISTER	BIT(S)	SYMBOL	R/W	DESCRIPTION
	6	UNDEFINED		
	7	UNDEFINED		
0:9	0	CRXD	R/W	**CLAMP RECEIVE DATA:** When set, the receive data output will be clamped to a high level.
	1	SPDM	R/W	**SERIAL DATA MODE SELECT:** When set, the serial/parallel data mode is selected. See STXD (Register 1, Bit 0) for mode description.
	2	SLAVE	R/W	**SLAVE MODE:** When this bit is set, the transmit clock is internally connected to the receive clock.
	3	ETE	R/W	**EXTERNAL TRANSMIT CLOCK ENABLE:** This bit, when set, allows an external transmit clock to be applied to pin 6 of the XR-2902.
	4	DLB	R/W	**DIGITAL LOOP BACK:** When enabled, set to a high, the transmit clock will track the receive clock, and transmit data will be tied to the receive data. This bit is used to enable remote digital loopback after a receive signal dotting pattern is detected.
	5	NTD	R/W	**NORMAL TRANSMIT DATA:** When this bit is set, the transmit path is from the STXD, transmit byte register, or TXD pin. When reset, the special transmit pattern bits control the data to be transmitted.
	6	STC1	R/W	**SPECIAL TRANSMIT PATTERN CONTROL 1:** See STC2
	7	STC2	R/W	**SPECIAL TRANSMIT PATTERN CONTROL 2:** STC1/STC2 control the generation of special transmit patterns, as described below:

STC2	STC1	PATTERN
0	0	Space
1	0	Mark
1	1	Dotting
1	0	300Hz for S1 Pattern

0:A	0	DBEN	R/W	**DATA BUFFER ENABLE:** This bit, when set, enables the async-to-sync and sync-to-async converters.
	1	DSPD	R/W	**DATA BUFFER OVERSPEED SELECT:** This bit, when set, extends the allowable asynchronous data rate from its normal +1% / -2.5% to +2.3% / -2.5%.
	2-3	BC1/BC2	R/W	**BIT PER CHARACTER SELECTION:** The asynchronous character lengths are controlled according to the following table:

BC2	BC1	Character Length (1 start+data+1 stop)
0	0	8 Bits
0	1	9 Bits
1	0	10 Bits
1	1	11 Bits

REGISTER	BIT(S)	SYMBOL	R/W	DESCRIPTION
	4	SPC	R/W	**SPEAKER CONTROL:** This bit, when set, enables the speaker output.
	5,6	VOL1, VOL2	R/W	**VOLUME CONTROL 1/2:** NOTE 1
	7	RESERVED	R/W	**SPECIAL EXAR TEST BIT.** This bit must be set to low for normal operation.
0:B	0-7	RESERVED		
0:C	0-7	RESERVED		
0:D	0-3	TXL1-4	R/W	**TRANSMIT LEVEL CONTROLS:** NOTE 1
	4-7	RESERVED		
0:E	0	MDA0	R	**MODEM DATA AVAILABLE:** NOTE 1
	1	MDAT	R	**TRANSMIT MODEM DATA AVAILABLE:** This bit, when set indicates transmit data can be applied to the transmit register.
	2	IEO	R/W	**RECEIVE INTERRUPT ENABLE:** This bit will go low when the receive data buffer is full.
	3	SETUP	R/W	**SETUP:** This bit must be set whenever a change is made to register 4. When the change is complete, the bit will be reset.
	4	IET	R/W	**INTERRUPT ENABLE:** This bit will be high when the transmit buffer is empty.
	5-6	RESERVED	R/W	
	7	IAO	R	**INTERRUPT ACTIVE:** This output indicates when the XR-2902 has requested an interrupt.
0:F	0-6	RMAA	R/W	**RAM ACCESS ADDRESS:** These bits select the RAM address for the XR-2901 for diagnostic purposes. Figure 10 contains the function information. The process of reading these locations is as follows: •Load desired RAM location into location 0F, Bits 0-6. •Read Register 0; this resets register 0E, Bit 0. •When Register 0E, Bit 0, returns to a Logic 1, data is present at Register 0:3 as described in Figure 10.
	7	PDM	R/W	**PARALLEL MODE:** This bit, when set, allows TXD/RXD to go through parallel bus.
1:0-1:4	0-7	RESERVED		
1:5	0-5	RESERVED		
	6	FED	R	**FAST ENERGY DETECT:** NOTE 1
	7	RESERVED		
1:6-1:A	0-7	RESERVED		
1:B	0-4	RESERVED		
	5, 6, 7	FR1, FR2, FR3	R	**FREQUENCY 1, 2, 3 DETECT:** NOTE 1
1:C	0-7	RESERVED		
1:D	0	RESERVED		
	1	FRT	R/W	**FREEZE EQUALIZER TAPS:** When set, the equalizer taps are fixed at their last value. This is used to compensate for a momentary loss of receive carrier.
	2-7	RESERVED		
1:E-1:F	0-7	RESERVED		

Location BIT	7	6	5	4	3	2	1	0
1F								
1E								
1D							$\overline{FRT}$	
1C								
1B	FR3	FR2	FR1					
1A								
19								
18								
17		$\overline{PNDET}$						$\overline{CDET}$
16								
15		$\overline{FED}$						
14						P2DET		
13								
12								
11								
10								
0F	PDM	RAM Access Address						
0E	IA0				SETUP	IE0		MDA0
0D		CAB2	CAB1	RDEQ	TXL4	TXL3	TXL2	TXL1
0C								
0B								
0A	TEST	VOL2	VOL1	SPC				
09								
08		$\overline{CTS}$						
07				RCVG				
06								
05	RTS	TDIS	RAMW		EPT	SQEXT		
04	Modem Configuration							
03	RAM Data XSM; FREQM							
02	RAM Data XSL; FREQL							
01								
00	Transceiver PTXRXD							

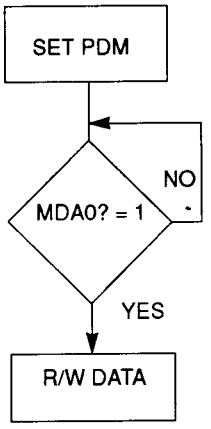
Figure 9. XR-2900 Control Register Plane for Fax Operation

Location	7	6	5	4	3	2	1	0
1 F								
1 E								
1 D							FRT	
1 C								
1 B	FR3	FR2	FR1					
1 A								
1 9								
1 8								
1 7								
1 6								
1 5		FED						
1 4								
1 3								
1 2								
1 1								
1 0								
0 F	PDM	RAM Access Address						
0 E	IA0			IET	SETUP	IE0	MDAT	MDA0
0 D	GTE				TXL4	TXL3	TXL2	TXL1
0 C								
0 B								
0 A	TEST	VOL2	VOL1	SPC	BC2	BC1	DSPD	DBEN
0 9	STC2	STC1	NTD	DLB	ETE	SLAVE	SPDM	CRXD
0 8			DOT	S1D	SGQ	CD	URXD	RXD
0 7	ALB	CPM	PWRD	RCVG	GTS	GTE	MOD	- -
0 6								
0 5	RTS			TXSP	RXSP	SCR		REQ
0 4	Modem Configuration							
0 3	RAM Data XSM; FREQM							
0 2	RAM Data XSL; FREQL							
0 1	Parallel Transmit Data PTXD							STXD
0 0	Parallel Receiving Data PRXD							

Figure 10. XR-2900 Control Register Plane for Data Mode

Read / Write Parallel Data Transfer to the XR-2900 -Transferring data to and from the XR-2900 is done differently, depending whether polling or interrupt driven.

POLLING



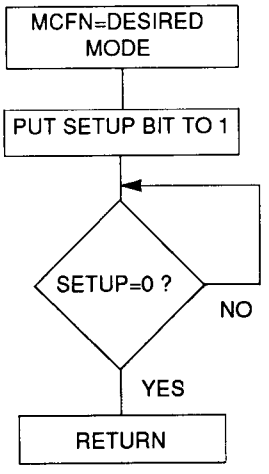
REG O: F (HEX15) BIT 7

INTERRUPT

FULL DUPLEX
1. Set PDM
2. Set IE0 IET to Enable Interrupt
3. Depending on Transmit or Receive Data
   MDA0 - For RXD
   MDAT - For TXD
   Reset INT to low
4. When Data is ready the interrupt will go low

HALF DUPLEX
1. Set PDM Mode
2. Set IEQ to Enable Interrupt
3. When Data is ready, the interrupt will go low

XR-2900 Mode Setting - The following flow diagram describes the XR-2900 mode setting procedure.



REG 0:E (HEX 14) BIT 3

POWER ON RESET

The XR-2900 contains an automatic internal hardware power-on reset/initialization routine. On power up the chip set is configured for V.29/9600 BPS fax operation. The following lists the functions within the fax mode set by the reset routine, with respective registers/values.

Mode/Function	(FAX Plane) Control Register	Register Value(HEX)
•V.29 / 9600 BPS	04	14
•Serial Data Transfer		
•Training Enabled		
•Echo Protector Tone Enabled	05	08
•No Extended Squelch		
•High Receive Gain Selected (16 dB)	07	00
•Unused Register	09	00
•Speaker Output is Disabled	0A	00
•Set Transmit Carrier Amplitude and Disable Receiver Cable Equalizer	0D	00

Call Progress Mode Operation

Call Progress Mode (CPM) is a mode of operation (during Data Mode) which allows the modem to detect various telephone signals. These signals are:

- Busy Tone
- Dial Tone
- Ring Back
- Answer Tone (Modem)

As the telephone signals fall in a different frequency band than the modem carriers, filtering requirements must change. To achieve this, the receive filter is changed for moniroting the various tones, as shown in table 1. In each case the carrier detect (CD) bit, bit2/Register 0:8 in data plane, is monitored. Sensing not only high or low, but also the duration and repetition rate of the CD active state is required.

CPM	MOD	CD
1	0	Receive High Band Monitor Answer Tone
1	1	Receive Low Band: Monitor Dial Tone, BusyTone and Ring Back Signal.
0	0	Normal High Band Energy Detect
0	1	Normal Low Band Energy Detect

CPM: REG 0:7, Bit 6
MOD: REG 0:7, Bit 1
CD: REG 0:8, Bit 2

Table 1. CD Frequency Band Assignments

APPLICATIONS INFORMATION

The XR-2900 Fax/Data chip set provides the complete data pump function for implementing a modem supporting 9600 BPS G3 facsimile operation, as well as full duplex data capability at 2400 BPS, 1200 BPS, and 300 BPS. The generalized system connection, figure 3, illustrates the remaining functions supporting the XR-2900 to complete the modem, also described here:

•Data Pump - XR-2900/XR-2901 chip set
- Modulation/demodulation for Fax/ Data Modes
- Signals for Handshaking/Establishing Connections/Telephone Signals (call progress, dialing)
- Test Modes
- Interface for Host Controller

•Telephone Line Interface (DAA)
- Line Interface Functions Required by FCC
- DC Isolation
- High Voltage Protectio
- Out of Band Frequency Suppression
- Hybrid Function for Separating Transmit and Receive Signals

•DTE (Data Terminal Equipment) Interface
- Serial (Stand-alone type modem)
- EIA Level Translation (RS-232C)
- Parallel (Internal Type Modem)

UART- (Serial to Parallel Conversion)

•Host Controller
- Timing/Control for Handshaking
- Command (Hayes®, MNP®, Fax Control) Interpretation
- ROM (EPROM) for Commands
- RAM (MNP, Data Mode)

EXAR's modem schematic illustrates a practical example of a stand-alone Fax/Data modem where a 8031 type microprocessor provides the system control for the XR-2901/XR-2902 chip set. An external EPROM contains the control commands, such as Hayes commands for data mode. EXAR will also offer a masked ROM controller, supporting MNP 5 V.42 and V.42bis operation during data mode (pin-to-pin replacement for generic 8031 controller).

LAYOUT CONSIDERATIONS

The XR-2900 provides the heart of the modem system, which processes signals from very low level analog to logic level digital. This mix of sensitive analog with noise causing digital signals calls for some special care in system layout.

Referring to figure 3, the generalized connection, the most critical signals path is that of the transmit (TXOUT) and receive (RCVIN) signals. They are passed from the telephone network through the line interface circuit (DAA) and on to the XR-2902 AFE. This path should be kept as short as possible and away from the digital circuitry, microcontroller and its memory components, and XR-2901 DSP. Figure 11 illustrates this concept.

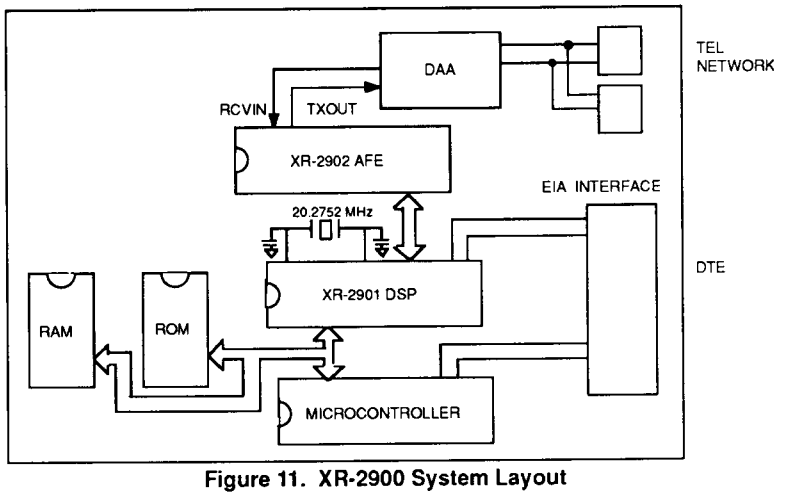


Figure 11. XR-2900 System Layout

CRYSTAL OSCILLATOR

The XR-2900 master clock, typically generated from a 20.2752 MHz crystal is another area requiring special attention. As with the analog and digital signal considerations, the crystal should be kept away from the TXC/RXC signal paths.

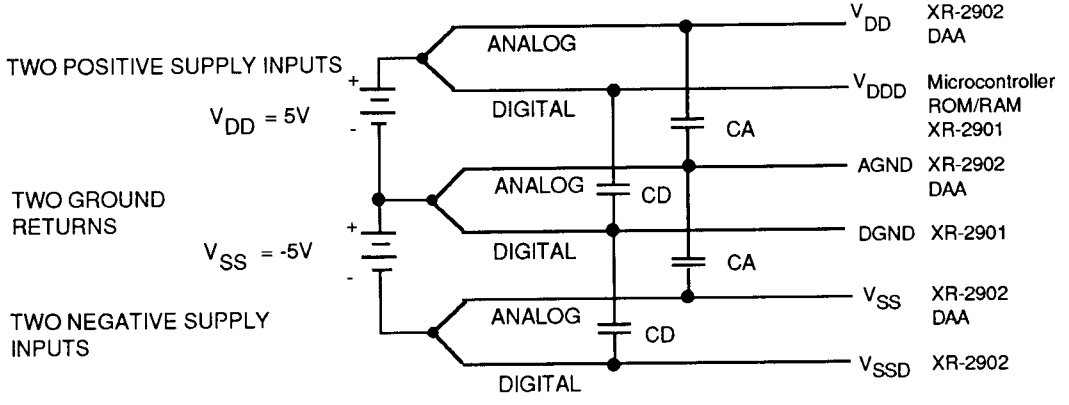
The accuracy and stability of the clock circuit are also extremely important. Per system specifications, it must have an accuracy of less than ±0.01 percent from nominal. The type of oscillator circuitry within the XR-2901 requires a parallel resonant type crystal. Typical external load capacitance (which can vary for different crystals) is 17pF. The capacitors should be returned to digital ground. The lines from the crystal to the XR-2901 should be kept short to minimize stray capacitance.

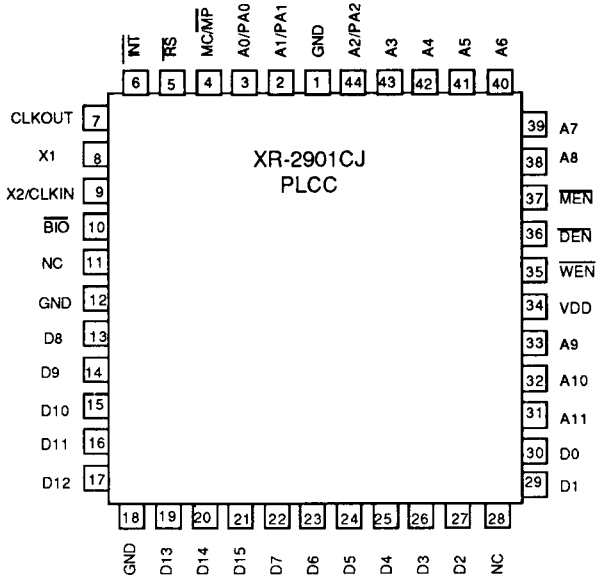
POWER / GROUND PRECAUTIONS

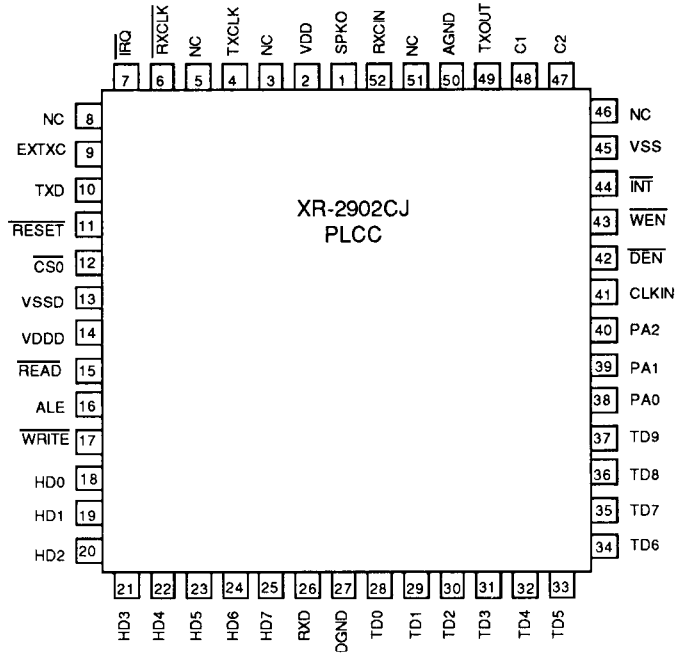
To help keep analog and digital circuitry separated, the system should incorporate independent paths for the power and signal supplies and gounds. As illustrated below, the digital and analog lines should be kept separated up to the power supply where they are single point connected.

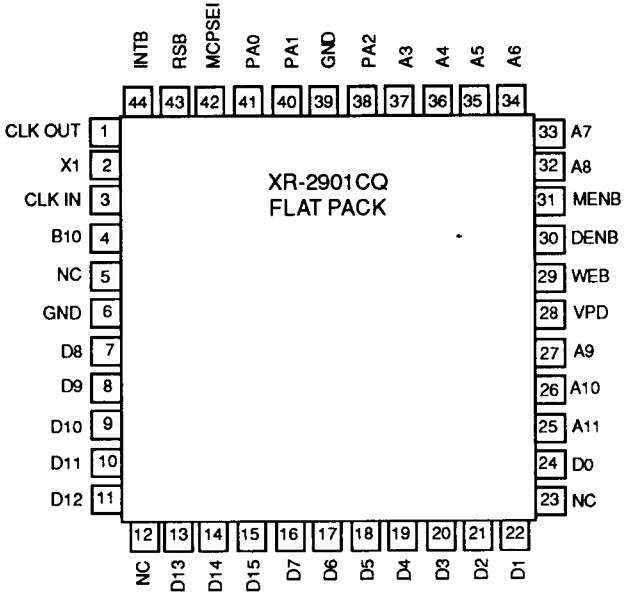
Supply bypassing is important with both VDD (VDDD) and VSS (VSSD), each having several bypassing capacitors distributed around the board. The VSS line near the XR-2902 is particularly critical and should have bypassing near it. Capacitors on analog supplies are returned to analog ground, and likewise digital to digital.

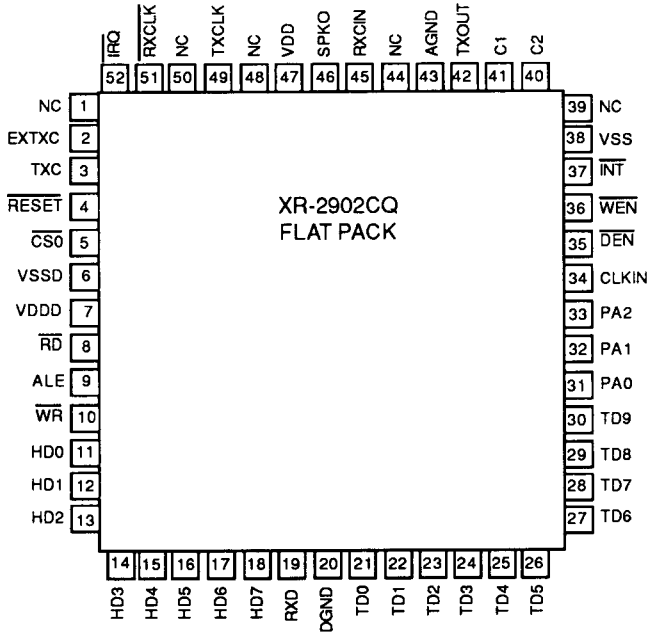
Capacitor valves around the board of 0.01μF are usually adequate, with a larger value, 4.7μF, at the power supply.




XR-2901CJ
PLCC
INT 6
TRS 5
MC/MP 4
A0/PA0 3
A1/PA1 2
GND 1
A2/PA2 44
A3 43
A4 42
A5 41
A6 40
CLKOUT 7
X1 8
X2/CLKIN 9
BIO 10
NC 11
GND 12
D8 13
D9 14
D10 15
D11 16
D12 17
39 A7
38 A8
37 MEN
36 DEN
35 WEN
34 VDD
33 A9
32 A10
31 A11
30 D0
29 D1
18 GND
19 D13
20 D14
21 D15
22 D7
23 D6
24 D5
25 D4
26 D3
27 D2
28 NC


XR-2902CJ
PLCC
IRQ 7
RXCLK 6
NC 5
TXCLK 4
NC 3
VDD 2
SPKO 1
RXCIN 52
NC 51
AGND 50
TXOUT 49
C1 48
C2 47
NC 8
EXTXC 9
TXD 10
RESET 11
CS0 12
VSSD 13
VDDD 14
READ 15
ALE 16
WRITE 17
HD0 18
HD1 19
HD2 20
46 NC
45 VSS
44 INT
43 WEN
42 DEN
41 CLKIN
40 PA2
39 PA1
38 PA0
37 TD9
36 TD8
35 TD7
34 TD6
21 HD3
22 HD4
23 HD5
24 HD6
25 HD7
26 RXD
27 DGND
28 TD0
29 TD1
30 TD2
31 TD3
32 TD4
33 TD5


XR-2901CQ
FLAT PACK
1 CLK OUT
2 X1
3 CLK IN
4 B10
5 NC
6 GND
7 D8
8 D9
9 D10
10 D11
11 D12
12 NC
13 D13
14 D14
15 D15
16 D7
17 D6
18 D5
19 D4
20 D3
21 D2
22 D1
23 NC
24 D0
25 A11
26 A10
27 A9
28 VPD
29 WEB
30 DENB
31 MENB
32 A8
33 A7
34 A6
35 A5
36 A4
37 A3
38 PA2
39 GND
40 PA1
41 PA0
42 MCPSEI
43 RSB
44 INTB


XR-2902CQ
FLAT PACK
1 NC
2 EXTXC
3 TXC
4 RESET
5 CS0
6 VSSD
7 VDDD
8 RD
9 ALE
10 WR
11 HD0
12 HD1
13 HD2
14 HD3
15 HD4
16 HD5
17 HD6
18 HD7
19 RXD
20 DGND
21 TD0
22 TD1
23 TD2
24 TD3
25 TD4
26 TD5
27 TD6
28 TD7
29 TD8
30 TD9
31 PA0
32 PA1
33 PA2
34 CLKIN
35 DEN
36 WEN
37 INT
38 VSS
39 NC
40 C2
41 C1
42 TXOUT
43 AGND
44 NC
45 RXCIN
46 SPKO
47 VDD
48 NC
49 TXCLK
50 NC
51 RXCLK
52 IRQ