CH7021/CH7022 SDTV/EDTV/HDTV Encoder

Features

- SDVO[1] to SDTV/EDTV/HDTV conversion supporting up to 160 MHz pixel clock
- SDVO to VGA conversion supporting up to 1600x1200 resolution[2]
- EDTV/HDTV support for 480p, 576p, 720p, 1080i and 1080p
- Support for NTSC, PAL, SECAM color modulation.
- Macrovision™ 7.1.L1 copy protection support for SDTV (CH7021 only)
- Macrovision™ copy protection support for progressive scan EDTV (480p, 576p) (CH7021 only)
- CGMS-A support for SDTV, EDTV and HDTV
- High-speed SDVO (1G~2Gbps) AC-coupled serial differential RGB inputs
- Flexible true scale rendering engine supports overscan compensation in all SDTV/EDTV and HDTV output resolutions[3]
- Text enhancement filter in scan conversion
- Adaptive de-flicker filter with up to 7 lines of filtering in scan conversion
- Contrast/Brightness/Sharpness control for TV output.
- Hue/Saturation Control for TV output.
- Support for SCART connector
- Support for EDTV / HDTV D-Connector
- Outputs CVBS, S-Video, VGA and YPbPr
- Support for VGA bypass
- TV / Monitor connection detect
- Programmable power management
- Four 10-bit video DAC outputs
- Three sets of DAC outputs supporting SDTV / EDTV / HDTV / VGA connectors
- Fully programmable through serial port
- Configuration through Intel® SDVO OpCode[1]
- Complete Windows driver support
- Offered in 64-pin LQFP and 64-pin QFN package

[1] Intel Proprietary.
[2] For the modes higher than 160 MHz pixel rate, please contact Chrontel Application Department for detail.
[3] Patent pending

General Description

The CH7021/CH7022 is a Display Controller device which accepts a digital graphics high speed AC coupled serial differential RGB input signal, and encodes and transmits data through analog SDTV ports (analog composite, s-video, VGA or YPrPb) or an analog EDTV/HDTV port (YPrPb). The device is able to encode the video signals and generate synchronization signals for NTSC, PAL and SECAM SDTV standards, as well as analog EDTV and HDTV interface standards and graphics standards up to UXGA. The device accepts one channel of RGB data over three pairs of serial data ports.

The TV-Out processor will perform scaling to convert VGA frames to all the supported TV output standards. Adaptive de-flicker filter provides superior text display. Large numbers of input graphics resolutions are supported up to 160 MHz pixel rate with full vertical and horizontal overscan compensation in all output standards. A high accuracy low jitter phase locked loop is integrated to create outstanding video quality.

In addition to scaling modes, bypass modes are included which perform color space conversion to all the TV standards and generate and insert all the TV sync signals, or output VGA style analog RGB.

Different analog video connectors are supported including composite, s-video, YPrPb, SCART, D-connector and VGA connector.

CGMS-A is also provided up to 1080i resolution. Content protection support is provided for Macrovision™ in SDTV and EDTV modes for CH7021 only.

The CH7021 is capable of adding Macrovision™ encoding to the output signal. CH7022 is the same chip without Macrovision™ encoding.

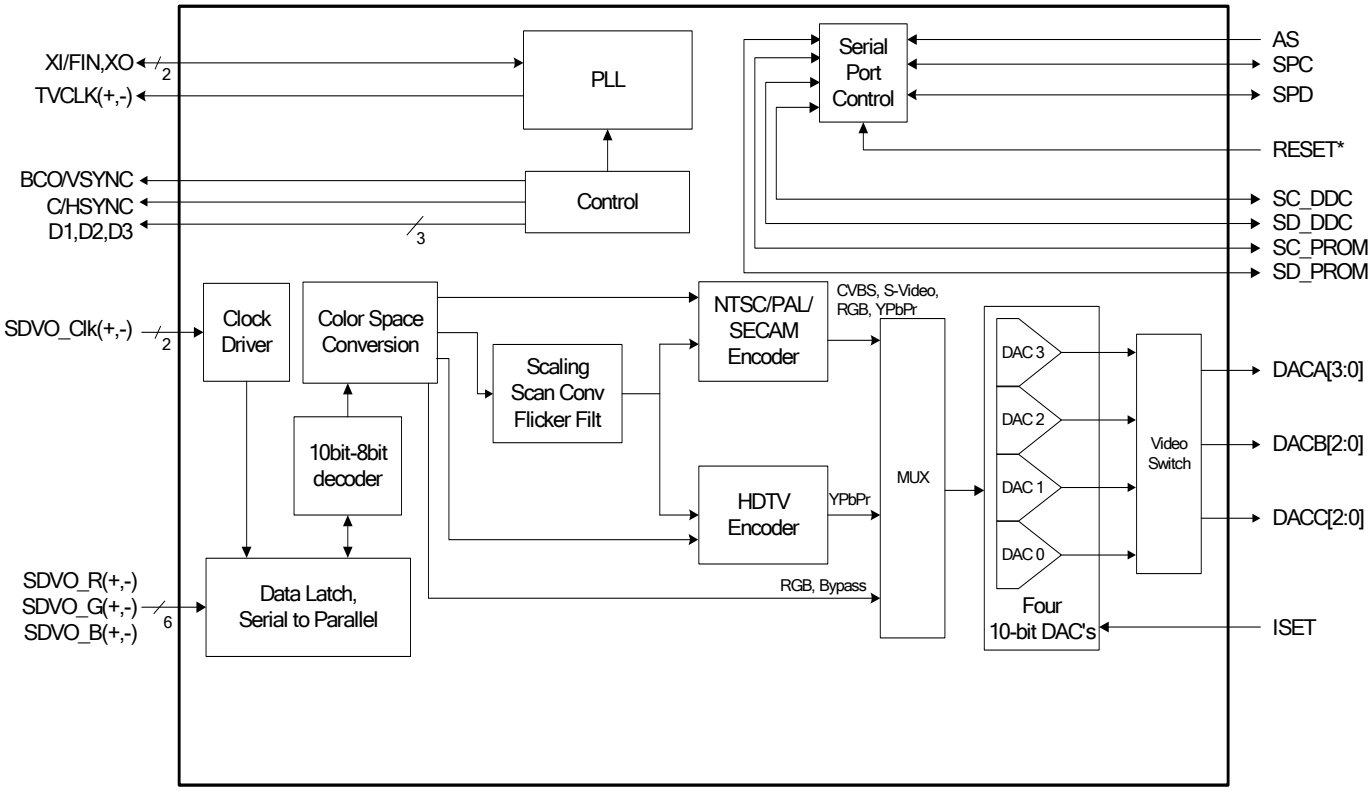

Figure 1: Functional Block Diagram

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1.0 Pin-Out

1.1 Package Diagram

1.1.1 The 64-Pin LQFP Package Diagram

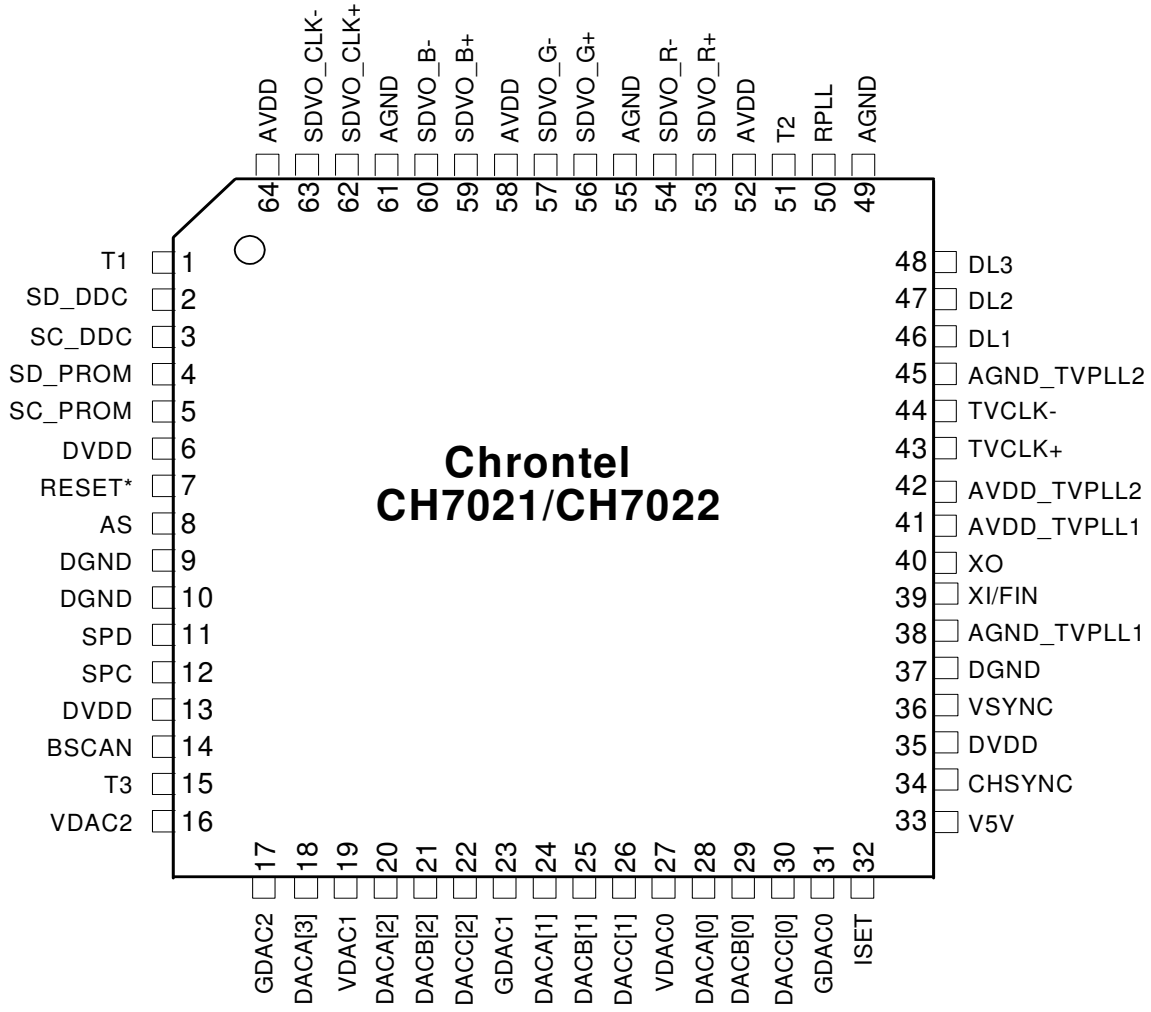


Figure 2: 64-Pin LQFP Package

1.1.2 The 64-Pin QFN Package Diagram

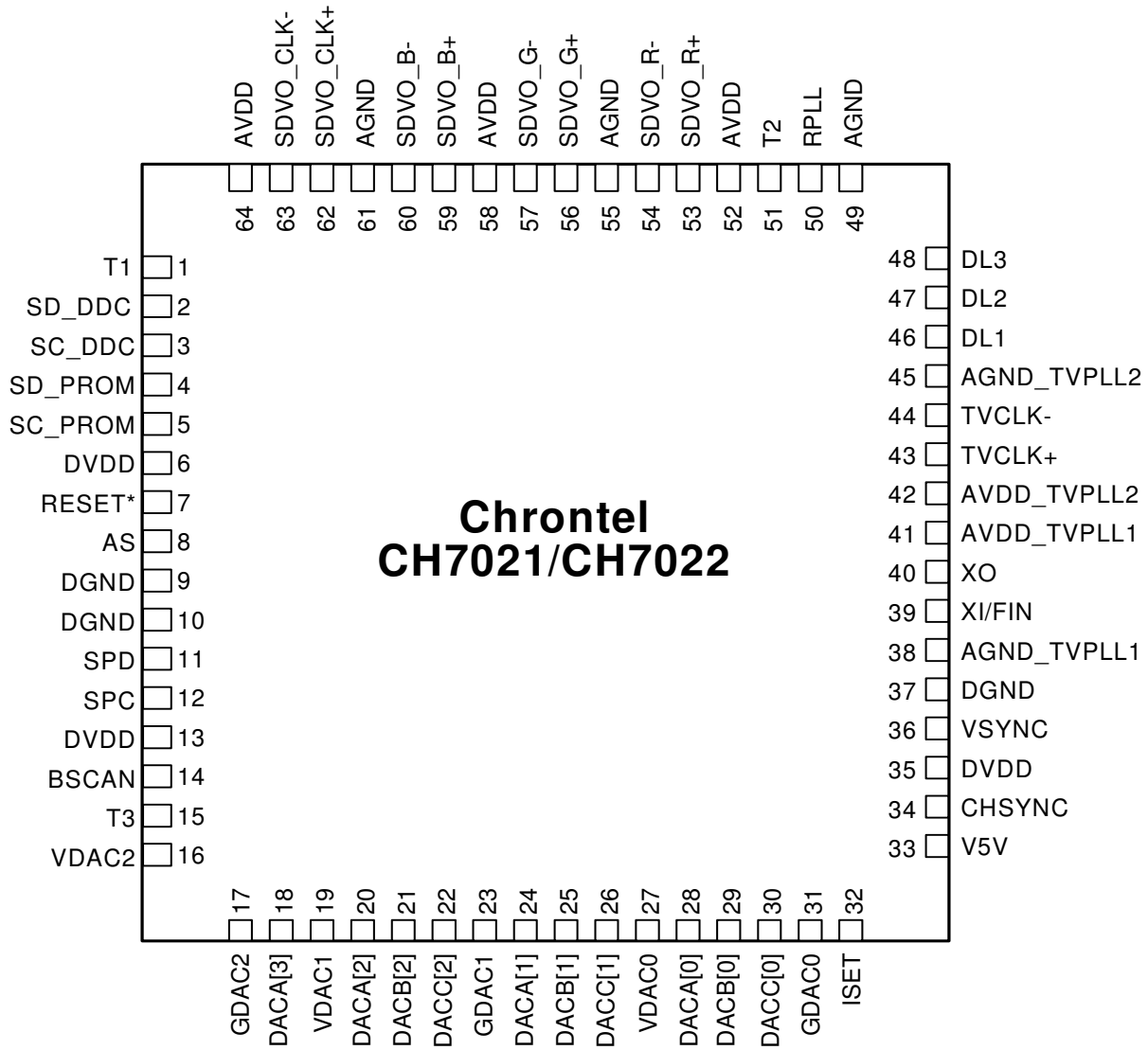


Figure 3: 64-Pin QFN Package

1.2 Pin Description

Table 1: Pin Description

Pin #	Type	Symbol	Description
1,51	Out	T1,T2	**Test** These pins are reserved for factory test and default to high impedance. These pins should be left open in normal operations.
2	In/Out	SD_DDC	**Routed Serial Port Data Output to DDC** This pin functions as the bi-directional data pin of the serial port to DDC receiver. This pin will require a 10k pull-up resistor to the desired high state voltage. Leave open if unused.
3	In/Out	SC_DDC	**Routed Serial Port Clock Output to DDC** This pin functions as the clock bus of the serial port to DDC receiver. This pin will require a 10k pull-up resistor to the desired high state voltage. Leave open if unused.
4	In/Out	SD_PROM	**Routed Data Output to PROM** This pin functions as the bi-directional data pin of the serial port for PROM on ADD2◊ card. This pin will require a 10k pull-up resistor to the desired high state voltage. Leave open if unused.
5	In/Out	SC_PROM	**Routed Clock Output to PROM** This pin functions as the clock bus of the serial port to PROM on ADD2 card. This pin will require a 10k pull-up resistor to the desired high state voltage. Leave open if unused.
7	In	RESET*	**Reset* Input (Internal pull-up)** When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port register. This pin is 3.3V compliant.
8	In	AS	**Address Select (Internal pull-up)** This pin determines the serial port address of the device (0,1,1,1,0,0,AS*,0). When AS is low the address is 72h, when high the address is 70h.
11	In/Out	SPD	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port and operates with inputs from 0 to 2.5V. Outputs are driven from 0 to 2.5V. This pin requires an external 4kΩ - 9 kΩ pull up resistor to 2.5V.
12	In/Out	SPC	**Serial Port Clock Input** This pin functions as the clock input of the serial port and operates with inputs from 0 to 2.5V. This pin requires an external 4kΩ - 9kΩ pull up resistor to 2.5V.
14	In	BSCAN	**BSCAN** (internal pull low) This pin should be left open or pulled low with a 10k resistor in the application. This pin enables the boundary scan for in-circuit testing. Voltage level is 0 to DVDD. This pin should be pulled low during normal operation.
15	In	T3	**Test** (internal pull-down) This pin should be left open or pulled low with a 10k resistor in the application.
18,20,24,28	Out	DACA[3:0]	**DAC Output A** Video Digital-to-Analog outputs. Refer to section 2.2.2 for information regarding support for Composite Video, S-Video, SCART, YPrPb and VGA Bypass outputs. Each output is capable of driving a 75-ohm doubly terminated load.
21,25,29	Out	DACB[2:0]	**DAC Output B** Video Digital-to-Analog outputs. Refer to section 2.2.2 for information regarding supports for Composite Video, S-Video, SCART, YPrPb and VGA Bypass outputs. Each output is capable of driving a 75-ohm doubly terminated load.

◊ Intel Proprietary.

Table 1: Pin Description (contd.)

Pin #	Type	Symbol	Description
22,26,30	Out	DACC[2:0]	**DAC Output C** Video Digital-to-Analog outputs. Refer to section 2.2.2 for information regarding supports for Composite Video, S-Video, SCART, YPrPb and VGA Bypass outputs. Each output is capable of driving a 75-ohm doubly terminated load.
32	In	ISET	**Current Set Resistor Input** This pin sets the DAC current. A 1.2Kohm (+/- 1%) resistor should be connected between this pin and DAC ground (pin 31) using short and wide traces.
34	Out	CHSYNC	**Composite / Horizontal Sync Output** A buffered version of VGA composite sync as well as horizontal sync can be acquired from this pin.
36	Out	VSYNC	**VSYNC** A buffered version of VGA vertical sync can be acquired from this pin.
39	In	XI/FIN	**Crystal Input / External Reference Input** A parallel resonant 27MHz crystal (±20 ppm) should be attached between this pin and XO. However, an external CMOS clock can drive the XI/FIN input.
40	Out	XO	**Crystal Output** A parallel resonance 27MHz crystal (±20 ppm) should be attached between this pin and XI/FIN. However, if an external CMOS clock is attached to the XI/FIN input, XO should be left open.
43,44	Out	TVCLK+/-	**Pixel Clock Output** When the chip is operating as a TV encoder in master clock mode, this pair outputs a differential clock to the VGA controller. The VGA controller uses this as a reference frequency to generate SDVO_CLK+/- to the chip. The clock frequency is between 100MHz ~ 200MHz. This clock pair will run at an integer multiple of the desired input pixel rate. Refer to section 2.1.3 for details.
46	Out	DL1	**D-Connector Line 1** Video format identification line for EDTV / HDTV D-Connector. See section 2.5.
47	Out	DL2	**D-Connector Line 2** Video format identification line for EDTV / HDTV D-Connector. See section 2.5.
48	Out	DL3	**D-Connector Line 3** Video format identification line for EDTV / HDTV D-Connector. See section 2.5.
50	In	RPLL	**PLL Resistor Input** External resistor 10Kohm should be connected between this pin and pin 49.
53,54,56,57 59,60	In	SDVO_R+/-, SDVO_G+/-, SDVO_B+/-	**SDVO Data Channel Inputs** These pins accept 3 AC-coupled differential pair of RGB inputs from a digital video port of a graphics controller.
62,63	In	SDVO_CLK+/-	**Differential Clock Input associated with SDVO Data channel (SDVO_R+/-, SDVO_G+/-, SDVO_B+/-)** The range of this clock pair is 100~200MHz. For specified pixel rates in specified modes this clock pair will run at an integer multiple of the pixel rate. Refer to section 2.1.3 for details.

Table 1: Pin Description (contd.)

Pin #	Type	Symbol	Description
6,13,35	Power	DVDD	**Digital Supply Voltage** (2.5V)
9,10,37	Power	DGND	**Digital Ground**
16	Power	VDAC2	**DAC Supply Voltage** (3.3V)
17	Power	GDAC2	**DAC Ground**
19	Power	VDAC1	**DAC Supply Voltage** (3.3V)
23	Power	GDAC1	**DAC Ground**
27	Power	VDAC0	**DAC Supply Voltage** (3.3V)
31	Power	GDAC0	**DAC Ground**
41	Power	AVDD_TVPLL1	**TV PLL1 Supply Voltage** (2.5V)
38	Power	AGND_TVPLL1	**TV PLL1 Ground**
42	Power	AVDD_TVPLL2	**TV PLL2 Supply Voltage** (2.5V)
45	Power	AGND_TVPLL2	**TV PLL2 Ground**
52,58,64	Power	AVDD	**Analog Supply Voltage** (2.5V)
49,55,61	Power	AGND	**Analog Ground**
33	Power	V5V	**D-Connector Supply Voltage** (5V)

2.0 Functional Description

2.1 Input Interface

2.1.1 Overview

One pair of differential clock signal and three differential pairs of data signals (R/G/B) form one channel data. The input data are 10-bit serialized data. Input data run at 1Gbits/s~2Gbits/s, being a 10x multiple of the clock rate (SDVO_CLK+/-). The CH7021/CH7022 de-serializes the input into 10-bit parallel data with synchronization and alignment. Then the 10-bit characters are mapped into 8-bit color data or control data (Hsync, Vsync, DE).

2.1.2 Interface Voltage Levels

All differential SDVO pairs are AC coupled differential signals. Therefore, there is not a specified DC signal level for the signals to operate at. The differential p-p input voltage has a min of 175mV, and a max of 1.2V. The differential p-p output voltage has a min of 0.8V, with a max of 1.2V.

2.1.3 Input Clock and Data Timing

A data character is transmitted least significant bit first. The beginning of a character is noted by the falling edge of the SDVO_CLK+ edge. The skew among input lanes is required to be no larger than 2ns.

The clock rate runs at 100MHz~200MHz. The pixel rate can be 25MP/s~165MP/s. The pixel rate and the clock rate do not always equal. The clock rate can be a multiple of the pixel rate (1x, 2x or 4x depending on the pixel rate) so that the clock rate will be stay in the 100MHz~200MHz range. In the condition that the clock rate is running at a multiple of the pixel rate, there isn't enough pixel data to fill the data channels. Dummy fill characters ('0001111010') are used to stuff the data stream. The CH7021/CH7022 supports the following clock rate multipliers and fill patterns shown in Table 2.

Table 2: CH7021/CH7022 supported Pixel Rates, Clock Rates, Data Transfer Rates and Fill Patterns

Pixel Rate	Clock Rate – Multiplier	Stuffing Format	Data Transfer Rate - Multiplier
25~50 MP/s	100~200 MHz – 4xPixel Rate	Data, Fill, Fill, Fill	1.00~2.00 Gbits/s – 10xClock Rate
50~100 MP/s	100~200 MHz – 2xPixel Rate	Data, Fill	1.00~2.00 Gbits/s – 10xClock Rate
100~200 MP/s	100~200 MHz – 1xPixel Rate	Data	1.00~2.00 Gbits/s – 10xClock Rate

2.1.4 Synchronization

Synchronization and channel-to-channel deskewing is facilitated by the transmission of special characters during the blank period. The CH7021/CH7022 synchronizes during the initialization period and subsequently uses the blank periods to re-synch to the data stream.

2.2 TV Output Operation

2.2.1 Overview

The CH7021/CH7022 is capable of being operated as a RGB to SDTV/EDTV/HDTV scaler/encoder, or as an SDTV/EDTV/HDTV bypass encoder. The output can be CVBS, S-video, SCART or YPrPb. In scaler/encoder mode, the input can be any resolution of RGB input. The CH7021/CH7022 will scale and format the data and sync signals to the proper output TV format. Table 3 lists some of the VGA resolutions. Table 4 lists the supported SDTV standards (refer to SMPTE170, ITU-R BT470). Table 5 lists the supported EDTV/HDTV standards. In TV bypass mode, input graphics frame size and timing is the same as the required output TV format. The CH7021/CH7022 will format the data and insert proper sync signals according to the output TV standard.

Table 3: Various VGA resolutions.

Name	Resolution
	320x200
QVGA	320x240
	400x300
	640x350, 640x400
VGA	640x480
	512x384
	704x480, 704x576
	720x350, 720x400, 720x480, 720x540, 720x576
	768x480, 768x576
SVGA/WSVGA	800x600
	832x624
	848x480
	920x766
	960x600
	1024x600
XGA/WXGA	1024x768
	1124x768
	1152x720
	1280x768, 1280x720, 1280x800, 1280x960
SXGA/WSXGA	1280x1024
	1360x768, 1366x768, 1466X768, 1360x1024
SXGA+/WSXGA+	1400x1050
	1400x1200
	1536x960
	1680x1050
UXGA/WUXGA	1600x1200
	1704x960
	1920x1080
	1900x1200[4]

[4] With reduced blanking.

Table 4: Supported SDTV standards

Standards	Field Rate (Hz)	Total	Scan Type
NTSC-M	60/1.001	858x525	Interlaced
NTSC-J	60/1.001	858x525	Interlaced
NTSC-443	60/1.001	858x525	Interlaced
PAL-60	60/1.001	858x525	Interlaced
PAL-M	60/1.001	858x525	Interlaced
SECAM-60	60/1.001	858x525	Interlaced
PAL-B/D/G/H/I	50	864x625	Interlaced
PAL-N	50	864x625	Interlaced
PAL-Nc	50	864x625	Interlaced
SECAM-B/D/G/K/K1/L	50	864x625	Interlaced

Table 5: Supported EDTV/HDTV standards

Standards		Field/Frame Rate(Hz)	Total	Active	Clock(MHz)	Scan Type
480/60p	SMPTE293M EIA770.2A	60/1.001	858x525	720x480	27	Progressive
576/50p	ITU-R BT1358	50	864x625	720x576	27	Progressive
720/60p	SMPTE296M	60 or 60/1.001	1650x750	1280x720	74.25	Progressive
720/50p	SMPTE296M	50	1980x750	1280x720	74.25	Progressive
1080/60i	SMPTE274M	60 or 60/1.001	2200x1125	1920x1080	74.25	Interlaced
1080/50i	SMPTE274M	50	2640x1125	1920x1080	74.25	Interlaced
1080/50i	SMPTE295M	50	2376x1250	1920x1080	74.25	Interlaced
1080/30p	SMPTE274M	30 or 30/1.001	2200x1125	1920x1080	74.25	Progressive
1080/25p	SMPTE274M	25	2640x1125	1920x1080	74.25	Progressive
1080/24p	SMPTE274M	24 or 24/1.001	2750x1125	1920x1080	74.25	Progressive
1080/60p	SMPTE274M	60 or 60/1.001	2200x1125	1920x1080	148.5	Progressive
1080/50p	SMPTE274M	50	2640x1125	1920x1080	148.5	Progressive
1080/50p	SMPTE295M	50	2376x1250	1920x1080	148.5	Progressive
1035/60i	SMPTE240M	60 or 60/1.001	2200x1125	1920x1035	74.25	Interlaced

2.2.2 Video DAC Outputs

Table 6 below lists the DAC output configurations of the CH7021/CH7022.

Table 6: Video DAC Configurations for CH7021/CH7022

Output Type	DACA[0]	DACA[1]	DACA[2]	DACA[3]
SCART	B	G	R	CVBS
VGA	B	G	R	
	DACB[0]	**DACB[1]**	**DACB[2]**	
CVBS	CVBS			
S-Video		Y	C	
	DACC[0]	**DACC[1]**	**DACC[2]**	
YPrPb	Pb	Y	Pr	

2.2.3 Adaptive Flicker Filter

The CH7021/CH7022 integrates an advanced up to 7-line (depending on input/output ratio) vertical deflickering filter circuit to help eliminate the flicker associated with interlaced displays. This flicker circuit provides an adaptive filter algorithm for implementing flicker reduction with selections of high, medium or low flicker content for both luma and chroma channels. In addition, a special text enhancement circuit incorporates additional filtering for enhancing the readability of text. The circuit can automatically calculate the possible flicker settings and it is also programmable through user input.

2.2.4 Overscan Compensation

The CH7021/CH7022 has the capability of compensating overscan of regular TV displays. Horizontal overscan adjustment is continuous and has a maximum of –50% compensation depending on input resolution and output standard. Vertical overscan adjustment requires the input timing to be changed and has a maximum of –50% compensation. In vertical scaling and overscan compensation mode the input vertical total is required to be a multiple of 10 lines when the output is interlaced scan type, or a multiple of 20 lines when the output is progressive scan type.

2.2.5 SDTV color sub-carrier generation

The CH7021/CH7022 allows the sub-carrier (NTSC, PAL, SECAM) frequency to be accurately generated from a 27 MHz crystal oscillator, leaving the subcarrier frequency independent of the graphics pixel clock frequency. This feature is important since even a ±0.01% subcarrier frequency variation is enough to cause some televisions to lose color lock.

2.2.6 TV picture adjustment

The CH7021/CH7022 has the capability of vertical and horizontal output picture position adjustment. The CH7021/CH7022 will automatically put the picture in the display center, and the position is also programmable through user input. The CH7021/CH7022 also provides brightness/sharpness/contrast adjustment. Hue and saturation adjustment are also available for NTSC/PAL output formats.

2.2.7 TV reference clock output

The CH7021/CH7022 will operate in Clock Master Mode. The CH7021/CH7022 integrates the low jitter PLL to generate a reference clock for the graphics controller. The reference clock will be at the input pixel rate and within 100-200MHz. If in some modes the clock rate is below 100MHz, it will be multiplied by 2 or 4 to fall within the required range.

2.2.8 TV Bypass mode

The CH7021/CH7022 can operate in TV Bypass mode. Input frame size and sync signal are the same as the selected TV output format. The data and sync signals are extracted and then formatted to the selected TV output standard.

2.3 VGA Bypass Operation

The CH7021/CH7022 can operate in VGA Bypass mode. In VGA Bypass mode, data from the graphics device, after proper decoding, are bypassed directly to the video DACs to implement a second RGB DAC function. Sync signals, after proper decoding, are buffered internally, and can be output to drive the RGB. The CH7021/CH7022 can support a pixel rate of 200MHz. This operating mode uses 8-bits of the DAC's 10-bit range, and provides a nominal signal swing of 0.661V (or 0.7V depending on DAC Gain setting in control registers) when driving a 75Ω doubly terminated load. No scaling, scan conversion or flicker filtering is applied in VGA Bypass modes.

2.4 Command Interface

Communication is through two-wire path, control clock (SPC) and data (SPD). The CH7021/CH7022 accepts incoming control clock and data from graphics controller, and is capable of redirecting that stream to an ADD2 card PROM, DDC, or CH7021/CH7022 internal registers. The control bus is able to run up to 1MHz when communicating with internal registers, up to 400kHz for the PROM and up to 100kHz for the DDC.

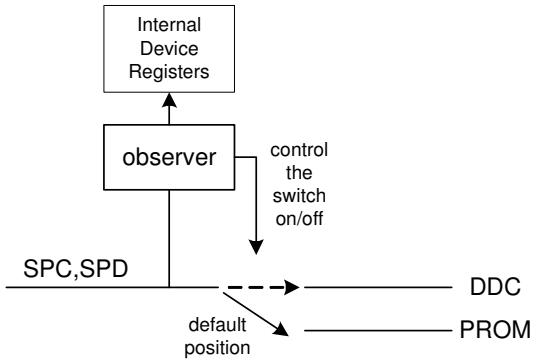


Figure 4: Control Bus Switch

Upon reset, the default state of the directional switch is to redirect the control bus to the ADD2 PROM. At this stage, the CH7021/CH7022 observes the control bus traffic. If the observing logic sees a control bus transaction destined for the internal registers (device address 70h or 72h), it disables the PROM output pairs, and switches to internal registers. In the condition that traffic is to the internal registers, an opcode command is used to set the redirection circuitry to the appropriate destination (ADD2 PROM or DDC). Redirecting the traffic to internal registers while at the stage of traffic to DDC occurs on observing a STOP after a START on the control bus.

2.5 D-Connector

The CH7021/CH7022 provides 3 pins (**DL[3:1]**) to identify the video scanning format and aspect ratio of the output signal from the encoder for digital broadcasting. An identification signal is discriminated using the voltage level of the 3 lines. The format of the signals follows EIAJ CP-4120 *Interface Between Digital Tuner and Television Receiver using D-Connector*. Table 7 below provides the specification of **DL1**, **DL2** and **DL3** for video format identification. Each line has 3 states depending on its DC voltage.

Table 7: Video Format Identification Using DL1, DL2 and DL3

Typical Voltage [V]	DL1 Total Scanning Lines (Effective Scanning Lines)	DL2 i or p (Note 1)	DL3 Aspect Ratio
5	1125 (1080)	59.94p, 60p	16:9
2.2	750 (720)	-	4:3 (Letter Box)
0	525 (480)	59.94i, 60i	4:3

Note 1: "i" = interlaced scanning, "p" = progressive scanning.

2.6 Boundary scan Test

CH7021/CH7022 provides so called "NAND TREE Testing" to verify IO cell function at the PC board level. This test will check the interconnection between chip I/O and the printed circuit board for faults (soldering, bend leads, open printed circuit board traces, etc.). NAND tree test is a simple serial logic which turns all IO cell signals to input mode, connects all inputs with NAND gates as shown in the figure below and switches each signal to high or low according to the sequence in Table 8. The test results then pass out at pin 51 (**T2**).

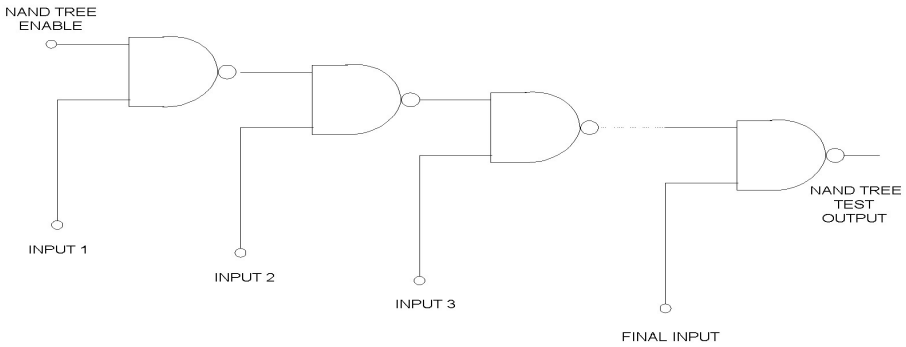


Figure 5: NAND Tree Connection

Testing Sequence

Set BSCAN =1; (internal weak pull low)

Set all signals listed in Table 8 to 1.

Set all signals listed in Table 8 to 0, toggle one by one with certain time period, suggested 100ns. Pin 51 (**T2**) will change its value each time an input value changed.

Table 8: Signal Order in the NAND Tree Testing

Order	Pin Name	LQFP Pin
1	SD_DDC	2
2	SC_DDC	3
3	SD_PROM	4
4	SC_ PROM	5
5	RESETB	7
6	AS	8
7	SPD	11
8	SPC	12
9	DACA[3]	18
10	DACA[2]	20
11	DACB[2]	21
12	DACC[2]	22
13	DACA[1]	24
14	DACB[1]	25
15	DACC[1]	26
16	DACA[0]	28
17	DACB[0]	29
18	DACC[0]	30
19	ISET	32
20	CHSYNC	34
21	VSYNC	36
22	XI/FIN	39
23	XO	40
24	TVCLK+	41
25	TVCLK-	42
26	DL1	46
27	DL2	47
28	DL3	48
29	T2	51

Table 9: Signals not Tested in NAND Test besides power pins

Pin Name	LQFP Pin
SDVO_R+	53
SDVO_R-	54
SDVO_G+	56
SDVO_G-	57
SDVO_B+	59
SDVO_B-	60
SDVO_CLK+	62
SDVO_CLK-	63
RESET*	7
BSCAN	14
T3	15
T1	1

3.0 Register Control

The CH7021/CH7022 is controlled via a serial control port. The serial bus uses only the SC clock to latch data into registers, and does not use any internally generated clocks so that the device can be written to in all power down modes. The device will retain all register values during power down modes.

Registers 00h to 11h are reserved for opcode use. All registers except bytes 00h to 11h are reserved for internal factory use. For details regarding Intel® SDVO opcodes, please contact Intel®.

4.0 Electrical Specifications

4.1 Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
	All 2.5V power supplies relative to GND All 3.3V power supplies relative to GND	-0.5 -0.5		3.0 5.0	V
T_{SC}	Analog output short circuit duration		Indefinite		Sec
T_{AMB}	Ambient operating temperature	-40		85	°C
T_{STOR}	Storage temperature	-65		150	°C
T_J	Junction temperature			150	°C
T_{VPS}	Vapor phase soldering (5 second) Vapor phase soldering (11 second) Vapor phase soldering (1 minute)			260 245 225	°C

Note:

1) Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating condition of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The temperature requirements of vapor phase soldering apply to all standard and lead free parts.

2) The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltages by more than ± 0.5V can induce destructive latchup.

4.2 Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
AVDD	Analog Power Supply Voltage	2.375	2.5	2.625	V
DVDD	Digital Power Supply Voltage	2.375	2.5	2.625	V
VDAC	DAC Power Supply	3.100	3.3	3.500	V
AVDD_TVPLL	Analog PLL Power Supply Voltage	2.375	2.5	2.625	V
VDD33	Generic for all 3.3V supplies	3.100	3.3	3.500	V
VDD25	Generic for all 2.5V supplies	2.375	2.5	2.625	V
V5V	D-Connector Power Supply	4.75	5.0	5.25	V
Rset	Resistor on Iset pin (32)	1188	1200	1212	Ω
	Ambient operating temperature	-40		85	°C

4.3 Electrical Characteristics

(Operating Conditions: T_A = –40°C to 85°C, VDD25 =2.5V ± 5%, VDD33 = 3. 3V ± 5%,)

Symbol	Description	Min	Typ	Max	Units
	Video D/A Resolution	10	10	10	bits
	Full scale output current		35.3		mA
	Video level error			10	%
$I_{VDD25,CVBS}$	Total VDD25 supply current (2.5V supplies) with CVBS output and 1024x768 input		250	280	mA
$I_{VDD25,S\text{-}Video}$	Total VDD25 supply current (2.5V supplies) with S-Video output and 1024x768 input		250	280	mA
$I_{VDD25,720p}$	Total VDD25 supply current (2.5V supplies) with YPrPb 720p output and 1024x768 input		300	350	mA
$I_{VDD25,1080i}$	Total VDD25 supply current (2.5V supplies) with YPrPb 1080i output and 1704x960 input		310	330	mA
$I_{VDD25,1080p}$	Total VDD25 supply current (2.5V supplies) with YPrPb 1080p output and 1704x960 input		330	350	mA
$I_{VDD33,CVBS}$	Total VDD33 supply current (3.3V supply) with CVBS output and 1024x768 input		50	60	mA
$I_{VDD33,S\text{-}Video}$	Total VDD25 supply current (2.5V supplies) with S-Video output and 1024x768 input		90	100	mA
$I_{VDD33,720p}$	Total VDD33 supply current (3.3V supply) with YPrPb 720p output and 1024x768 input		160	180	mA
$I_{VDD25,1080i}$	Total VDD33 supply current (3.3V supplies) with YPrPb 1080i output and 1704x960 input		140	160	mA
$I_{VDD25,1080p}$	Total VDD33 supply current (3.3V supplies) with YPrPb 1080p output and 1704x960 input		160	180	mA
I_{VDDV}	Total V5V current (5.0V supply)		100	300	µA
I_{PD}	Total Power Down Current		0.1		mA

4.4 DC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
$V_{RX-DIFFp-p}$	SDVO Receiver Differential Input Peak to Peak Voltage	$V_{RX-DIFFp-p} = 2 * \lvert V_{RX-D+} - V_{RX-D-} \rvert$	0.175		1.200	V
$Z_{RX-DIFF-DC}$	SDVO Receiver DC Differential Input Impedance		80	100	120	Ω
$Z_{RX-COM-DC}$	SDVO Receiver DC Common Mode Input Impedance		40	50	60	Ω
$Z_{RX-COM-INITIAL-DC}$	SDVO Receiver Initial DC Common Mode Input Impedance	Impedance allowed when receiver terminations are first turned on	5	50	60	Ω
$Z_{RX-COM-High-IMP-DC}$	SDVO Receiver Powered Down DC Common Mode Input Impedance	Impedance allowed when receiver terminations are not powered	20k		200k	Ω
V_{PP_TVCLK}	TVCLK Differential Pk – Pk Output Voltage		0.8		1.2	V
V_{SDOL} [1]	SPD (serial port data) Output Low Voltage	I_{OL} = 2.0 mA			0.4	V
V_{SPIH} [2]	Serial Port (SPC, SPD) Input High Voltage		2.0		+5V +0.5	V
V_{SPIL} [2]	Serial Port (SPC, SPD) Input Low Voltage		GND-0.5		0.4	V
V_{HYS}	Hysteresis of Serial Port Inputs		0.25			V
V_{DDCIH}	DDC Serial Port Input High Voltage		4.0		+5V +0.5	V
V_{DDCIL}	DDC Serial Port Input Low Voltage		GND-0.5		0.4	V
V_{PROMIH}	PROM Serial Port Input High Voltage		4.0		+5V +0.5	V
V_{PROMIL}	PROM Serial Port Input Low Voltage		GND-0.5		0.4	V
V_{SD_DDCOL} [3]	SPD (serial port data) Output Low Voltage from SD_DDC (or SD_EPROM)	Input is V_{INL} at SD_DDC or SD_EPROM. 4.0kΩ pullup to 2.5V.			$0.9*V_{INL}$ + 0.25	V
V_{DDCOL} [4]	SC_DDC and SD_DDC Output Low Voltage	Input is V_{INL} at SPC and SPD. 5.6kΩ pullup to 5.0V.			$0.933*V_{INL}$ + 0.35	V
$V_{EPROMOL}$ [5]	SC_EPROM and SD_EPROM Output Low Voltage	Input is V_{INL} at SPC and SPD. 5.6kΩ pullup to 5.0V.			$0.933*V_{INL}$ + 0.35	V

Symbol	Description	Test Condition	Min	Typ	Max	Unit
$V_{MISC1IH}$ [6]	RESET* Input High Voltage		2.7		VDD33 + 0.5	V
$V_{MISC1IL}$ [6]	RESET* Input Low Voltage		GND-0.5		0.5	V
$V_{MISC2IH}$ [7]	AS, BSCAN, T3 Input High Voltage		2.0		VDD25 + 0.5	V
$V_{MISC2IL}$ [7]	AS, BSCAN, T3 Input Low Voltage	DVDD=2.5V	GND-0.5		0.5	V
I_{PU}	AS, RESET* Pull Up Current	V_{IN} = 0V	10		30	µA
I_{PD}	BSCAN, T3 Pull Down Current	V_{IN} = 2.5V	10		30	µA
V_{SYNCOH} [8]	CHSYNC, VSYNC Output High Voltage	I_{OH} = -0.4mA	2.0			V
V_{SYNCOL} [8]	CHSYNC, VSYNC Output Low Voltage	I_{OL} = 3.2mA			0.4	V
DL_{OH}	DL[3:1] Output High Voltage	100kΩ load	3.5		5.0	V
DL_{OM}	DL[3:1] Output Mid Voltage	100kΩ load	1.4	2.0	2.4	V
DL_{OL}	DL[3:1] Output Low Voltage	100kΩ load	0		0.8	V
Z_{DL}	DL[3:1] Output Impedance	DC	7	10	13	kΩ

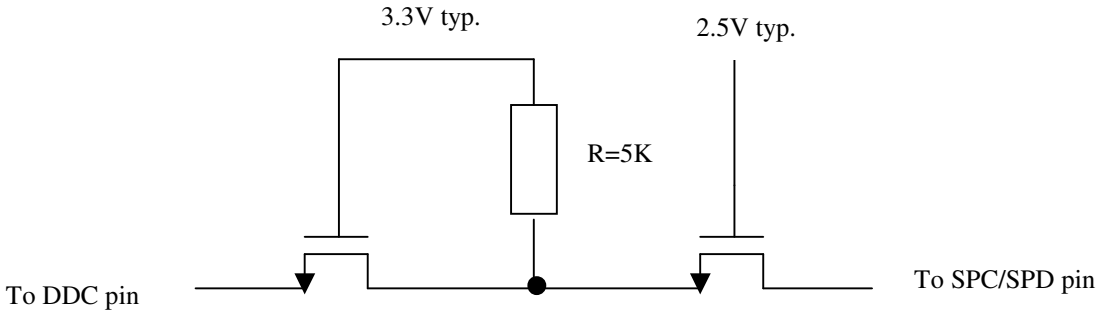
Notes:

1. V_{SDOL} is the SPD output low voltage when transmitting from internal registers, not from DDC or EEPROM.
2. V_{SPIH} and V_{SPIL} are the serial port (SPC and SPD) input low voltage when transmitting to internal registers. Separate requirements may exist for transmission to the DDC and EEPROM.
3. V_{SD_DDCOL} is the output low voltage at the SPD pin when the voltage at SD_DDC or SD_EPROM is V_{INL}. Maximum output voltage has been calculated with a worst case pullup of 4.0kΩ to 2.5V on SPD.
4. V_{DDCOL} is the output low voltage at the SC_DDC and SD_DDC pins when the voltage at SPC and SPD is V_{INL}. Maximum output voltage has been calculated with 5.6k pullup to 5V on SC_DDC and SD_DDC.
5. $V_{EPROMOL}$ is the output low voltage at the SC_EPROM and SD_EPROM pins when the voltage at SPC and SPD is V_{INL}. Maximum output voltage has been calculated with 5.6kΩ pullup to 5V on SC_EPROM and SD_EPROM.
6. V_{MISC1} - refers to RESET* input which is 3.3V compliant.
7. V_{MISC2} - refers to AS, BSCAN, T3 which are 2.5V compliant
8. V_{SYNC} – refers to CHSYNC and VSYNC outputs.

4.5 AC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
UI_{DATA}	SDVO Receiver Unit Interval for Data Channels		Typ. – 300ppm	1/[Data Transfer Rate]	Typ. + 300ppm	ps
f_{SDVO_CLK}	SDVO CLK Input Frequency		100		200	MHz
f_{PIXEL}	SDVO Receiver Pixel frequency		25		165	MHz
f_{SYMBOL}	SDVO Receiver Symbol frequency		1		2	GHz
t_{RX-EYE}	SDVO Receiver Minimum Eye Width		0.4			UI
$t_{RX-EYE-JITTER}$	SDVO Receiver Max. time between jitter median and max. deviation from median				0.3	UI
$V_{RX-CM-ACp}$	SDVO Receiver AC Peak Common Mode Input Voltage				150	mV
$RL_{RX-DIFF}$	Differential Return Loss	50MHz – 1.25GHz	15			dB
RL_{RX-CM}	Common Mode Return Loss	50MHz – 1.25GHz	6			dB
T_{SPR}	SPC, SPD Rise Time (20% - 80%)	Standard mode 100k Fast mode 400k 1M running speed			1000 300 150	ns ns ns
T_{SPF}	SPC, SPD Fall Time (20% - 80%)	Standard mode 100k Fast mode 400k 1M running speed			300 300 150	ns ns ns
T_{PROMR}	SC_PROM, SD_PROM Rise Time (20% - 80%)	Fast mode 400K			300	ns
T_{PROMF}	SC_PROM, SD_PROM Rise Time (20% - 80%)	Fast mode 400K			300	ns
T_{DDCR}	SC_DDC, SD_DDC Rise Time (20% - 80%)	Standard mode 100k			1000	ns
T_{DDCF}	SC_DDC, SD_DDC Fall Time (20% - 80%)	Standard mode 100k			300	ns
$T_{DDCR-DELAY}$[1]	SC_DDC, SD_DDC Rise Time Delay (50%)	Standard mode 100k		0		ns
$T_{DDCF-DELAY}$[1]	SC_DDC, SD_DDC Fall Time Delay (50%)	Standard mode 100k		3		ns
t_{SKEW}	SDVO Receiver Total Lane to Lane Skew of Inputs	Across all lanes			2	ns
t_R	CHSYNC and VSYNC (when configured as outputs) Output Rise Time (20% - 80%)	15pF load DVDD = 2.5V			1.50	ns
t_F	H and V (when configured as outputs) Output Fall Time (20% - 80%)	15pF load DVDD = 2.5V			1.50	ns

Notes:
1. Refers to the figure below, the delay refers to the time pass through the internal switches.



5.0 Package Dimensions

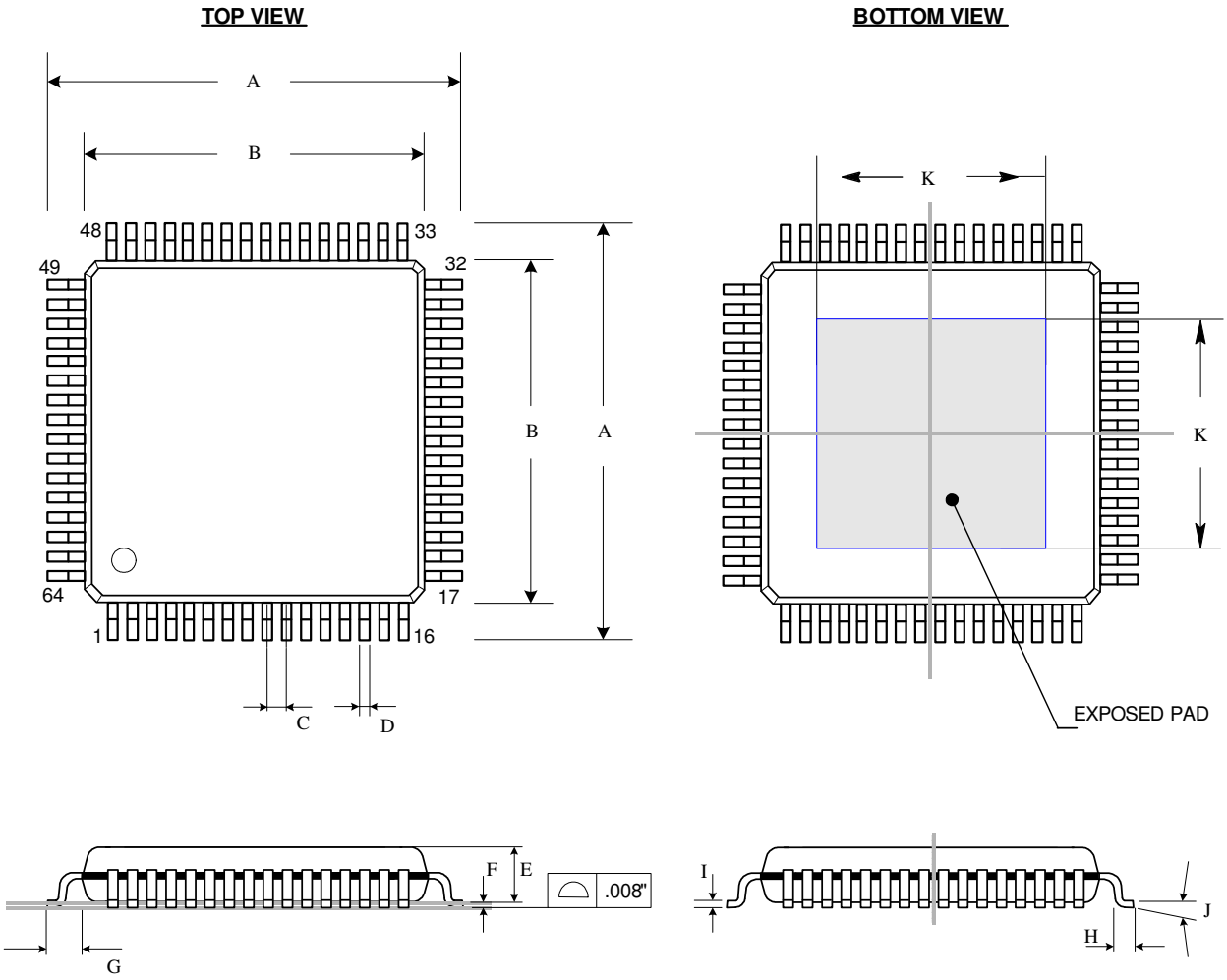


Figure 6: 64 Pin LQFP (Exposed Pad) Package

Table of Dimensions

No. of Leads		SYMBOL										
64 (10 X 10 mm)		A	B	C	D	E	F	G	H	I	J	K
Milli-meters	MIN	12	10	0.50	0.17	1.35	0.05	1.00	0.45	0.09	0°	5.85
	MAX				0.27	1.45	0.15		0.75	0.20	7°	7

Notes:

1. Conforms to JEDEC standard JESD-30 MS-026D.
2. Dimension B: Top Package body size may be smaller than bottom package size by as much as 0.15 mm.
3. Dimension B does not include allowable mold protrusions up to 0.25 mm per side.

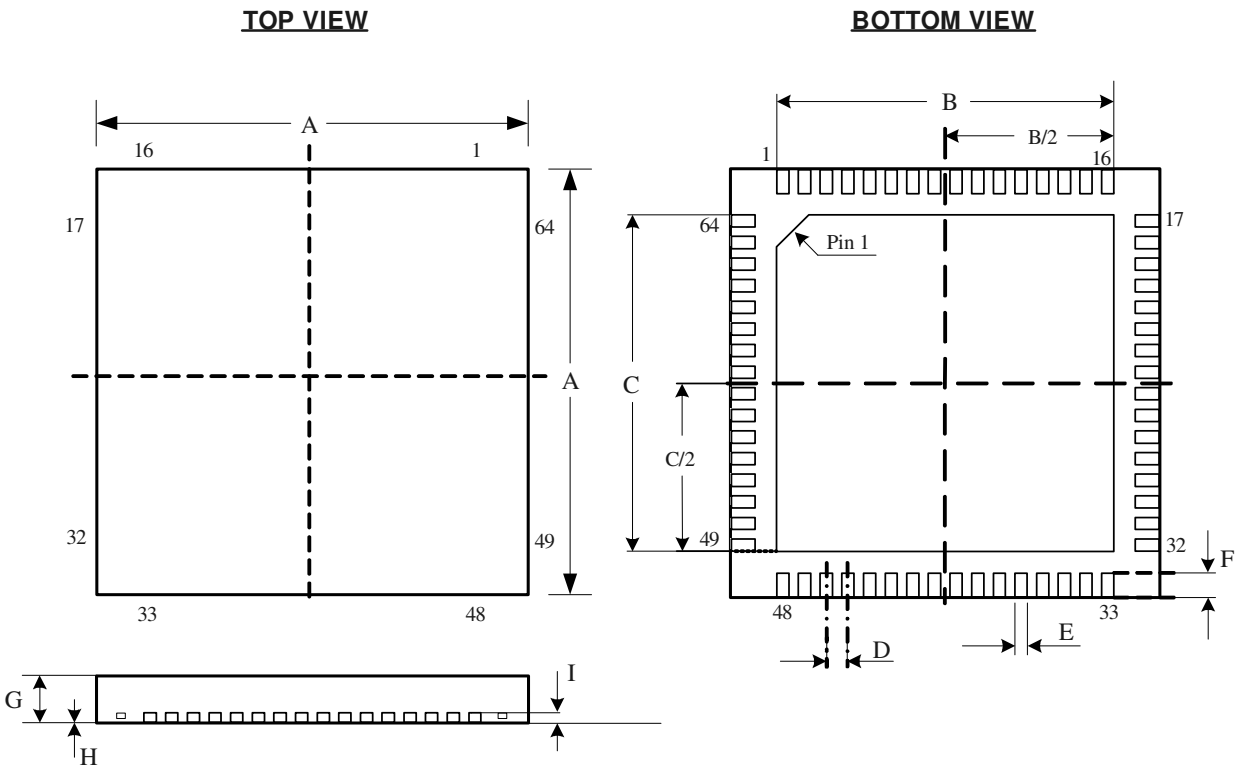


Figure 7: 64 Pin QFN Package (8 x 8 x 0.8mm)

Table of Dimensions

No. of Leads		SYMBOL								
64 (8 X 8 mm)		A	B	C	D	E	F	G	H	I
Milli-meters	MIN	8	6.1	6.1	0.4	0.15	0.35	0.7	0	0.203
	MAX		6.3	6.3		0.25	0.45	0.8	0.05	

Notes:

1. Conforms to JEDEC standard JESD-30 MO-220.

6.0 Revision History

Table 10: Revisions

Rev. #	Date	Section	Description
1.0	3/21/05	All	First official release.
1.1	4/28/05	4.3	Updated symbol names and descriptions
	4/28/05	4.4	Changed DL_{OM} limits
1.2	9/14/05	Figure 1	Added video switch
	9/14/05	4.2	Added reset specification
	9/14/05	1.2	Added “10k resistor” to descriptions of pin 3, 4, 5.
	10/12/05	4.4, 4.5	Updated descriptions of SPD, SPC, DDC, and PROM
1.22	4/6/07	4.3	Updated section 4.3 Electrical Characteristics
1.3	10/3/07	1.1, 5.0	Added a 64-QFN package.
1.31	10/26/07	4.4	Change VDD5+ to +5V
2.0	3/21/08	All	Combined CH7021 and CH7022.
2.1	4/21/08	Ordering Information	Added 64 QFN package for CH7022A
2.2	10/30/08	4.2	Added Ambient operating temperature.
2.3	03/02/10	Features, Table3	Make some description more clear.
2.4	05/10/10	Figure 1, Table 1	Make some pin type clear.
2.5	06/07/11	4.1, 4.2, 4.3	Update ambient operating temperature to industrial standard.

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ORDERING INFORMATION

Part Number	Package Type	Number of Pins	Voltage Supply
CH7021A-TEF	Lead Free LQFP with exposed pad	64	2.5V & 3.3V
CH7021A-TEF-TR	Lead Free LQFP with exposed pad in Tape & Reel	64	2.5V & 3.3V
CH7021A-BF	Lead Free QFN	64	2.5V & 3.3V
CH7021A-BF-TR	Lead Free QFN in Tape & Reel	64	2.5V & 3.3V
CH7022A-TEF	Lead Free LQFP with exposed pad	64	2.5V & 3.3V
CH7022A-TEF-TR	Lead Free LQFP with exposed pad in Tape & Reel	64	2.5V & 3.3V
CH7022A-BF	Lead Free QFN	64	2.5V & 3.3V
CH7022A-BF-TR	Lead Free QFN in Tape & Reel	64	2.5V & 3.3V

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