HIGH-SPEED CMOS 8-BIT IDENTITY COMPARATOR

IDT54AHCT521

Integrated Device Technology, Inc.

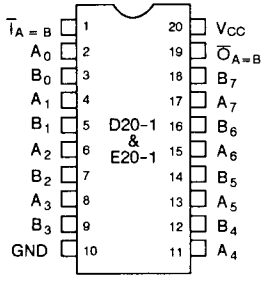
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 9ns typical propagation delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- 8-bit identity comparator
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

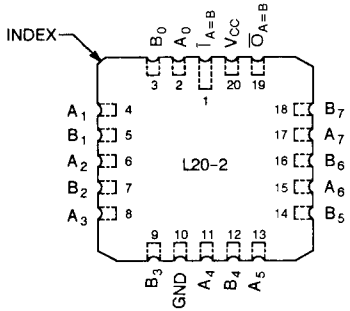
DESCRIPTION:

The IDT54AHCT521 is an 8-bit identity comparator built using advanced CEMOS™, a dual metal CMOS technology. The device compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active LOW enable input.

PIN CONFIGURATIONS

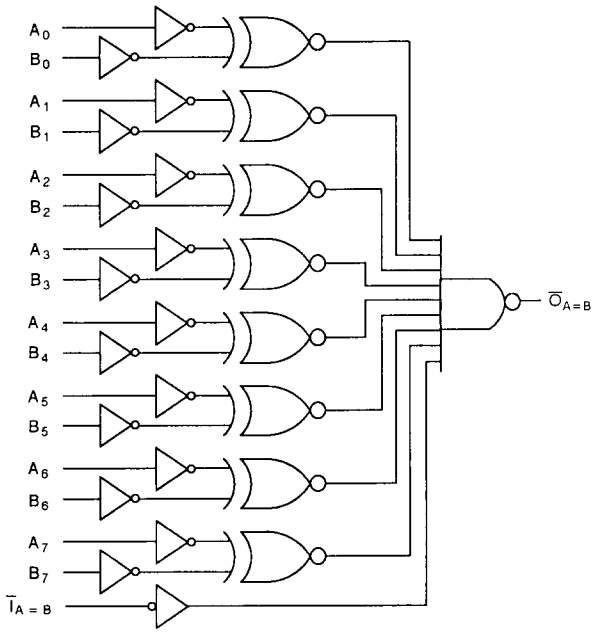


DIP/CERPACK TOP VIEW



LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



10

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
T_A = -55°C to +125°C
V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 14mA	–	–	0.4	

NOTES:

1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_I = 0		–	0.001	1.5	mA
I_{CCT}	Power Supply Current Per TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[5]	V_{CC} = Max. Output Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Output Open f_I = 1.0MHz, 50% Duty Cycle On Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	–	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	0.4	2.8	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = ClockFrequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.
5. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$A_0 - A_7$	Word A Inputs
$B_0 - B_7$	Word B Inputs
$\overline{I}_{A=B}$	Expansion or Enable Input (Active LOW)
$\overline{O}_{A=B}$	Identity Output (Active LOW)

TRUTH TABLE

INPUTS		OUTPUT
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

H = HIGH Voltage Level
L = LOW Voltage Level
*$A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

10

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	TYP.	MIN.[2]	MAX.	UNIT
t_{PLH} t_{PHL}	Propagation Delay A_N or B_N to $\overline{O}_{A=B}$	C_L = 50pF R_L = 500Ω	9.0	–	17.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$		5.0	–	11.0	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

ORDERING INFORMATION