S-34 ORIG

SS-5-1032
SS-6-1032

002648

T-2648 G1

Variable Length Static Shift Registers

FEATURES

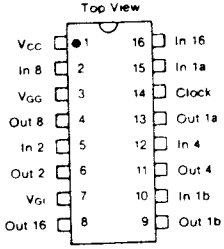
- TTL/DTL Compatible Clock Input
- TTL/DTL Compatible Data—
  No external interfacing components required on data inputs or outputs.
- DC-1MHz Operation
- Full Static Operation—
  Data is stored independently of the clock logic level.
- Two Temperature Ranges—
  SS-5: 0°C to +70°C
  SS-6: -55°C to +125°C
- Zener Protected Inputs
- Glass Passivation Protection

DESCRIPTION

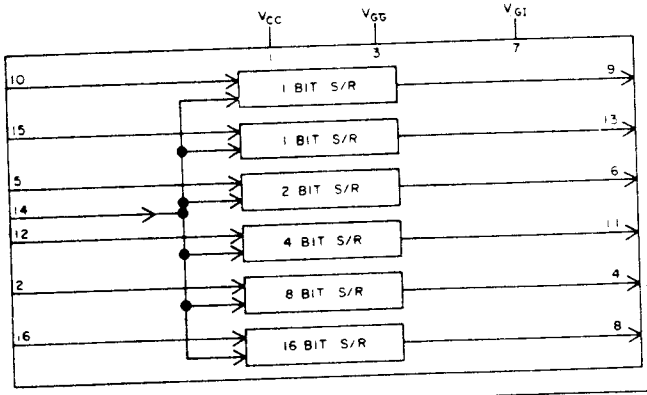
The SS-5-1032 and SS-6-1032 are 32-bit static shift registers consisting of 1, 1, 2, 4, 8 and 16-bit individual registers with common clock and separate data inputs and outputs. The device is constructed on a monolithic chip utilizing P-Channel enhancement mode transistors. It is compatible with TTL/DTL and MOS logic without the use of any special interface components.

PIN CONFIGURATION

16 LEAD DUAL IN LINE



BLOCK DIAGRAM



TIMING DIAGRAM

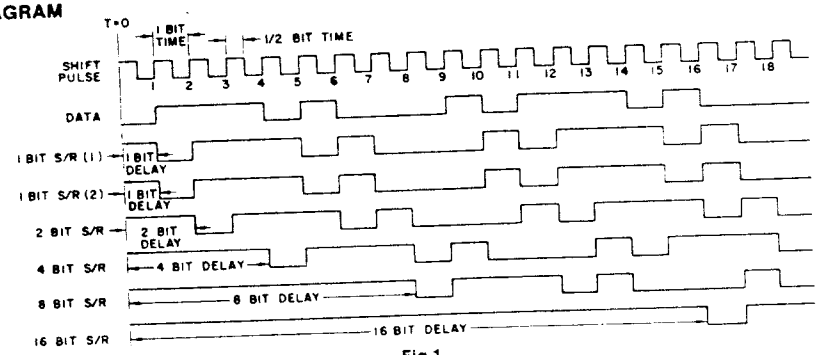


Fig.1

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GI} and V_{GG} (with respect to V_{CC}) ..... -20V to +0.3V
Clock and Logic Input Voltages (with respect to V_{CC}) ... -15V to +0.3V
Storage Temperature ..... -55°C to +150°C
Operating Temperature SS-5-1032 ..... 0°C to +70°C
SS-6-1032 ..... -55°C to +125°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

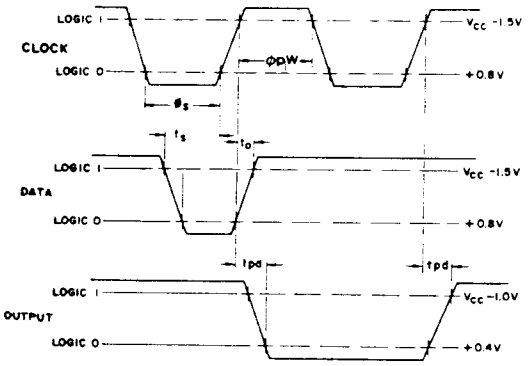
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±0.5 Volts (V_{CC} = Substrate voltage)
V_{GG} = -12 Volts ±1 Volt
V_{GI} = GND
Operating Temperature (T_A) = 0°C to +70°C (SS-5-1032)
= -55°C to +125°C (SS-6-1032)

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Input (See Fig.2)					
Repetition Rate	DC	—	1	MHz	
Clock Pulse Width (ϕpW)	450	—	—	ns	
Pulse Separation (ϕs)	450	—	—	ns	
Logic Levels					
Logic '0'	—	—	+0.8	V	
Logic '1'	(V_{CC}-1.5)	—	—	V	
Input Capacitance	—	10	20	pF	Measured at $V_{in} = V_{CC}$
Input Impedance	1.0	—	—	MΩ	
Rise and Fall Time	—	—	1	μs	
Noise Immunity	+0.4	—	—	V	
Data Input (See Fig.2)					
Pulse Width (SD_w)	200	—	—	ns	
Set Up Time, t_s	200	—	—	ns	
Data Overlap, t_o	25	—	—	ns	
Logic Levels					
Logic '0'	—	—	+0.8	V	
Logic '1'	(V_{CC}-1.5)	—	—	V	
Input Capacitance	—	5	10	pF	Measured at $V_{in} = V_{CC}$
Input Impedance	1.0	—	—	MΩ	
Noise Immunity	+0.4	—	—	V	
Data Output (See Fig.2)					
Logic '0'	—	—	-0.4	V	1_{OL} = 1.6mA
Logic '1'	(V_{CC}-1.0)	—	—	—	1_{OH} = 100 μA
Propagation Delay,	—	—	450	ns	See Fig.2
Total Power Consumption	—	200	—	mW	Nominal Power Supply

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAM



The data is clocked in during the Logic "0" state of the clock and should be present and stable in its required state for 200 nsec with 25 nsec after the clock changes from logic "0" to "1". The data in the register will shift toward the output upon the positive transition of the clock.

Fig.2