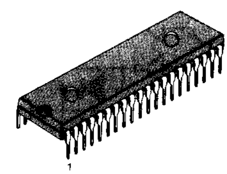
QUAD UNIVERSIAL ASYNCHRONOUS RECEIVER AND TRANSMITTER

The KS5812, QUAD-UART, is a Si-Gate CMOS IC which provides the data formatting and control to interface serial asynchronous data communications between main system and subsystems.

The parallel data of the bus system is serially transmitted and by the asynchronous data interface with proper formatting and error checking. The KS5812 includes Transmit part, Receive part, Programmable control part, Status check part, and Select part. The control register that is programmed via the data bus during system initialization, provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control.

40 DIP



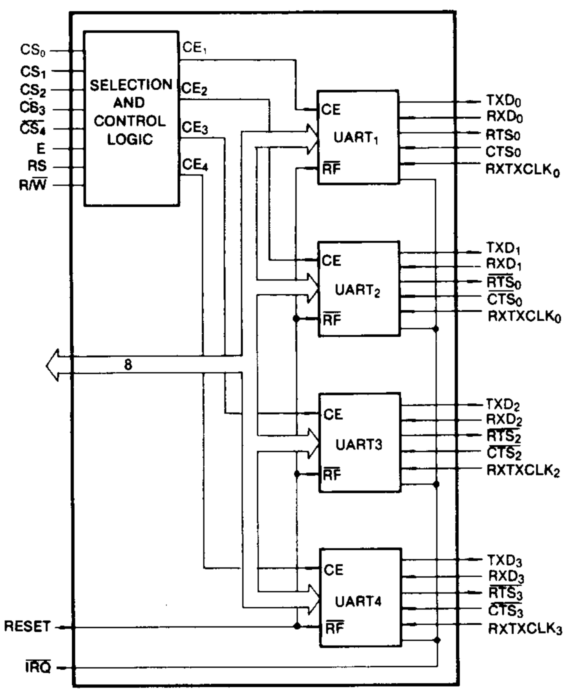
FEATURES

- **Low power, High speed CMOS process.**
- **Serial/Parallel conversion of Data**
- **8-and 9-bit Transmission**
- **Optional Even and Odd Parity**
- **Parity, Overrun and Framing Error Checking**
- **Programmable Control Register**
- **Optional ÷1, ÷16, and ÷64 Clock Modes**
- **Peripheral/Modem Control Functions**
- **Double Buffered**
- **One-or Two-Stop Bit Operation**

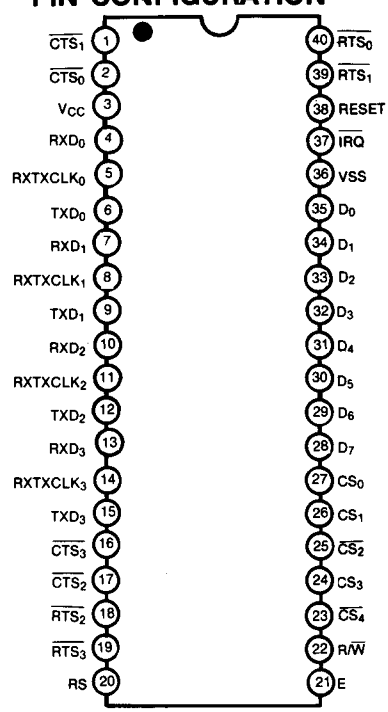
ORDERING INFORMATION

Device	Package	Operating Temperature
KS5812	40 DIP	−20 ~ +75°C

BLOCK DIAGRAM



PIN CONFIGURATION



UART BLOCK DIAGRAM

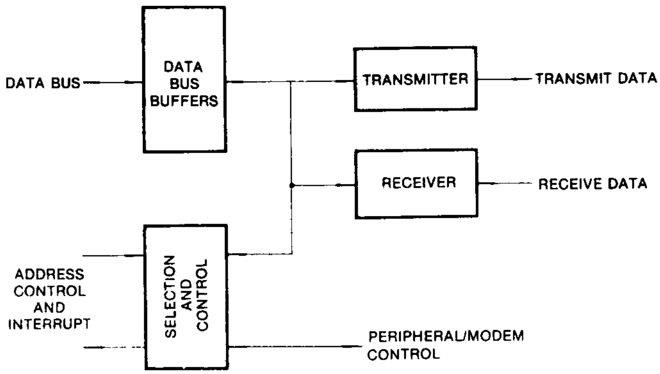


Fig. 3

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ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage*	V_{DD}*	−0.3 to +7.0	V
Input Voltage*	V_I*	−0.3 to +7.0	V
Maximum Output Current**	$I_{O\,(MAX)}$	10	mA
Operating Temperature	T_{OPR}	−20 to +75	°C
Storage Temperature	T_{STG}	−55 to +150	°C

*With respect to V_{SS} (System GND)

**Maximum output current is the maximum current which can flow out from one output terminal or I/O common terminal ($D_0 \sim D_7$, $\overline{RTS}$, Tx Data, $\overline{IRQ}$)

(Note) Permanent IC damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If they are exceeded, it could affect the reliability of the IC.

RECOMMENDED OPERATING CONDITIONS (Ta = 25°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{DD}*	4.5	5.0	5.5	V
Input "Low" Voltage		V_{IL}*	0	—	0.8	V
Input "High" Voltage	$D_0 \sim D_7$, RS, $\overline{CTS_i}$, RxD_i	V_{IH}*	2.0	—	V_{CC}	V
	CS_0, CS_2, CS_1, R/$\overline{W}$, E, CS_3, $\overline{CS_4}$, $RXTXCLK_i$		2.2	—	V_{CC}	
Operating Temperature		T_{opr}	−20	25	75	°C

* With respect to V_{SS} (System GND)

DC CHARACTERISTICS (V_{DD} = +5V ± 5%, V_{SS} = 0V, Ta = −20 ~ +75°C, unless otherwise noted.)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Input "High" Voltage	$D_0 \sim D_7$, RS, CTSi,	V_{IH}		2.0	—	V_{CC}	V
	CS_0, CS_2, CS_1, $R/\overline{W}$, E, CS_3, $\overline{CS_4}$ RXTXCLKi			2.2	—	V_{CC}	
Input "Low" Voltage	All inputs	V_{IL}		−0.3	—	0.8	V
Input Leakage Current	$R/\overline{W}$, CS_0, CS_1, CS_2, E, CS_3, $\overline{CS_4}$	$I_{I(LKG)}$	$V_{IN} = 0 \sim V_{CC}$	−2.5	—	2.5	μA
Three-State (Off State) Input Current	$D_0 \sim D_7$	$I_{I(3\ STATE)}$	$V_{IN} = 0.4 \sim V_{CC}$	−10	—	10	μA
Output "High" Voltage	$D_0 \sim D_7$	V_{OH}	$I_{OH} = -400\mu A$	4.1	—	—	V
			$I_{OH} \leq -10\mu A$	V_{CC}-0.1	—	—	
	TXDi, $\overline{RTSi}$		$I_{OH} = -400$	4.1	—	—	
			$I_{OH} \leq -10\mu A$	V_{CC}-0.1	—	—	
Output "Low" Voltage	All outputs	V_{OL}	$I_{OH} = 1.6mA$	—	—	0.4	V
Output Leakage Current (off state)	$\overline{IRQ}$	$I_{O(LKG)}$	$V_{OH} = V_{CC}$	—	—	10	μA
Input Capacitance	$D_0 \sim D_7$	C_I	V_{IN} = 0V, Ta = 25°C f = 1.0 MHz	—	—	12.5	pF
	E, RXTXCLKi, $R/\overline{W}$, RS, RXDi, CS_0, CS_1, CS_2, CTS, CS_3, $\overline{CS_4}$			—	—	7.5	
Output Capacitance	$\overline{RTS}$, TXDi	C_O	V_{IN} = 0V, Ta = 25°C f = 1.0 MHz	—	—	10	pF
	$\overline{IRQ}$			—	—	5.0	
Operating Current	• Under transmitting and Receiving operation • 500 kbps • Data bus in $R/\overline{W}$ operation	I_{DD}	E = 1.0 MHz	—	—	3	mA
			E = 1.5 MHz	—	—	4	
			E = 2.0 MHz	—	—	5	
	• Chip is not selected • 500 kbps • Under non transmitting and receiving operation • Input level (Except E) V_{IH} min = $V_{CC} - 0.8V$ V_{IL} max = 0.8V		E = 1.0 MHz	—	—	200	μA
			E = 1.5 MHz	—	—	250	
			E = 2.0 MHz	—	—	300	

AC CHARACTERISTICS (V_{DD} = 5.0V ± 5%, V_{SS} = 0V, Ta = −20 ~ +75°C, unless otherwise noted.)

1. TIMING OF DATA TRANSMISSION

Characteristic		Symbol	Test Conditions	Min	Max	Unit
Minimum Clock Pulse Width	÷1 Mode	$t_{WCK\ (MIN)\ L}$	Fig. 4	900	—	ns
	÷16, ÷64 Modes			600	—	ns
	÷1 Mode	$t_{WCK\ (MIN)\ H}$	Fig. 5	900	—	ns
	÷16, ÷64 Modes			600	—	ns
Clock Frequency	÷1 Mode	f_{CK}		—	500	KHz
	÷16, ÷64 Modes			—	800	KHz
Clock-to-Data Delay for Transmitter		$t_{DCK\ (TX)}$	Fig. 6	—	600	ns
Receive Data Setup Time	÷1 Mode	$t_{SU\ (RX)}$	Fig. 7	250	—	ns
Receive Data Hold Time	÷1 Mode	$t_{H\ (RX)}$	Fig. 8	250	—	ns
$\overline{IRQ}$ Release Time		$t_{RL\ (\overline{IRQ})}$	Fig. 9	—	1200	ns
$\overline{RTS}$ Delay Time		$t_{D\ (\overline{RTS})}$	Fig. 9	—	560	ns
Rise Time and Fall Time	Except E	t_R, t_F		—	1000*	ns

* 1.0μs or 10% of the pulse width, whichever is smaller.

2. BUS TIMING CHARACTERISTICS

1) READ

Characteristic	Symbol	Test Conditions	Min	Max	Unit
Enable Cycle Time	$t_{CY\ (E)}$	Fig. 10	1000	—	ns
Enable "High" Pulse Width	$t_{WH\ (E)}$	Fig. 10	450	—	ns
Enable "Low" Pulse Width	$t_{WL\ (E)}$	Fig. 10	430	—	ns
Setup Time, Address and R/$\overline{W}$ Valid to Enable Positive Transition	$t_{SU\ (AD\text{-}R/W)}$	Fig. 10	80	—	ns
Data Delay Time	$t_{D\ (DATA)}$	Fig. 10	—	290	ns
Data Hold Time	$t_{H\ (DATA)}$	Fig. 10	20	100	ns
Address Hold Time	$t_{H\ (ADD)}$	Fig. 10	10	—	ns
Rise and Fall Time for Enable Input	$t_{R\ (E)}$, $t_{F\ (E)}$	Fig. 10	—	25	ns

2) WRITE

Characteristic	Symbol	Test Conditions	Min	Max	Unit
Enable Cycle Time	$t_{CY (E)}$	Fig. 11	1000	—	ns
Enable "High" Pulse Width	$t_{WH (E)}$	Fig. 11	450	—	ns
Enable "Low" Pulse Width	$t_{WL (E)}$	Fig. 11	430	—	ns
Setup Time, Address and R/$\overline{W}$ Valid to Enable Positive Transition	$t_{SU (AD\text{-}R/W)}$	Fig. 11	80	—	ns
Data Setup Time	$t_{SU (DATA)}$	Fig. 11	165	—	ns
Data Hold Time	$t_{H (DATA)}$	Fig. 11	10	—	ns
Address Hold Time	t_{AH}	Fig. 11	10	—	ns
Rise and Fall Time for Enable Input	$t_{R (E)}, t_{F (E)}$	Fig. 11	—	25	ns

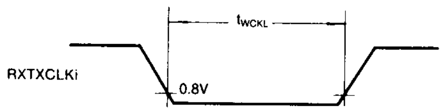


Fig. 4 Clock Pulse Width, "Low" State

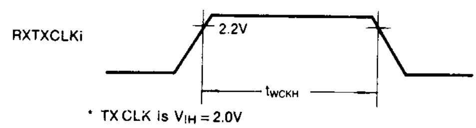


Fig. 5 Clock Pulse Width, "High" State

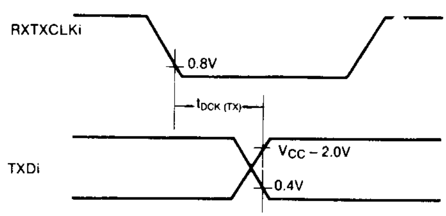


Fig. 6 Transmit Data Output Delay

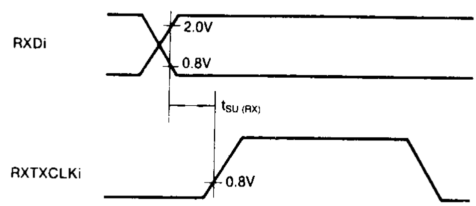


Fig. 7 Receive Data Setup Time (÷1 Mode)

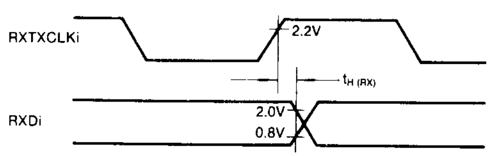
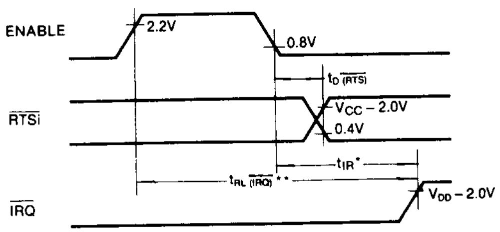


Fig. 8 Receive Data Hold Time (÷1 Mode)



* (1) $\overline{IRQ}$ Release Time applied to R_xDi Register read operation
(2) $\overline{IRQ}$ Release Time applied to T_xDi Register write operation
(3) $\overline{IRQ}$ Release Time applied to control Register write TIE = 0, RIE = 0 operation.

** $\overline{IRQ}$ Release Time applied to R_x Data Register read operation right after read status register, when $\overline{IRQ}$ is asserted by DCD rising edge.

Note: Note that the following takes place when $\overline{IRQ}$ is asserted by the detection of transmit data register empty status. $\overline{IRQ}$ is released to "High" asynchronously with E signal when $\overline{CTSi}$ goes "High".

Fig. 9 $\overline{RTSi}$ Delay and $\overline{IRQ}$ Release Time

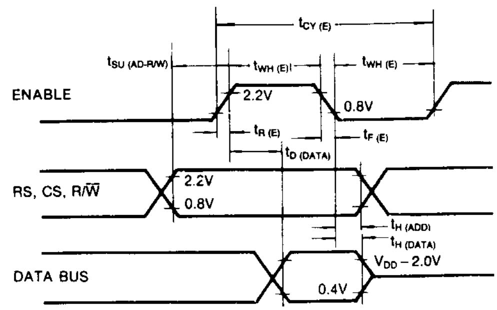


Fig. 10 Bus Read Timing Characteristics (Read information from UART)

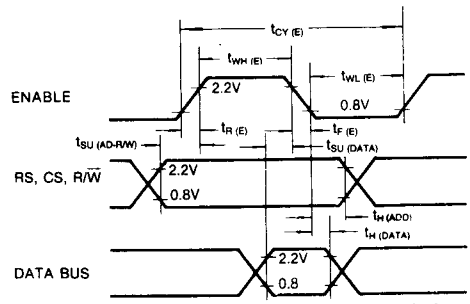


Fig. 11 Bus Write Timing Characteristics (Write information into UART)

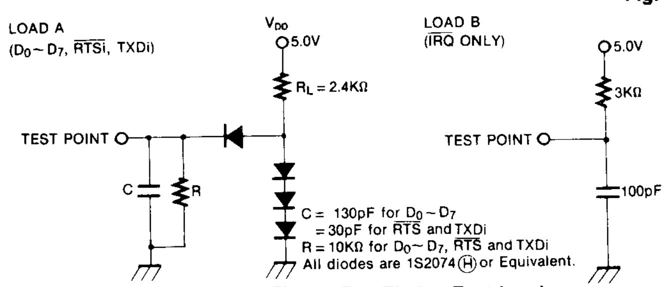


Fig. 12 Bus Timing Test Loads

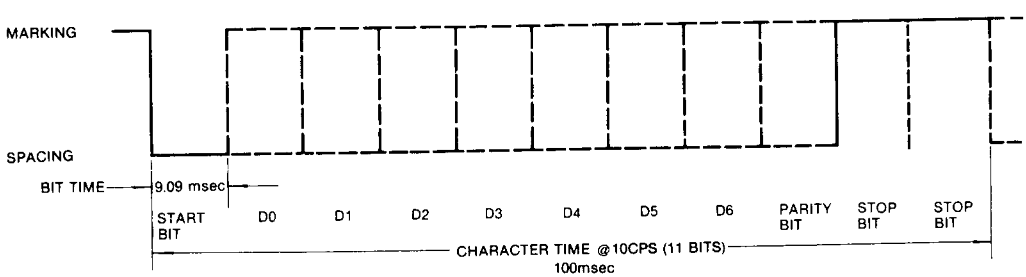


Fig. 13 Baud Serial ASCII Data Timing

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APPLICATION INFORMATION DEVICE OPERATION

At the bus interface, the UARTi appears as two addressable memory locations. Internally, there are four registers: two read-only and two write-only registers. The read-only registers are Status and Receive Data; the write-only registers are Control and Transmit Data. The serial interface consists of serial input and output lines with independent clocks, and three peripheral/modem control lines.

1. POWER ON/MASTER RESET

The master reset (CR0, CR1) should be set during system initialization to insure the reset condition and prepare for programming the UARTi functional configuration when the communications channel is required. During the first master reset, the $\overline{IRQ}$ and $\overline{RTSi}$ outputs are held at level 1. On all other master resets, the $\overline{RTSi}$ output can be programmed high or low with the $\overline{IRQ}$ output held high. Control bits CR5 and CR6 should also be programmed to define the state of $\overline{RTSi}$ whenever master reset is utilized. The UARTi also contains internal power-on reset logic to detect the power line turn-on transition and hold the chip in a reset state to prevent erroneous output transitions prior to initialization. This circuitry depends on clean power turn-on transitions. The power-on reset is released by means of the bus-programmed master reset which must be applied prior to operating the UARTi. After master resetting the UARTi, the programmable Control Register can be set for a number of options such as variable clock divider ratios, variable word length, one or two stop bits, parity (even, odd, or none), etc.

2. TRANSMIT

A typical transmitting sequence consists of reading the UARTi. Status Register either as a result of an interrupt or in the UARTi's turn in a polling sequence. A character may be written into the Transmit Data Register if the status read operation has indicated that the Transmit Data Register is empty. This character is transferred to Shift Register where it is serialized and transmitted from the Transmit Data output preceded by a start bit and followed by one or two stop bits. Internal parity (odd or even) can be optionally added to the character and will occur between the last data bit and the first stop bit. After the first character is written in the Data Register, the Status Register can be read again to check for a Transmit Data Register Empty condition and current peripheral status. If the|Register is empty, another character can be loaded for transmission even though the first character is in the process of being transmitted (because of double buffering). The second character will be automatically transferred into the Shift Register when the first character transmission is completed. This sequence continues until all the characters have been transmitted.

3. RECEIVE

Data is received from a peripheral by means of the Receive Data input. A divide-by-one clock ratio is provided for an externally synchronized clock (to its data) while the divide by-16 and 64 ratios are provided for internal synchronization. Bit synchronization in the divide-by-16 and 64 modes is initiated by the detection of 8 or 32 low samples on the receive line in the divide-by-16 and 64 modes respectively. False start bit deletion capability insures that a full half bit of a start bit has been received before the internal clock is synchronized to the bit time. As a character is being received, parity (odd or even) will be checked and the error indication will be available in the Status Register along with framing error, overrun error, and Receive Data Register full. In a typical receiving sequence, the Status Register is read to determine if a character has been received from a peripheral. If the Receiver Data Register is full, the character is placed on the 8-bit UARTi bus when a Read Data command is received from the MPU. When parity has been selected for a 7-bit word (7 bits plus parity), the receiver strips the parity bit (D7 = 0) so that data alone is transferred to the MPU. This feature reduces MPU programming. The Status Register can continue to be read to determine when another character is available in the Receive Data Register. The receiver is also double buffered so that a character can be read from the data register as another character is being received in the shift register. The above sequence continues until all characters have been received.

INPUT/OUTPUT FUNCTIONS

1. UART INTERFACE SIGNALS FOR MPU

The KS5812 interfaces to the MPU with an 8-bit bidirectional data bus, five chip select lines, a register select line, an interrupt request line, read/write line, and enable line. These signals permit the MPU to have complete control over the KS5812.

UART Bidirectional Data (D0-D7) — The bidirectional data lines (D0-D7) allow for data transfer between the KS5812 and the MPU. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an UARTi read operation.

UART Enable (E) — The Enable signal, E, is a high-impedance TTL-compatible input that enables the bus input/output data buffers and clocks data to and from the KS5812.

Read/Write (R/$\overline{W}$) — The Read/Write line is a high-impedance input that is TTL compatible and is used to control the direction of data flow through the UARTi's input/output data bus interface. When Read/Write is high (MPU Read cycle), KS5812 output drivers are turned on and a selected register is read. When it is low, the KS5812 output drivers are turned off and the MPU writes into a selected register. Therefore, the Read/Write signal is used to select read-only or write-only registers within the KS5812.

Chip Select (CS0, CS1, CS2, CS3, $\overline{CS4}$) — These five high-impedance TTL-compatible input lines are to select and address the KS5812. Each UART can be enabled when CS2 and CS3 are high and $\overline{CS4}$ is low. CS0 and CS1 are used to select individual UART.

CS0	CS1	CS2	CS3	$\overline{CS4}$	UARTi
0	0	1	1	0	UART1
0	1	1	1	0	UART2
1	0	1	1	0	UART3
1	1	1	1	0	UART4

Register Select (RS) — The Register Select line is a high-impedance input that is TTL compatible. A high level is used to select the Transmit/Receive Data Registers and a low level the Control/Status Registers. The Read/Write signal line is used in conjunction with Register Select to select the read-only or write-only register in each register pair.

Interrupt Request ($\overline{IRQ}$) — Interrupt Request is a TTL-compatible, open-drain (no internal pullup), active low output that is used to interrupt the MPU. The $\overline{IRQ}$ output remains low as long as the cause of the interrupt is present and the appropriate interrupt enable within the KS5812 is set. The $\overline{IRQ}$ status bit, when high, indicates the $\overline{IRQ}$ output is in the active state.

Interrupts result from conditions in both the transmitter and receiver sections of the UARTi. The transmitter section causes an interrupt when the Transmitter Interrupt Enabled condition is selected (CR5•$\overline{CR6}$), and the Transmit Data Register Empty (TDRE) status bit is high. The TDRE status bit indicates the current status of the Transmitter Data Register except when inhibited by Clear-to-Send ($\overline{CTSi}$) being high or the UARTi being maintained in the Reset condition. The interrupt is cleared by writing data into the Transmit Data Register. The interrupt is masked by disabling the Transmitter Interrupt via CR5 or CR6 or by the loss of $\overline{CTSi}$ which inhibits the TDRE status bit. The Receiver section causes an interrupt when the Receiver Interrupt Enable is set and the Receive Data Register Full (RDRF) status bit is high, an Overrun has occurred. An interrupt resulting from the RDRF status bit can be cleared by reading data or resetting the UARTi. Interrupts caused by Overrun are cleared by reading the status register after the error condition has occurred and then reading the Receive Data Register or resetting the UARTi. The receiver interrupt is masked by resetting the Receiver Interrupt Enable.

2. CLOCK INPUTS

High-impedance TTL-compatible inputs are provided for clocking of transmitted and received data. Clock frequencies of 1, 16, or 64 times the data rate may be selected.

3. RECEIVE AND TRANSMITTER CLOCK (RXTXCLKi)

—The RXTXCLKi input are both used for the clocking of transmitted data and for synchronization of received data. (In the /1 mode, the clock and data must be synchronized externally.) The transmitter initiates data on the negative transition of the clock and the receiver samples the data on the positive transition of the clock.

4. SERIAL INPUT/OUTPUT LINES

Receive Data (RXDi) — The Receive Data line is a high-impedance TTL-compatible input through which data is received in a serial format. Synchronization with a clock for detection of data is accomplished internally when clock rates of 16 or 64 times the bit rate are used.

Transmit Data (TXDi) — The Transmit Data output line transfers serial data to a modem or other peripheral.

5. PERIPHERAL/MODEM CONTROL

The UARTi includes several functions that permit limited control of a peripheral or modem. The functions included are Clear-to-Send, Request-to-Send and Data Carrier Detect.

Clear-to-Send ($\overline{CTSi}$) — This high-impedance TTL-compatible input provides automatic control of the transmitting end of a communications link via the modem Clear-to-Send active low output by inhibiting the Transmit Data Register Empty (TDRE) status bit.

Request-to-Send ($\overline{RTSi}$) — The Request-to-Send output enables the MPU to control a peripheral or modem via the data bus. The $\overline{RTSi}$ output corresponds to the state of the Control Register bits CR5 and CR6. When CR6 = 0 or both CR5 and CR6 = 1, the $\overline{RTSi}$ output is low (the active state). This output can also be used for Data Terminal Ready (DTR).

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6. TRANSMIT DATA REGISTER (TDR)

Data is written in the Transmit Data Register during the negative transition of the enable (E) when the UARTi has been addressed with RS high and R/$\overline{W}$ low. Writing data into the register causes the Transmit Data Register Empty bit in the Status Register to go low. Data can then be transmitted. If the transmitter is idling and no character is being transmitted, then the transfer will take place within 1-bit time of the trailing edge of the Write command. If a character is being transmitted, the new data character will commence as soon as the previous character is complete. The transfer of data causes the Transmit Data Register Empty (TDRE) bit to indicate empty.

7. RECEIVE DATA REGISTER (RDR)

Data is automatically transferred to the empty Receive Data Register (RDR) from the receiver deserializer (a shift register) upon receiving a complete character. This event causes the Receive Data Register Full bit (RDRF) in the status buffer to go high (full). Data may then be read through the bus by addressing the UARTi and selecting the Receive Data Register with RS and R/$\overline{W}$ high when the UARTi is enabled. The non-destructive read cycle causes the RDRF bit to be cleared to empty although the data is retained in the RDR. The status is maintained by RDRF as to whether or not the data is current. When the Receive Data Register is full, the automatic transfer of data from the Receiver Shift Register to the Data Register is inhibited and the RDR contents remain valid with its current status stored in the Status Register.

8. CONTROL REGISTER

The UARTi Control Register consists of eight bits of write-only buffer that are selected when RS and R/$\overline{W}$ are low. This register controls the function of the receiver, transmitter, interrupt enables, and the Request-to-Send peripheral/modem control output.

Counter Divide Select Bits (CR0 and CR1) — The Counter Divide Select Bits (CR0 and CR1) determine the divide ratios utilized in both the transmitter and receiver sections of the UARTi. Additionally, these bits are used to provide a master reset for the UARTi which clears the Status Register (except for external conditions on $\overline{CTSi}$ and $\overline{DCD}$) and initializes both the receiver and transmitter. Master reset does not affect other Control Register bits. Note that after power-on or a power fail/restart, these bits must be set high to reset the UARTi. After resetting, the clock divide ratio may be selected. These counter select bits provide for the following clock divide ratios:

CR1	CR0	Function
0	0	÷1
0	1	÷16
1	0	÷64
1	1	Master Reset

Word Select Bits (CR2, CR3, and CR4) — The Word Select bits are used to select word length, parity, and the number of stop bits. The encoding format is as follows;

CR4	CR3	CR2	Function
0	0	0	7 Bits + Even Parity + 2 Stop Bits
0	0	1	7 Bits + Odd Parity + 2 Stop Bits
0	1	0	7 Bits + Even Parity + 1 Stop Bit
0	1	1	7 Bits + Odd Parity + 1 Stop Bit
1	0	0	8 Bits + 2 Stop Bits
1	0	1	8 Bits + 1 Stop Bit
1	1	0	8 Bits + Even Parity + 1 Stop Bit
1	1	1	8 Bits + Odd Parity + 1 Stop Bit

Word length, Parity Select, and Stop Bit changes are not buffered and therefore become effective immediately.

Transmitter Control Bits (CR5 and CR6) — Two Transmitter Control bits provide for the control of the interrupt from the Transmit Data Register Empty condition, the Request-to-Send ($\overline{RTSi}$) output, and the transmission of a Break level (space). The following encoding format is used:

CR6	CR5	Function
0	0	$\overline{RTSi}$ = low, Transmitting Interrupt Disabled.
0	1	$\overline{RTSi}$ = low, Transmitting Interrupt Enabled.
1	0	$\overline{RTSi}$ = high, Transmitting Interrupt Disabled.
1	1	RTS = low, Transmits a Break level on the Transmit Data Output. Transmitting Interrupt Disabled.

Receive Interrupt Enable Bit (CR7) — The following interrupts will be enabled by a high level in bit position 7 of the Control Register (CR7). Receive Data Register Full Overrun.

9. STATUS REGISTER

Information on the status of the UARTi is available to the MPU by reading the UARTi Status Register. This read only register is selected when RS is low and R/$\overline{W}$ is high. Information stored in this register indicates the status of the Transmit Data Register, the Receive Data Register and error logic, and the peripheral/modem status inputs of the UARTi

Receive Data Register Full (RDRF), Bit 0 — Receive Data Register Full indicates that received data has been transferred to the Receive Data Register. RDRF is cleared after an MPU read of the Receive Data Register or by a master reset. The cleared or empty state indicates that the contents of the Receive Data Register are not current. Data Carrier Detect being high also causes RDRF to indicate empty.

Transmit Data Register Empty (TDRE), Bit 1 — The Transmit Data Register Empty bit being set high indicates that the Transmit Data Register contents have been transferred and that new data may be entered. The low state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

Clear-to-Send ($\overline{CTS}$), Bit 3 — The Clear-to-Send bit indicates the state of the Clear-to-Send input from a modem. A low $\overline{CTS}$ indicates that there is a Clear-to-Send from the modem. In the high state, the Transmit Data Register Empty bit is inhibited and the Clear-to-Send status bit will be high. Master reset does not affect the Clear-to-Send status bit.

Framing Error (FE), Bit 4 — Framing error indicates that the received character is improperly framed by a start and a stop bit and is detected by the absence of the first stop bit. This error indicates a synchronization error, faulty transmission, or a break condition. The framing error flag is set or reset during the receive data transfer time. Therefore, this error indicator is present throughout the time that the associated character is available.

Receiver Overrun (OVRN), Bit 5 — Overrun is an error flag the indicates that one or more characters in the data stream were lost. That is, a character or a number of characters were received but not read from the Receive Data Register (RDR) prior to subsequent characters being received. The overrun condition begins at the midpoint of the last bit of the second character received in succession without a read of the HDR having occurred. The Overrun does not occur in the Status Register until the valid character prior to Overrun has been read. The RDRF bit remains set until the Overrun is reset. Character synchronization is maintained during the Overrun condition. The Overrun indication is reset after the reading of data from the Receive Data Register or by a Master Reset.

Parity Error (PE), Bit 6 — The parity error flag indicates that the number of highs (ones) in the character does not agree with the preselected odd or even parity. Odd parity is defined to be when the total number of ones is odd. The parity error indication will be present as long as the data character is in the RDR. If no parity is selected, then both the transmitter parity generator output and the receiver parity check results are inhibited.

Interrupt Request ($\overline{IRQ}$), Bit 7 — The $\overline{IRQ}$ bit indicates the state of the $\overline{IRQ}$ output. Any interrupt condition with its applicable enable will be indicated in this status bit. Anytime the $\overline{IRQ}$ output is low the $\overline{IRQ}$ bit will be high to indicate the interrupt or service request status. $\overline{IRQ}$ is cleared by a read operation to the Receive Data Register or a write operation to the Transmit Data Register.