HB56A240 Series

2,097,152-Word x 40-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56A240B/SB is a 2M x 40 dynamic RAM module, mounted 20 pieces of 4 Mbit DRAM (HM514400AS) sealed in SOJ package. An outline of the HB56A240B/SB is a 72-pin single in-line package. Therefore, the HB56A240B/SB makes high density mounting possible without surface mount technology. The HB56A240B/SB provides common data inputs and outputs. Its module board has decoupling capacitors beneath the each SOJ but only on the one side of its module board.

■ FEATURES

- 72-pin Single In-line Package
  Lead Pitch 1.27mm
- Single 5V (±5%) Supply
- High Speed
  Access Time .....60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  Operation .....6038 mW/5513 mW/4988 mW/4463 mW (max)
  Standby .....210 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycles .....(16 ms)
- 2 Variations of Refresh
  $\overline{RAS}$ Only Refresh
  $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

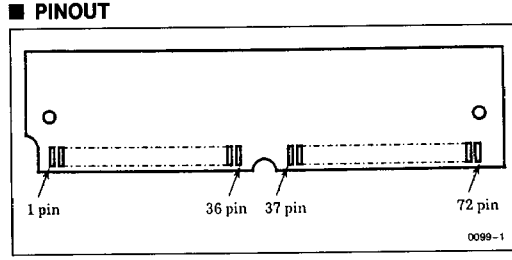
■ ORDERING INFORMATION

Part No.	Access Time	Package	Contact Pad
HB56A240B-6A	60 ns	72-pin SIP Socket Type	Gold
HB56A240B-7A	70 ns		
HB56A240B-8A	80 ns		
HB56A240B-10A	100 ns		
HB56A240SB-6A	60 ns	72-pin SIP Socket Type	Solder
HB56A240SB-7A	70 ns		
HB56A240SB-8A	80 ns		
HB56A240SB-10A	100 ns		

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_8	Refresh Address Input
DQ_0–DQ_{39}	Data-in/Data-out
$\overline{CAS0}$, $\overline{CAS1}$	Column Address Strobe
$\overline{RAS0}$, $\overline{RAS0}$	Row Address Strobe
$\overline{WE}$	Read/Write Enable
$\overline{OE}$	Output Enable
V_{DD}	Power Supply (+ 5V)
V_{SS}	Ground
PD1–PD4	Presence Detect Pin
NC	No Connection

■ PINOUT

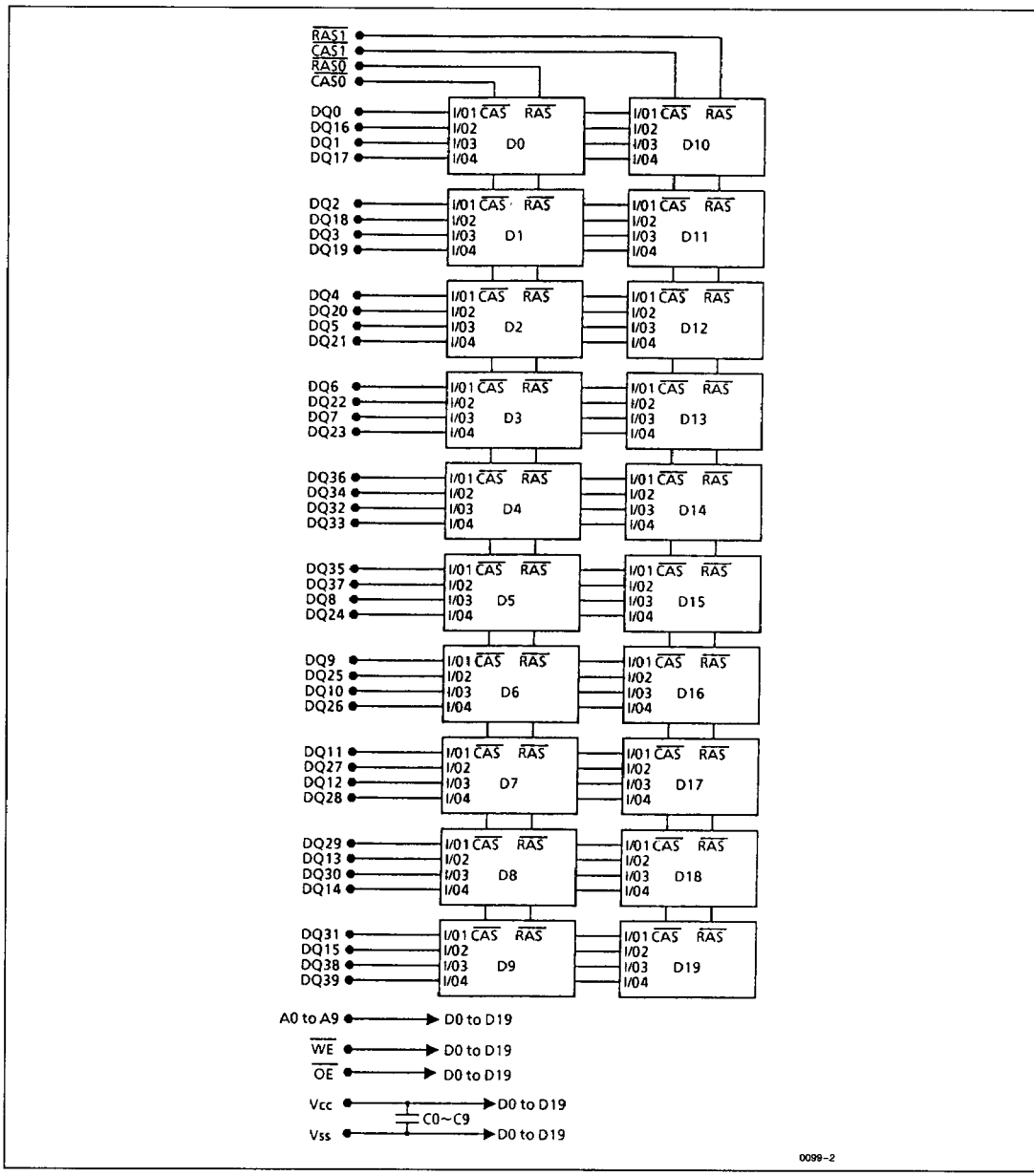


Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	$\overline{OE}$	37	DQ_{33}	55	DQ_{11}
2	DQ_0	20	DQ_4	38	DQ_{35}	56	DQ_{27}
3	DQ_{16}	21	DQ_{20}	39	V_{SS}	57	DQ_{12}
4	DQ_1	22	DQ_5	40	NC	58	DQ_{28}
5	DQ_{17}	23	DQ_{21}	41	$\overline{CAS0}$	59	V_{DD}
6	DQ_2	24	DQ_6	42	$\overline{CAS1}$	60	DQ_{29}
7	DQ_{18}	25	DQ_{22}	43	NC	61	DQ_{13}
8	DQ_3	26	DQ_7	44	$\overline{RAS0}$	62	DQ_{30}
9	DQ_{19}	27	DQ_{23}	45	$\overline{RAS1}$	63	DQ_{14}
10	V_{DD}	28	A_7	46	DQ_{37}	64	DQ_{31}
11	NC	29	DQ_{36}	47	$\overline{WE}$	65	DQ_{15}
12	A_0	30	V_{DD}	48	GND	66	DQ_{38}
13	A_1	31	A_8	49	DQ_8	67	PD1
14	A_2	32	A_9	50	DQ_{24}	68	PD2
15	A_3	33	NC	51	DQ_9	69	PD3
16	A_4	34	NC	52	DQ_{25}	70	PD4
17	A_5	35	DQ_{34}	53	DQ_{10}	71	DQ_{39}
18	A_6	36	DS_{36}	54	DQ_{26}	72	V_{SS}

■ PRESENCE DETECT PINOUT

Pin No.	Pin Name	HB56A240B/SB			
		-6A	-7A	-8A	-10A
67	PD1	NC	NC	NC	NC
68	PD2	NC	NC	NC	NC
69	PD3	NC	V_{SS}	NC	V_{SS}
70	PD4	NC	NC	V_{SS}	V_{SS}

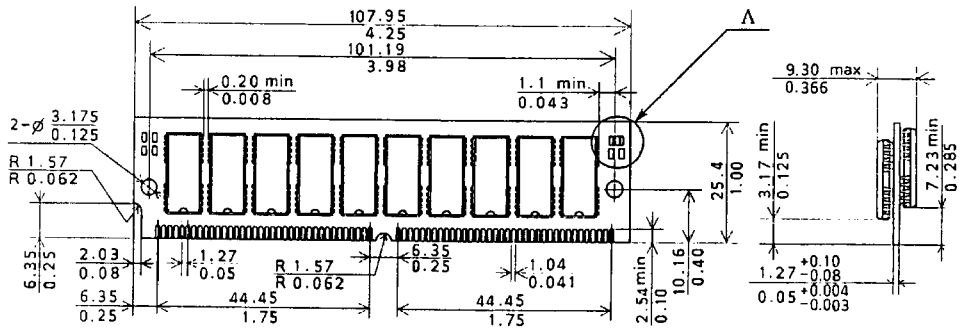
■ BLOCK DIAGRAM



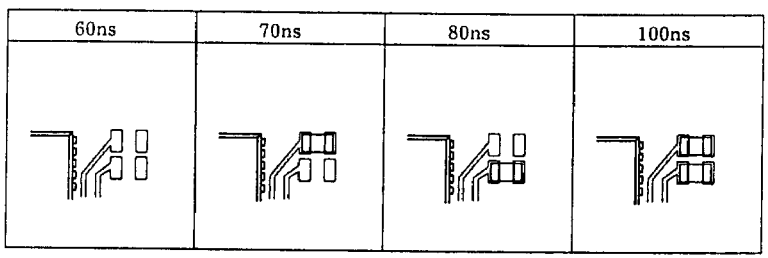
* D0 to D9: HM514400AS

■ PHYSICAL OUTLINE

Unit: mm / inch



Detail A



Note: Following the specification of the contact pad.

Part No.	Contact Pad
HB56A240B-XXA	Gold
HB56A240SB-XXA	Solder

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	10	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	− 1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)

Parameter	Symbol	HB56A240B/SB								Unit	Test Conditions	Note
		-6A		-7A		-8A		-10A				
		Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	1150	—	1050	—	950	—	850	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	40	—	40	—	40	—	40	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	20	—	20	—	20	—	20	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	1150	—	1050	—	950	—	850	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	100	—	100	—	100	—	100	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	1150	—	1050	—	950	—	850	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	1150	—	1050	—	950	—	850	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	V	I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±5%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address A_0-A_9)	C_{I1}	—	140	pF	1
Input Capacitance ($\overline{WE}$, $\overline{OE}$)	C_{I2}	—	160	pF	1
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$)	C_{I4}	—	90	pF	1
Input/Output Capacitance (DQ_0 to DQ_{39})	$C_{I/O1}$	—	25	pF	1

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)[1, 14, 15, 16]

Read, Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HB56A240B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	150	—	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	100000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10000	20	10000	20	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	20	60	25	75	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	15	40	20	55	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	20	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	15	—	20	—	20	—	25	—	ns	
$\overline{OE}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	0	—	0	—	ns	
$\overline{CAS}$ Setup Time from D_{in}	t_{DZC}	0	—	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	
Refresh Period	t_{REF}	—	16	—	16	—	16	—	16	ms	

• **Read Cycle**

Parameter	Symbol	HB56A240B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	2, 3, 17
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	20	—	20	—	25	ns	3, 4, 13
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	ns	3, 4, 13, 16
Access Time from $\overline{OE}$	t_{OAC}	—	15	—	20	—	20	—	25	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	0	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	45	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	0	15	0	20	0	20	0	20	ns	6
Output Buffer Turn-off Time to $\overline{OE}$	t_{OFF2}	0	15	0	20	0	20	0	20	ns	6
$\overline{CAS}$ to D_{in} Delay Time	t_{CDD}	15	—	20	—	20	—	25	—	ns	

• Write Cycle

Parameter	Symbol	HB56A240B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	10	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	20	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	20	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	15	—	20	—	ns	11

• Read-Modify-Write Cycle

Parameter	Symbol	HB56A240B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Read-Write Cycle Time	t_{RWC}	150	—	180	—	200	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	80	—	95	—	105	—	135	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	35	—	45	—	45	—	60	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	50	—	60	—	65	—	80	—	ns	10
$\overline{OE}$ Hold Time from $\overline{WE}$	t_{OEH}	15	—	20	—	20	—	25	—	ns	

• Refresh Cycle

Parameter	Symbol	HB56A240B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	ns	

• Fast Page Mode Cycle

Parameter	Symbol	HB56A240B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	40	—	45	—	50	—	55	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	ns	12
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	35	—	40	—	45	—	50	ns	13, 17
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	—	40	—	45	—	50	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	80	—	95	—	100	—	110	—	ns	

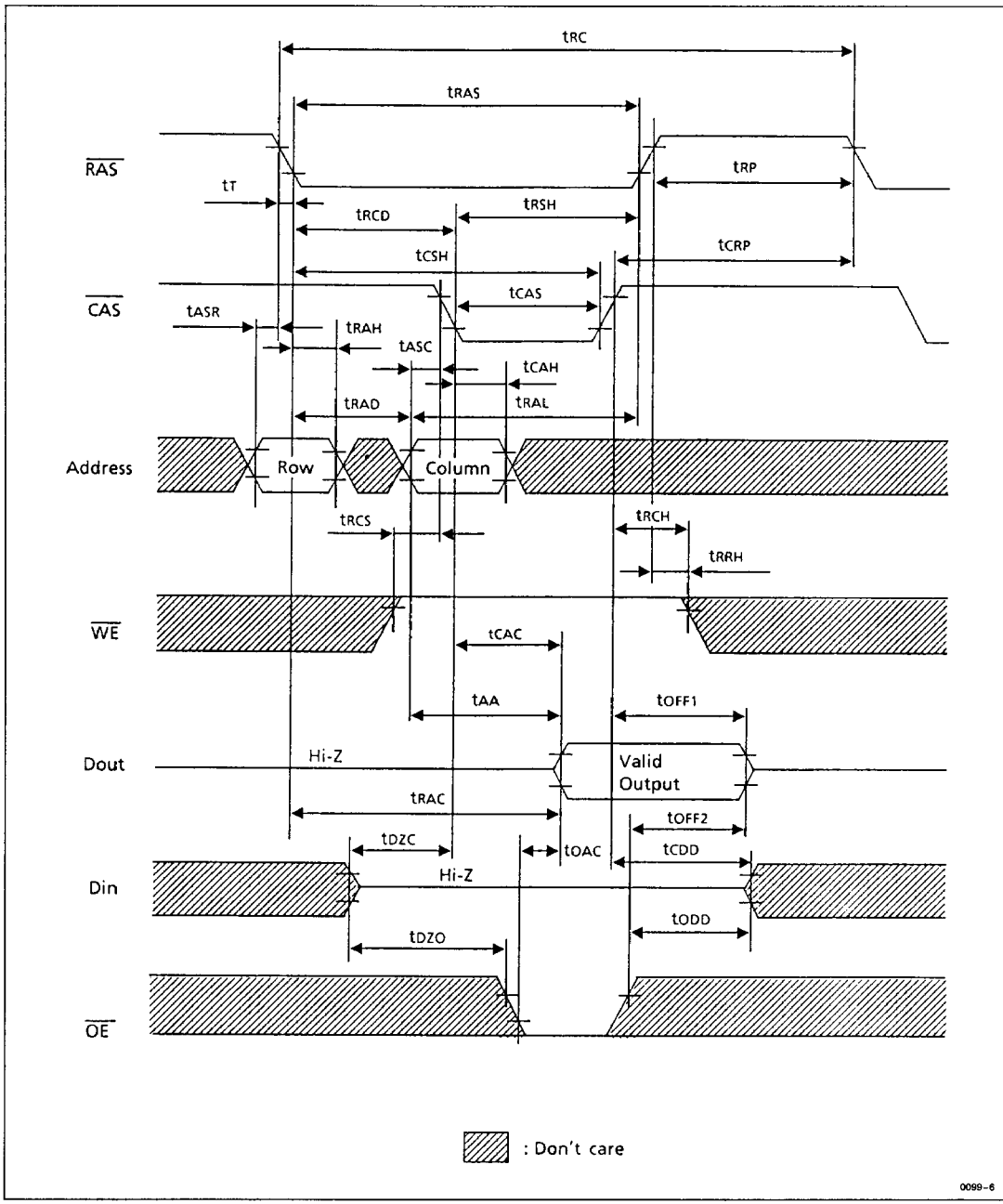
• Test Mode Cycle

Parameter	Symbol	HB56A240B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Test Mode $\overline{WE}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WH}	10	—	10	—	10	—	10	—	ns	

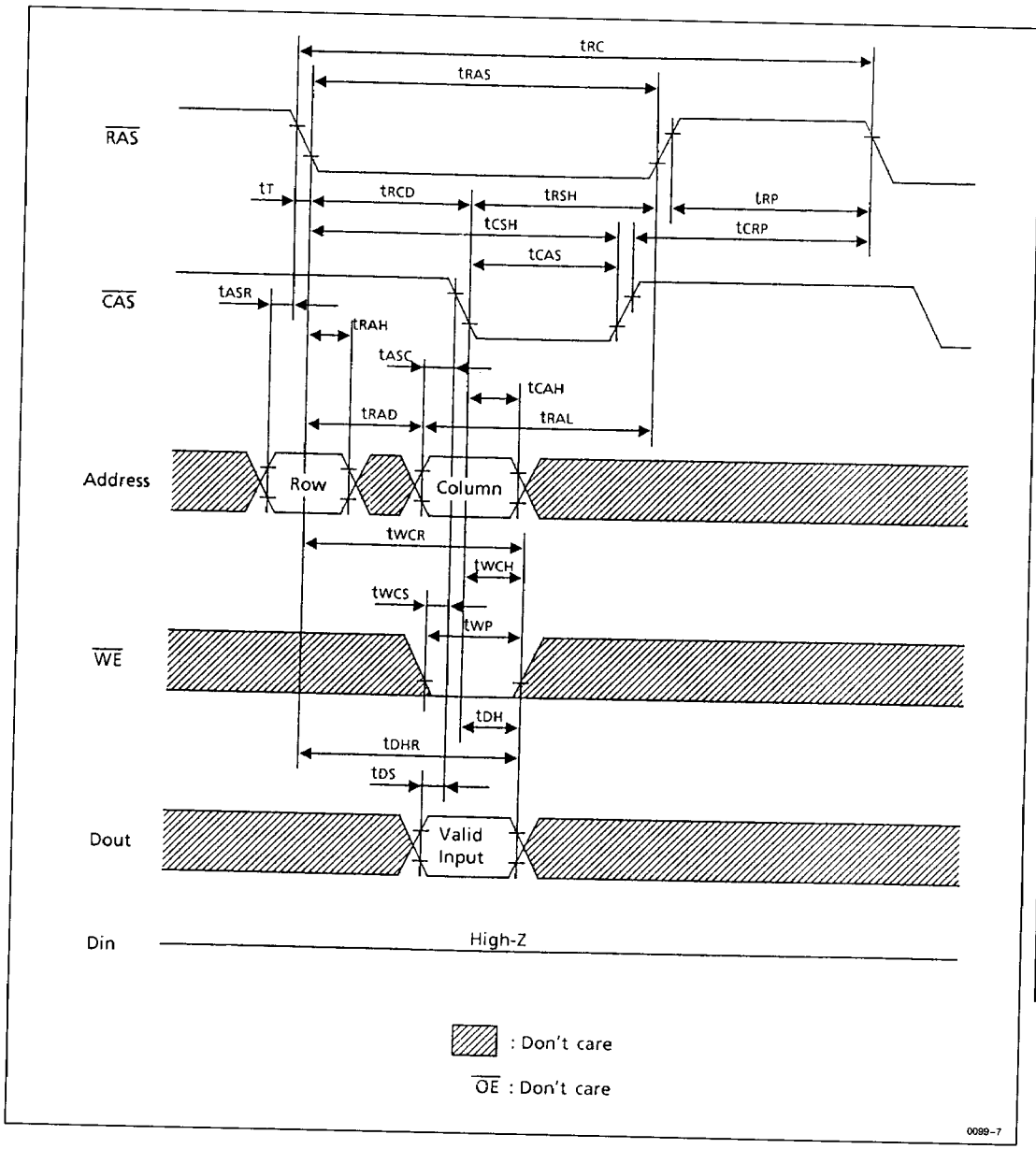
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL load and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of condition is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading in an early write cycle and to WE leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycle.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pulse of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycle is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits ... CA0. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is low level. Data output pin is I/O_3 and data input pin is I/O_2. In order to end this test mode operation, perform a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
17. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{OAC} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

■ TIMING WAVEFORMS

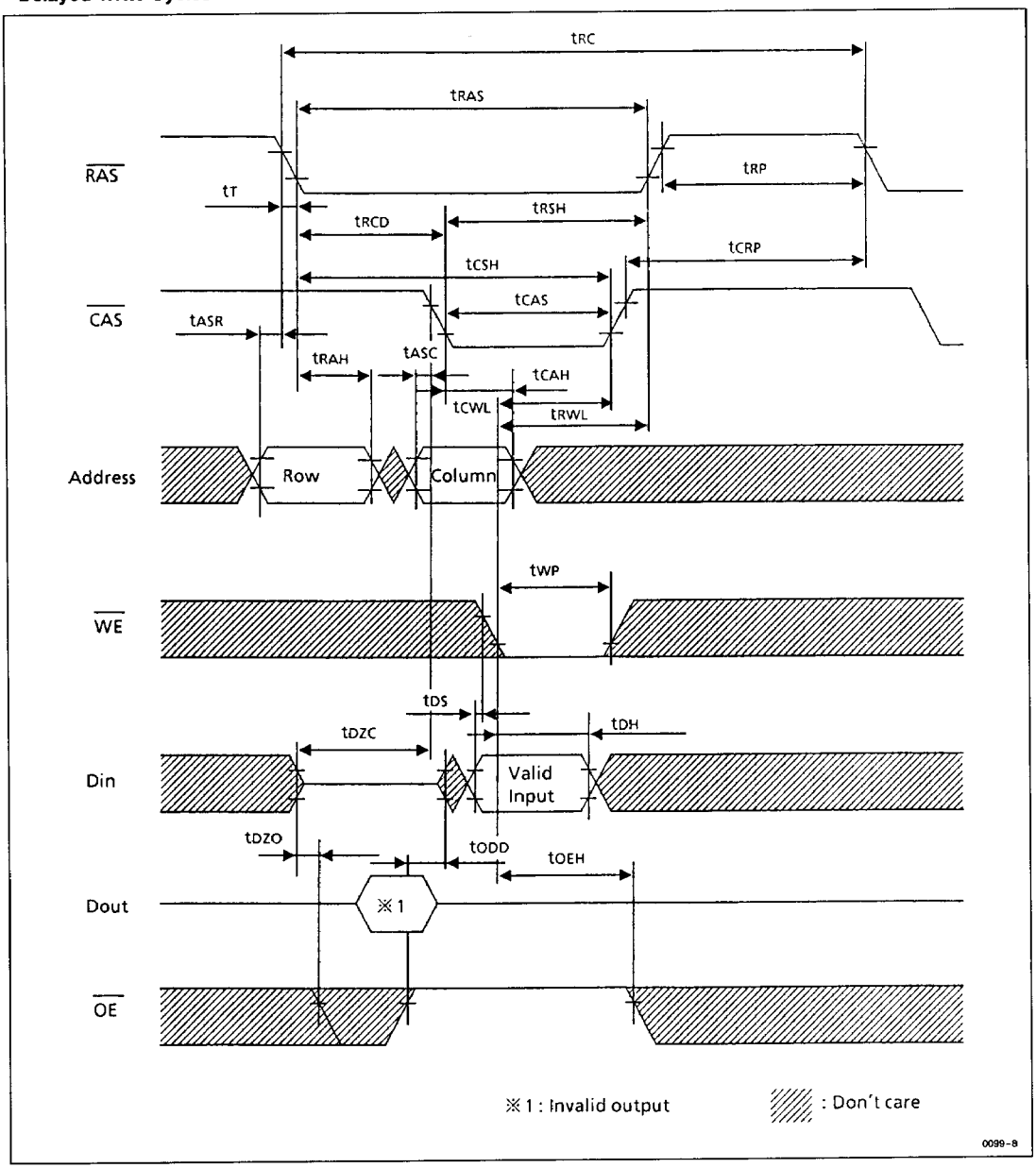
• Read Cycle



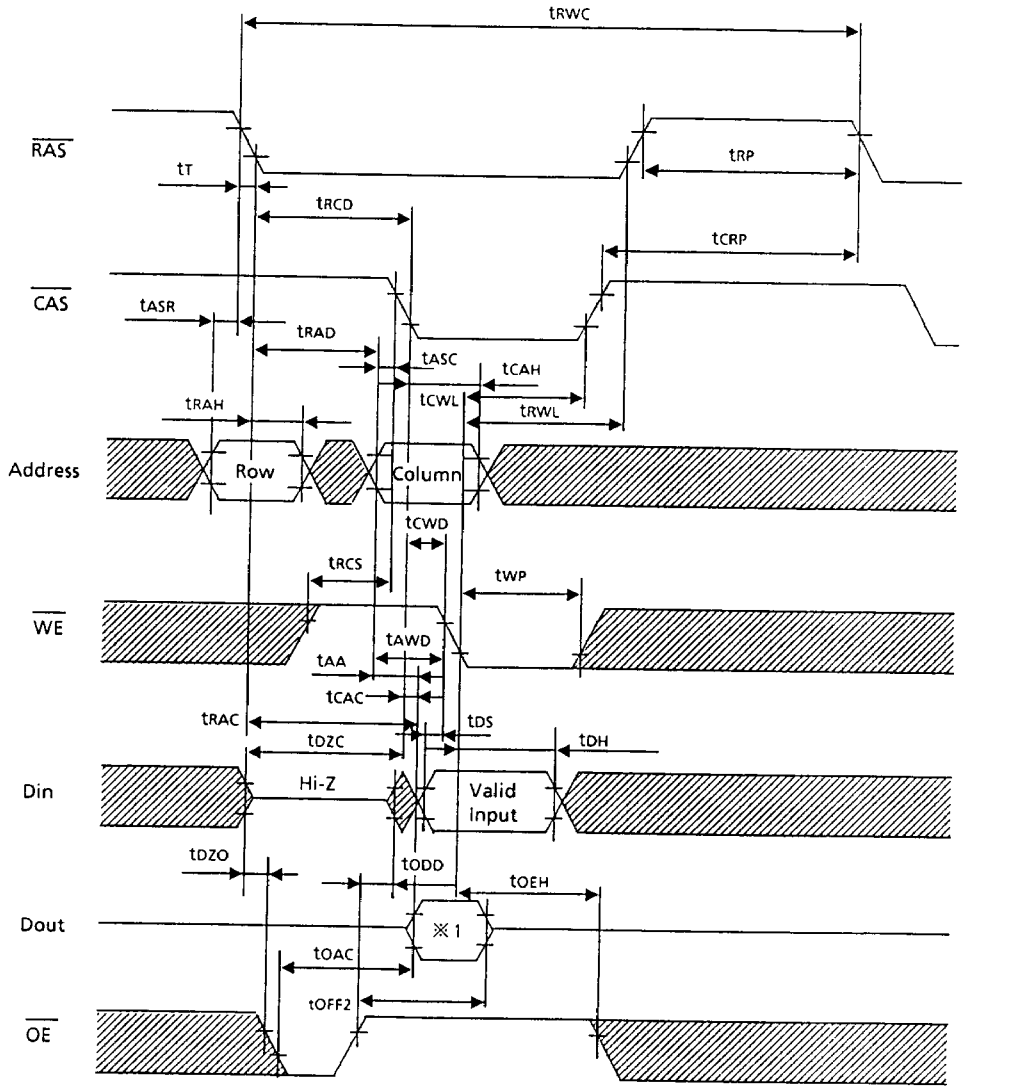
• **Early Write Cycle**



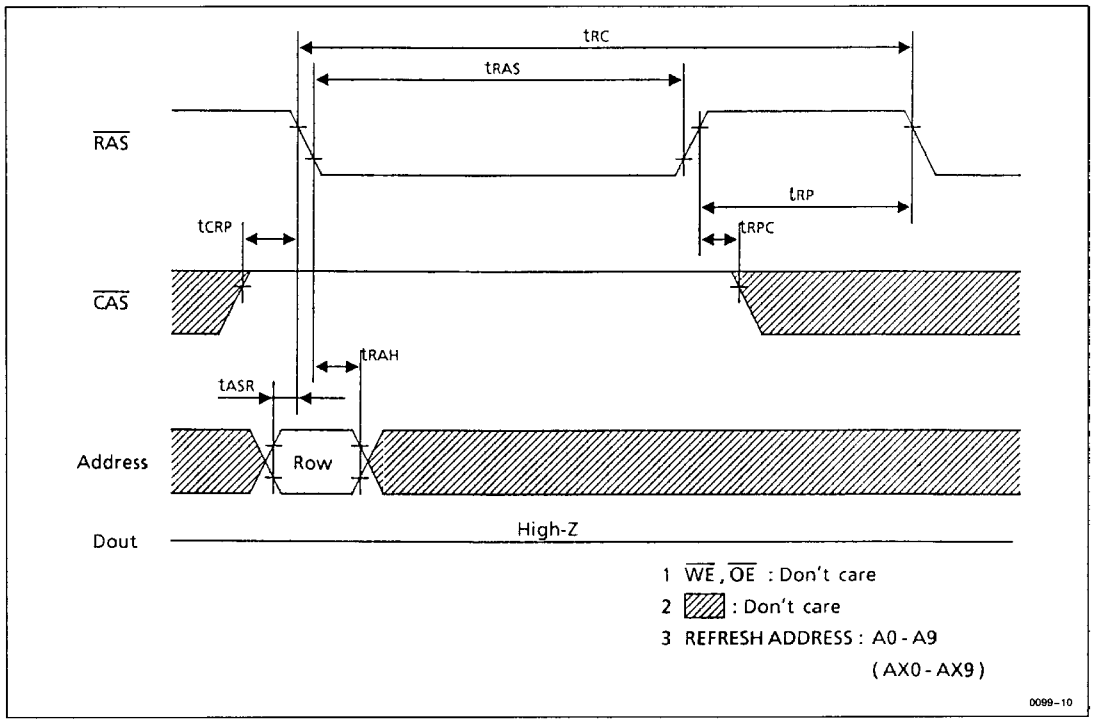
• **Delayed Write Cycles**



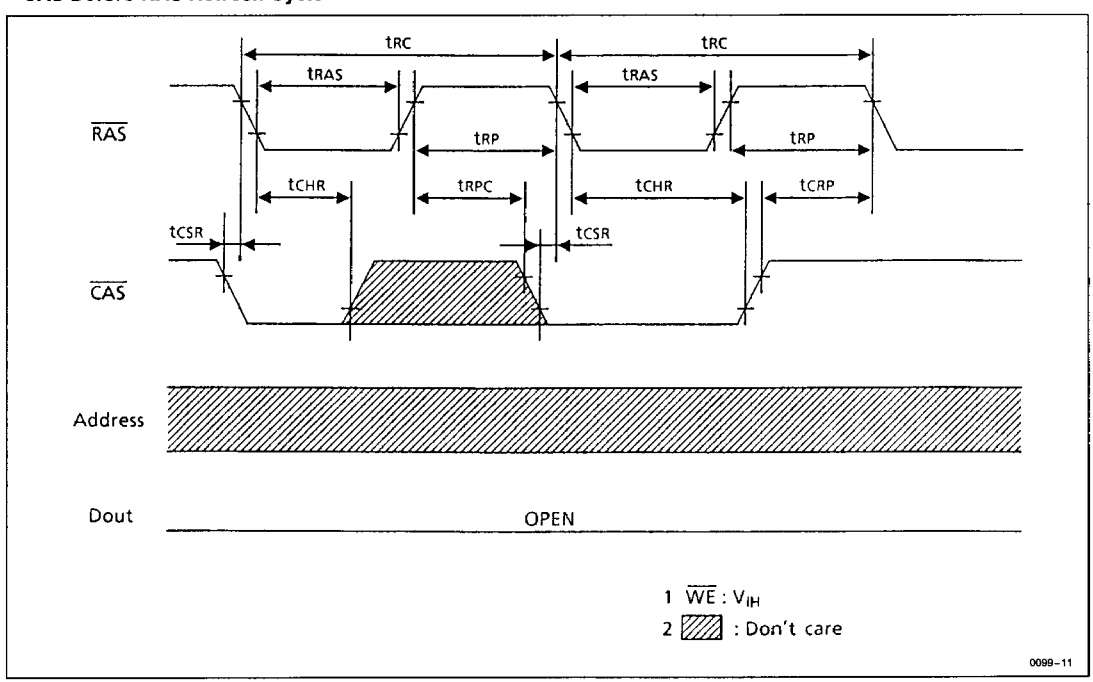
• **Read-Modify-Write Cycle**



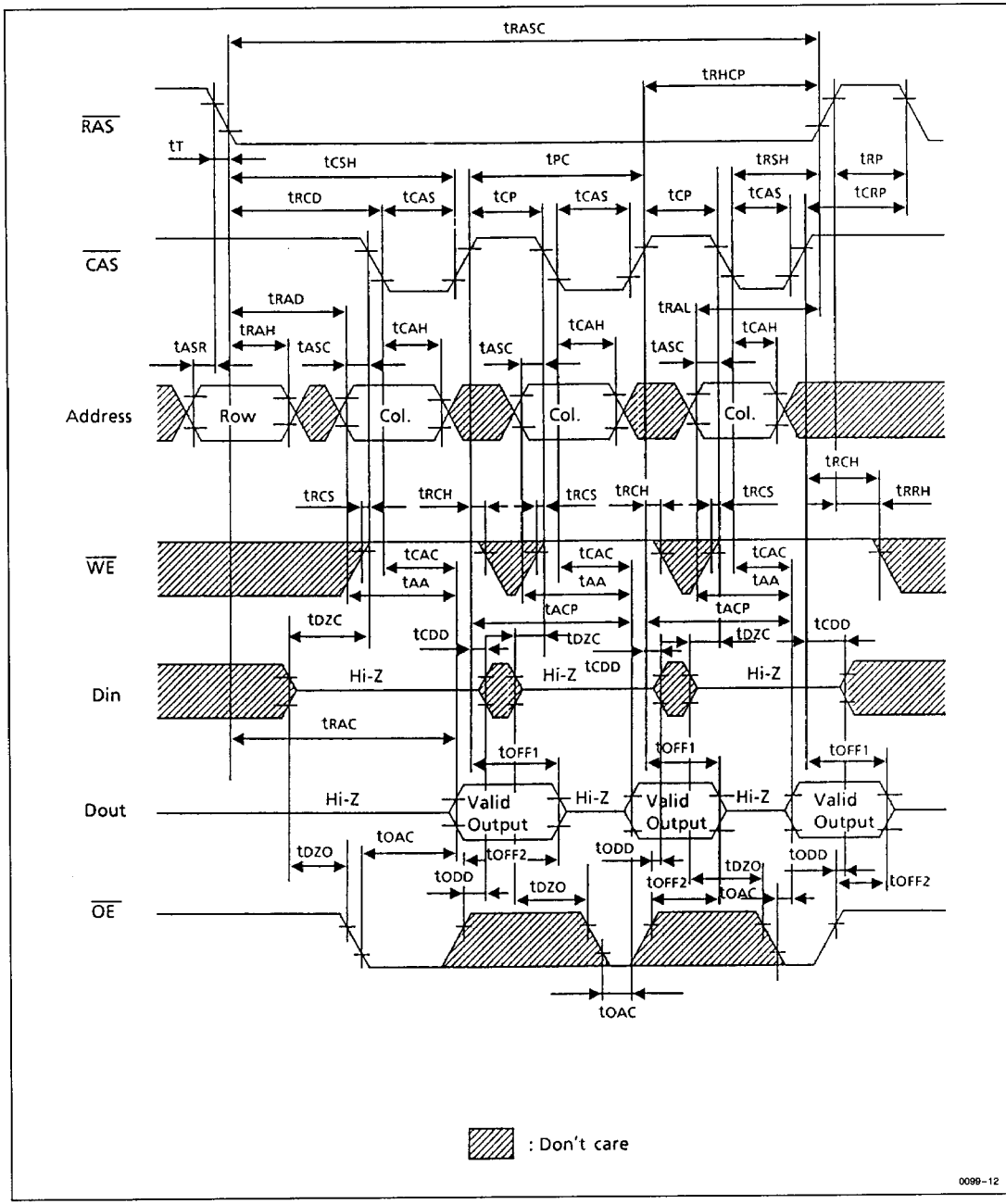
• $\overline{RAS}$ Only Refresh Cycle



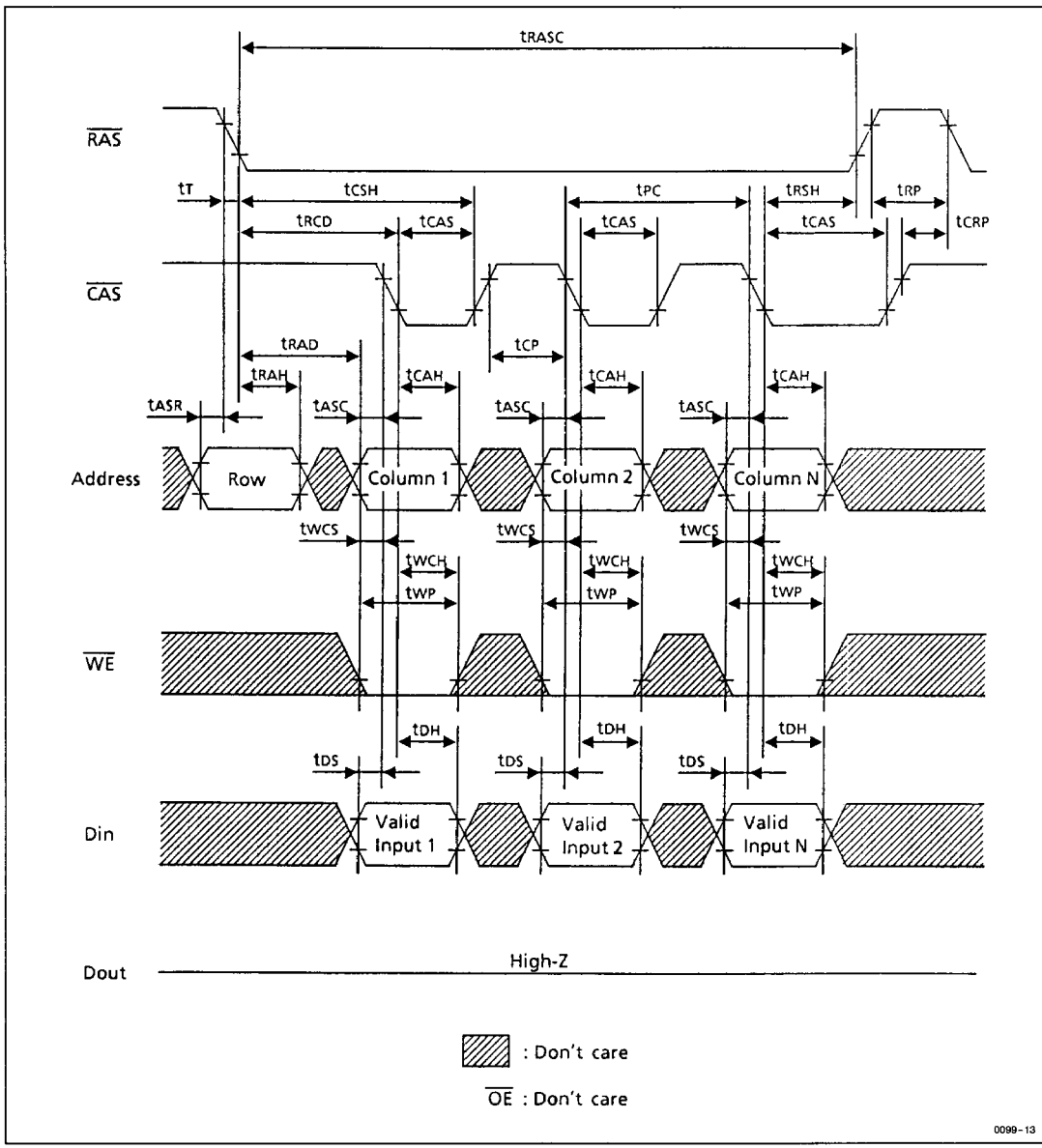
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



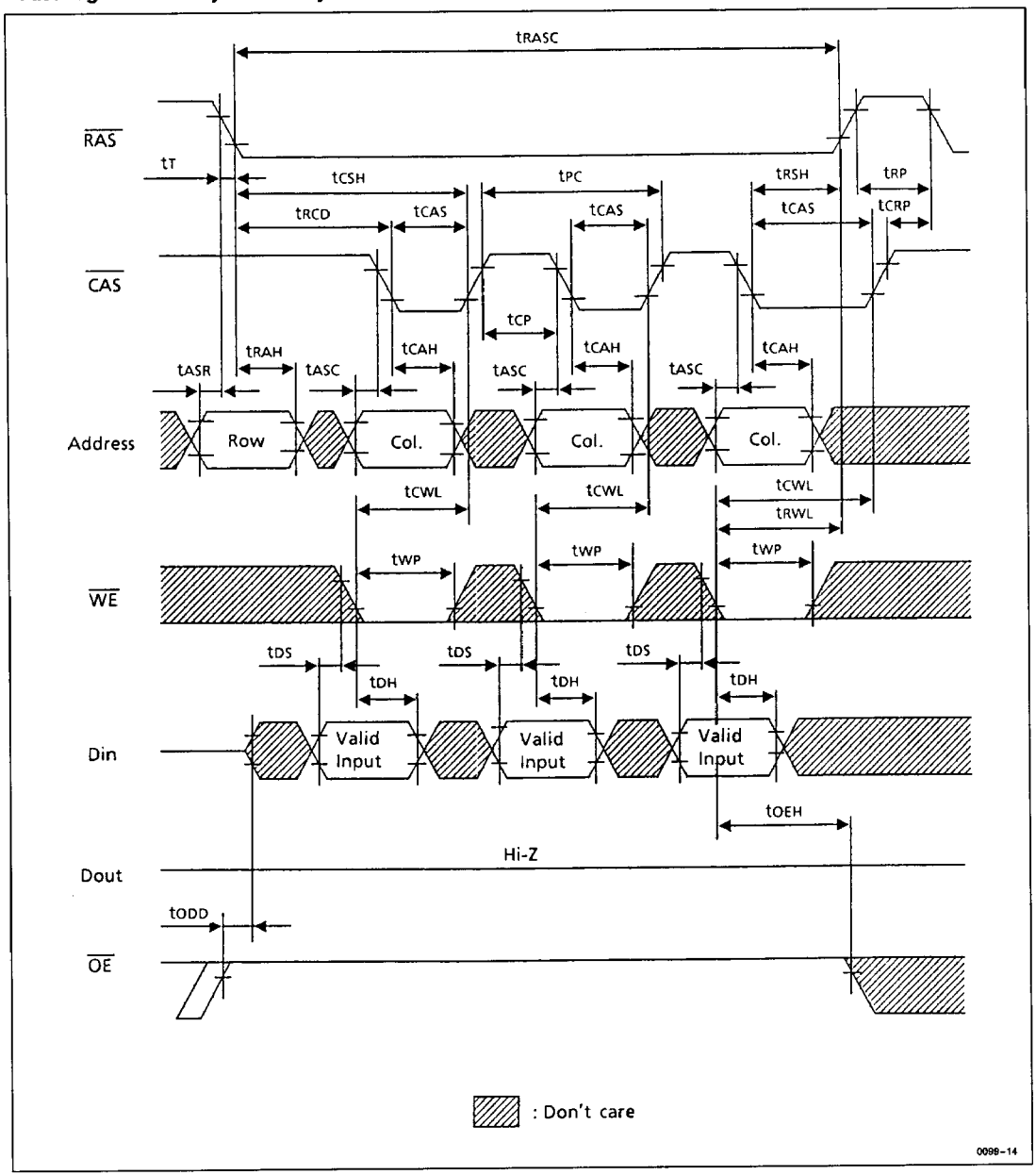
• **Fast Page Mode Read Cycle**



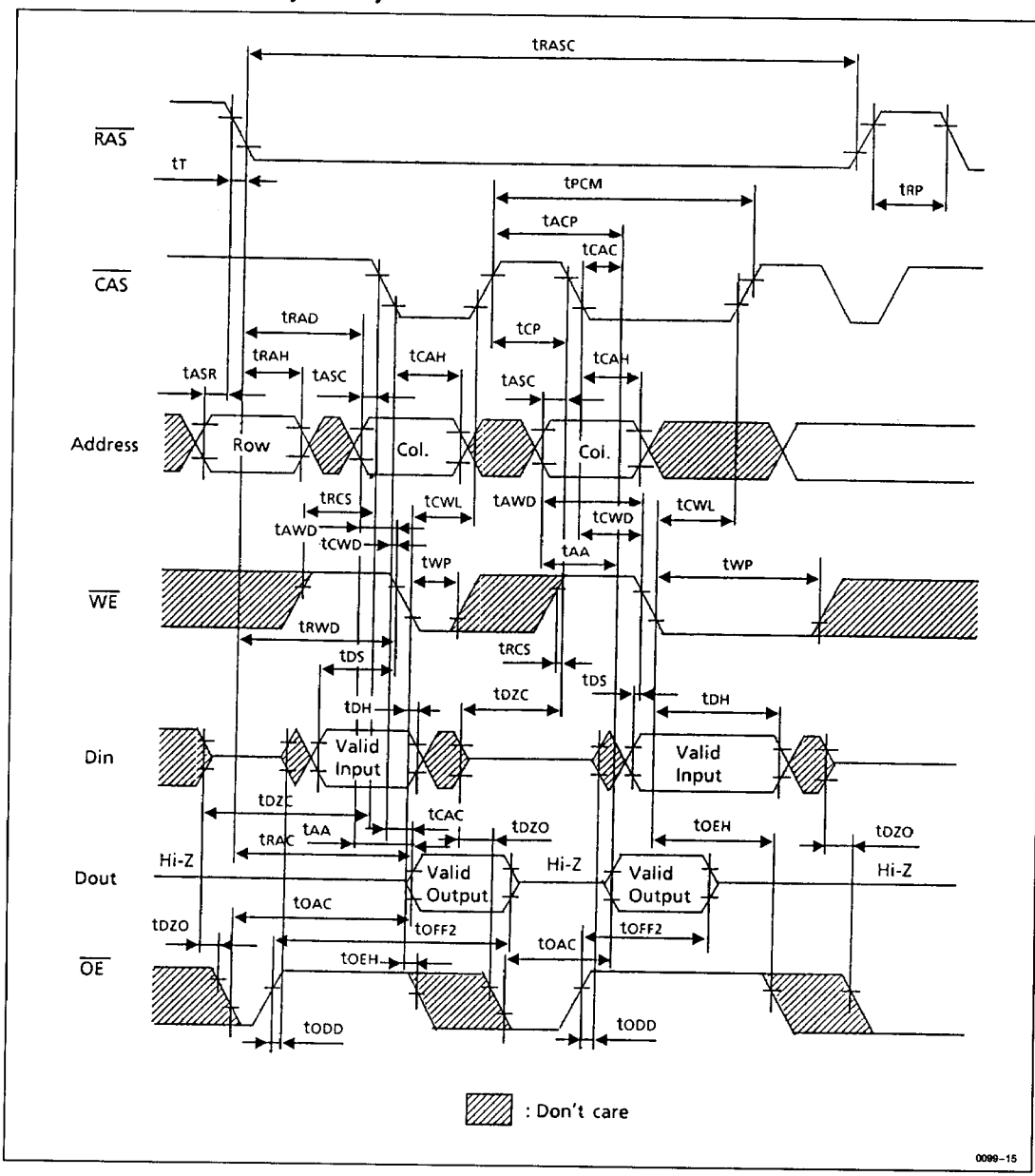
• **Fast Page Mode Early Write Cycle**



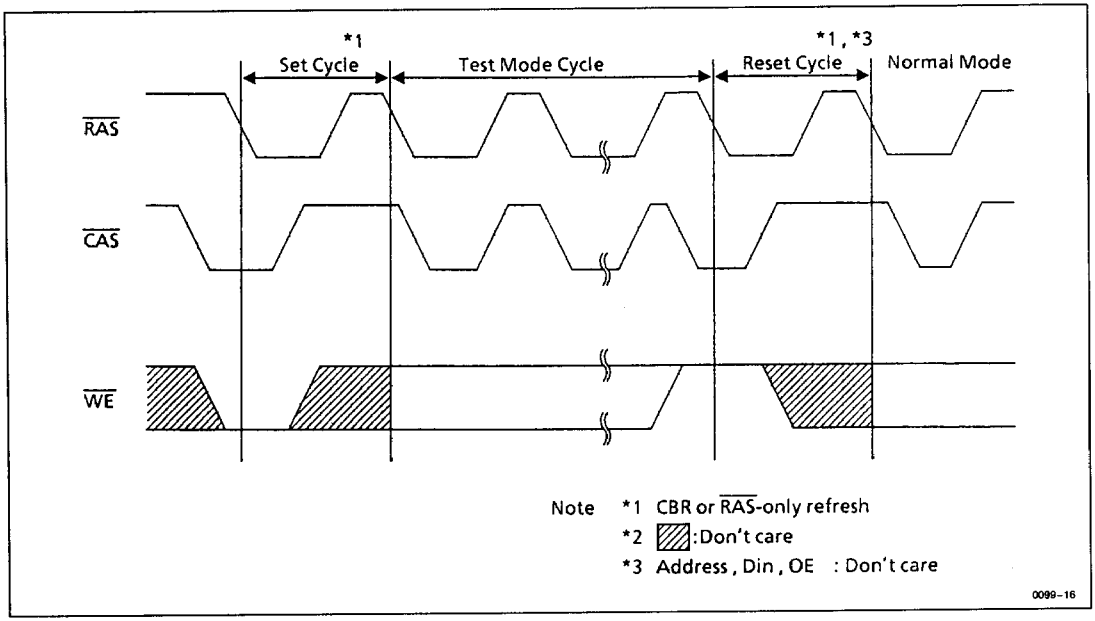
• **Fast Page Mode Delayed Write Cycle**



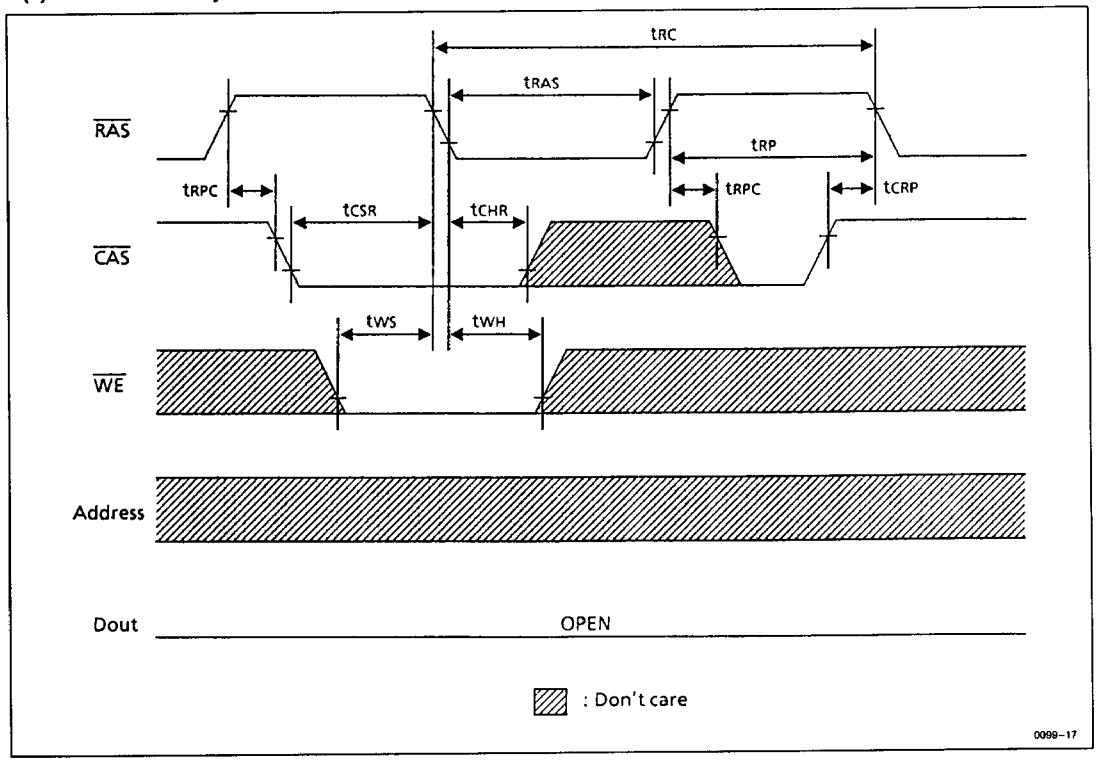
• **Fast Page Mode Read-Modify-Write Cycle**



• **TEST MODE CYCLE**

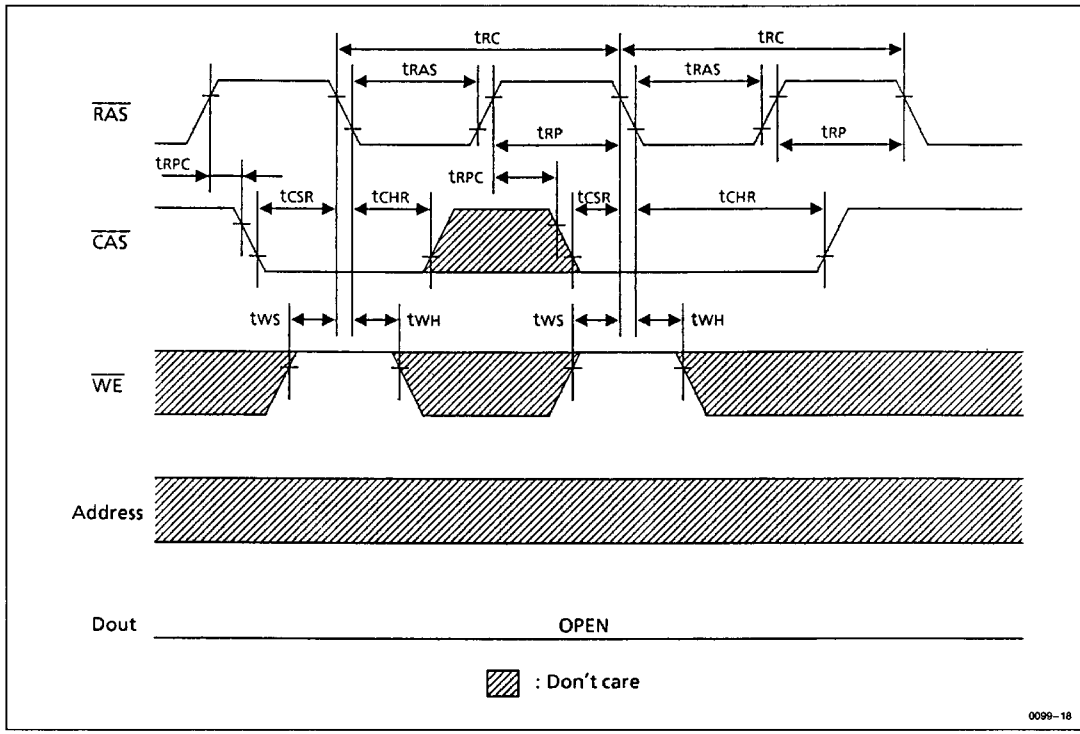


• **(1) Test Mode Set Cycle**

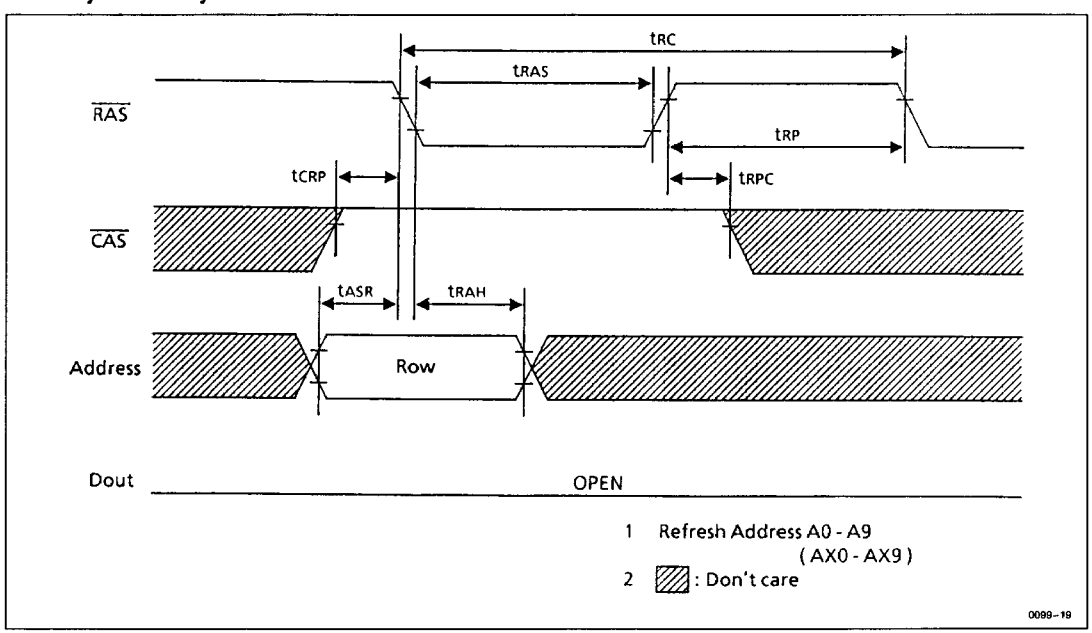


• (2) Test Mode Reset Cycle

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



$\overline{RAS}$ Only Refresh Cycle



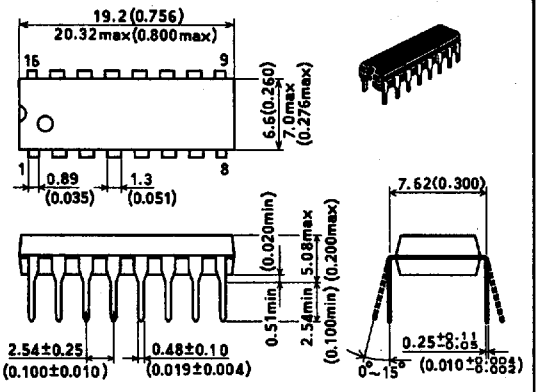
PACKAGE INFORMATION

T-90-20

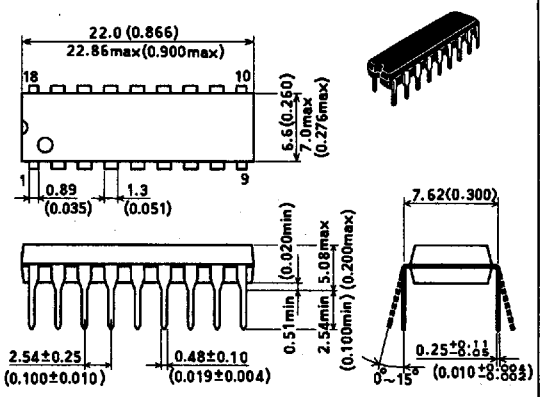
• Dual-in-line Plastic

Unit: mm (inch) Scale 3/2

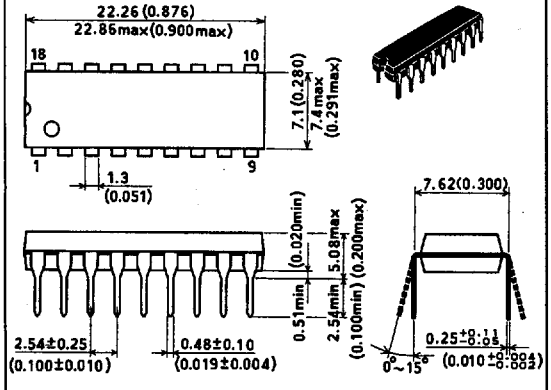
• DP-16B



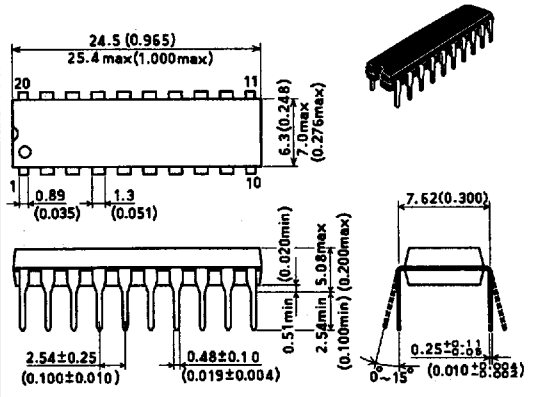
• DP-18B



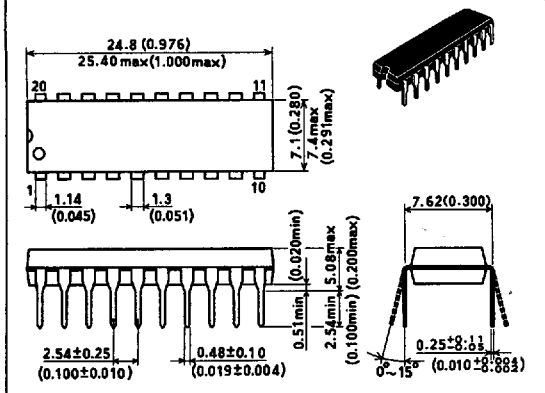
• DP-18C



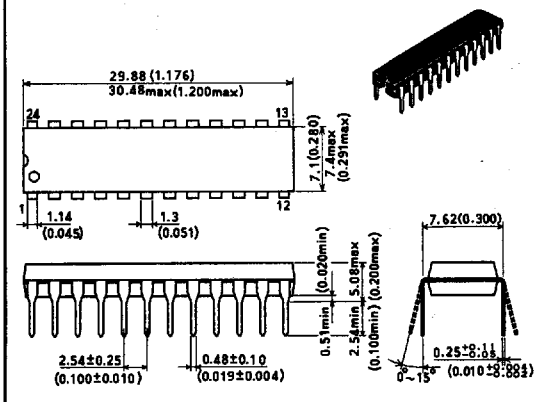
• DP-20N



• DP-20NA



• DP-20NC

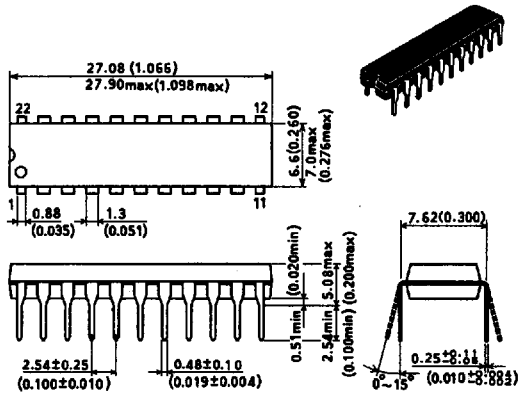


• Dual-in-line Plastic

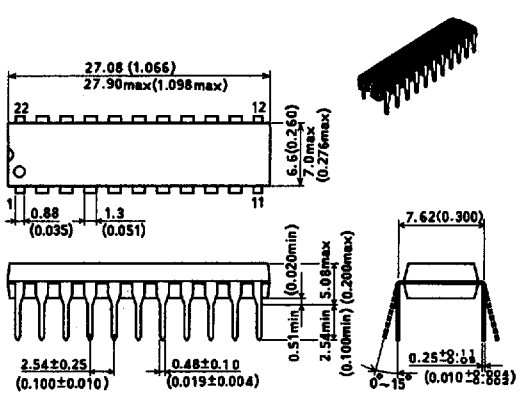
Unit: mm (inch) Scale 3/2

T-90-20

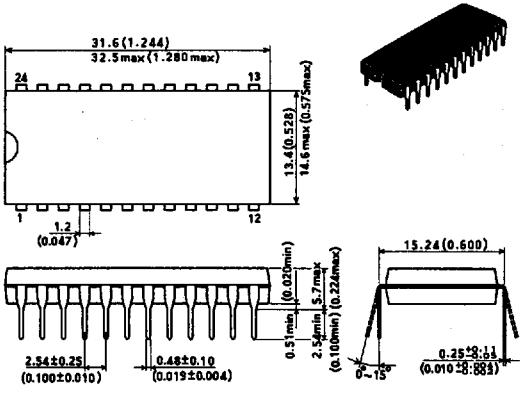
• DP-22N



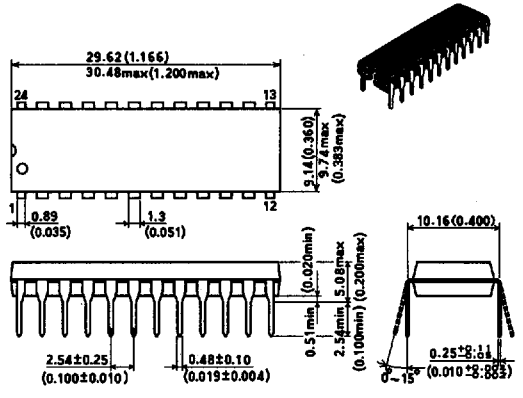
• DP-22NB



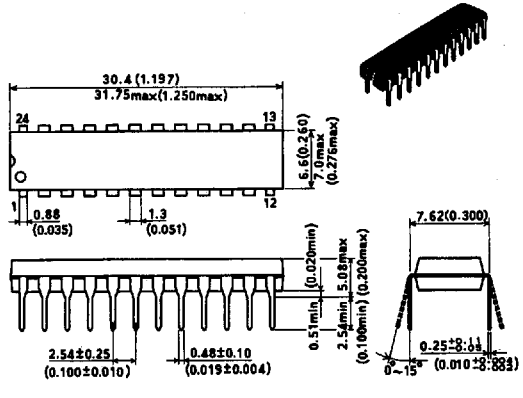
• DP-24



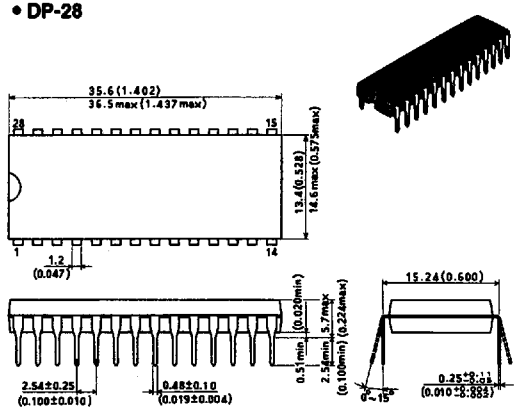
• DP-24A



• DP-24N



• DP-28



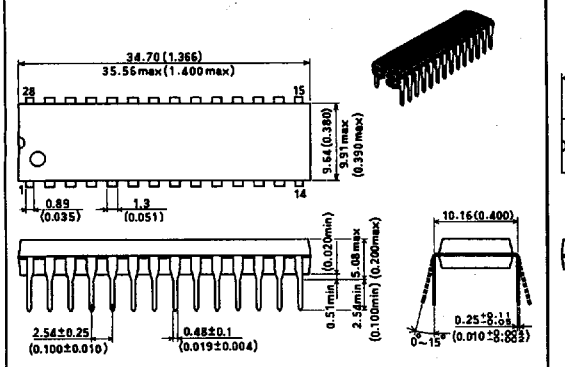
• Dual-in-line Plastic

HITACHI/ LOGIC/ARRAYS/MEM

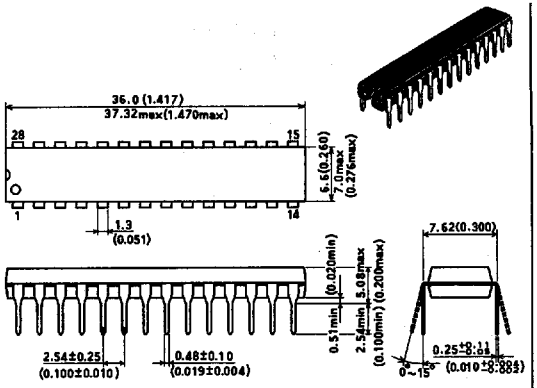
Unit: mm (inch) Scale 3/2

T-90-20

• DP-28C



• DP-28N

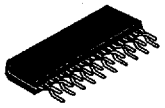


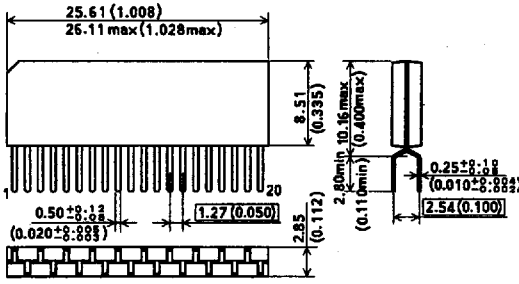
• Zigzag-in-line Plastic HITACHI/ LOGIC/ARRAYS/MEM

Unit: mm (inch) Scale 3/2

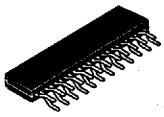
T-90-20

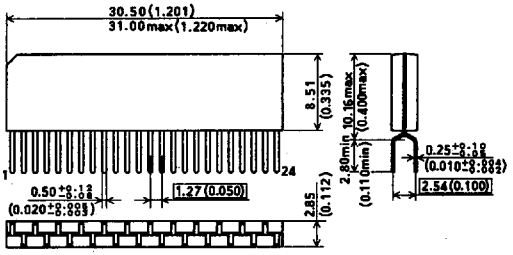
• ZP-20



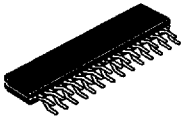


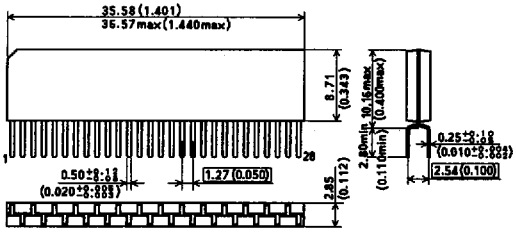
• ZP-24



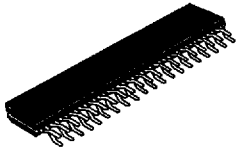


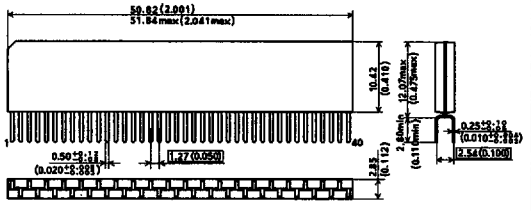
• ZP-28





• ZP-40





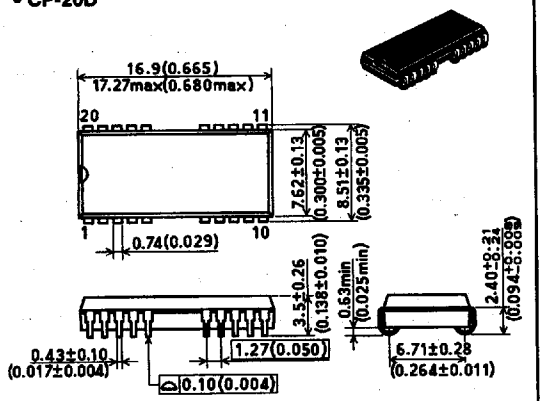
• Flat Package (J-bend Leads)

HITACHI/ LOGIC/ARRAYS/MEM

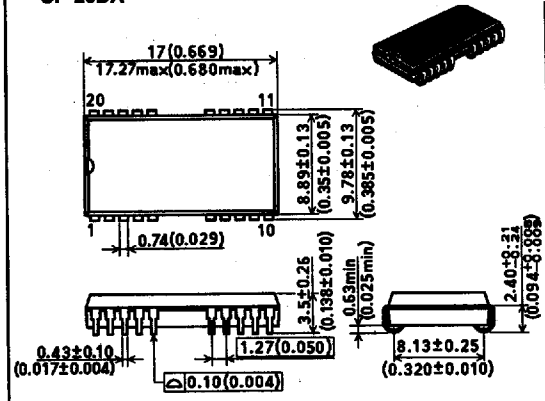
Unit: mm (inch) Scale 3/2

T-90-20

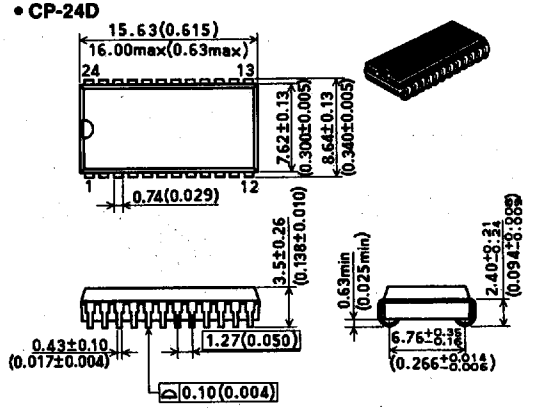
• CP-20D



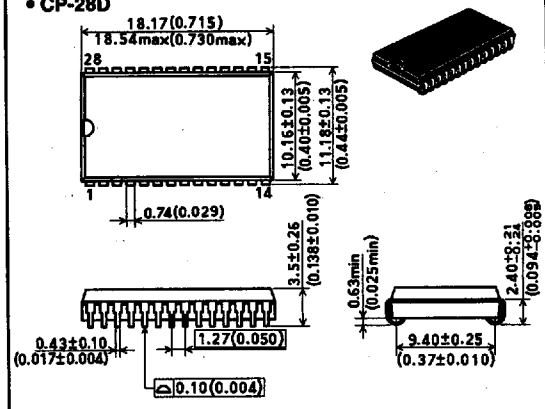
• CP-20DA



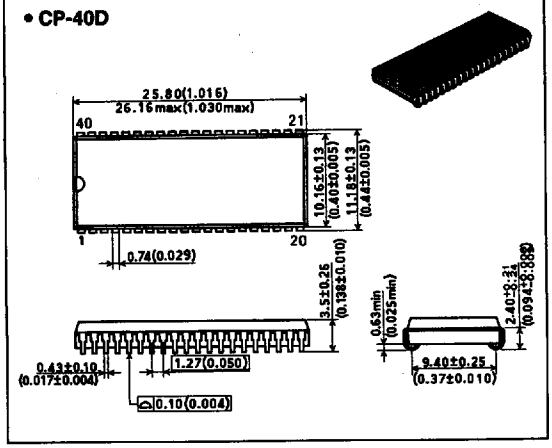
• CP-24D



• CP-28D



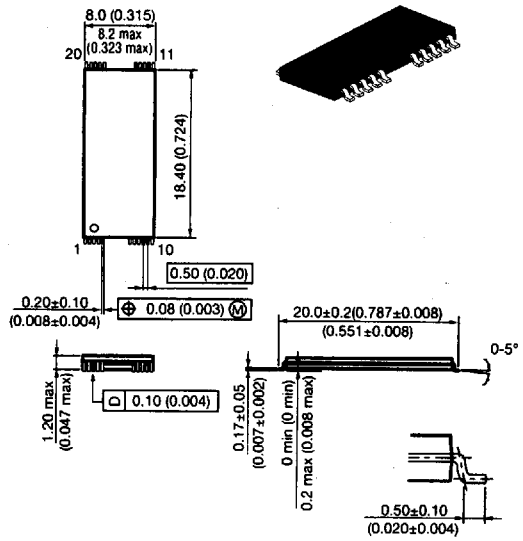
• CP-40D



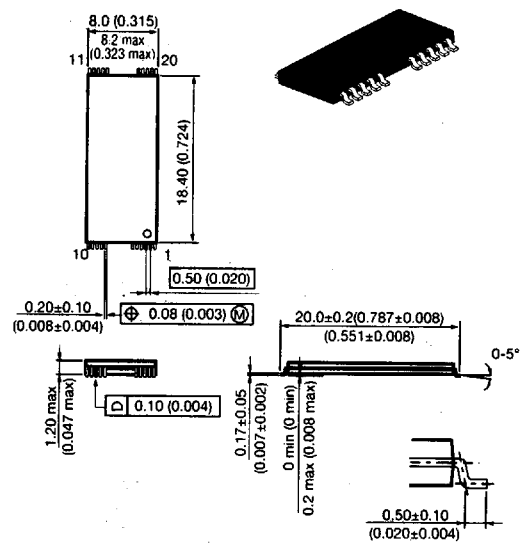
• TSOP (Thin Small Outline Package)

Unit: mm (inch) Scale 3/2

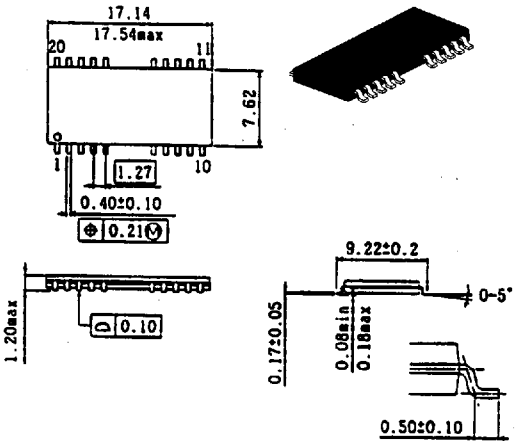
• TFP-20DA



• TFP-20DAR



• TTP-20D



• TTP-20DR