REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Made technical changes to Table I. Figure 4 added. Editorial changes throughout. mlp	92-01-27	Monica L. Poelking
B	Changes in accordance with NOR 5962-R107-93. tvn	93-04-01	Monica L. Poelking
C	Add package CDFP4-F16. Use new boilerplate. ljs	98-02-04	Raymond Monnin
D	V_{EE} changed to -3.2 V for AC tests in Table I. Figure 4 modified to be consistent with Table I. ljs	98-09-15	Raymond Monnin
E	Update to current requirements. Editorial changes throughout. gap	06-03-06	Raymond Monnin
F	Update drawing to current MIL-PRF-38535 requirements. - jt	13-06-24	C. SAFFLE

The original first page of this drawing has been replaced.

REV																				
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SHEET																				

REV STATUS	REV	F	F	F	F	F	F	F	F	F	F	F	F		
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

PREPARED BY
David W. Queenan

CHECKED BY
D. A. DiCenzo

APPROVED BY
Robert P. Evans

DRAWING APPROVAL DATE
88-01-29

REVISION LEVEL
F

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

MICROCIRCUIT, DIGITAL, ECL-TO-TTL TRANSLATOR, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-87508**

SHEET 1 OF 12

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-87508	01	E	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	10H525	Quad TTL-to-ECL translator

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual -in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat package
X	CDFP4-F16	16	Flat-package
2	CQCC1-N20	20	Square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range (V_{EE}) ..... -8.0 V dc to 0.0 V dc
Input voltage range ..... 0.0 V dc to -5.46 V dc
Storage temperature range ..... -65°C to +165°C
Lead temperature (soldering, 10 seconds) ..... +300°C
Junction temperature (T_J) ..... +165°C
Maximum power dissipation (P_D) ..... 255 mW
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage range (V_{EE}) ..... -5.46 V dc minimum to -4.94 V dc maximum
Case operating temperature range(T_C) ..... -55°C to +125°C
Minimum high level input voltage (V_{IH}):
T_A = +25°C ..... -0.780 V dc
T_A = +125°C ..... -0.650 V dc
T_A = -55°C ..... -0.840 V dc
Maximum low level input voltage (V_{IL})..... -1.950 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Logic diagrams. The logic diagrams shall be as specified on figure 3.

3.2.5 Test circuit and switching waveforms. Test circuit and switching waveforms shall be as specified on figure 4

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, 8A and 8B in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 shall include verification of the truth table specified on figure 2 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified			Group A subgroups	Limits		Unit
						Min	Max	
Cases E, F, 2 and X		Quiescent tests 1/						
			V_{IH}	V_{IL}				
High level output voltage	V_{OH}	V_{EE} = -5.2 V, 2/ V_{CC} = +5.0 V, Load = -2 mA	-0.780	-1.950	1	2.500		V
			-0.650	-1.950	2	2.500		
			-0.840	-1.950	3	2.500		
Low level output voltage	V_{OL}	GND = 0.0 V	-0.780	-1.950	1		0.500	V
			-0.650	-1.950	2		0.500	
			-0.840	-1.950	3		0.500	
High level threshold output voltage	V_{OHA}		-1.110	-1.480	1	2.500		V
			-0.960	-1.465	2	2.500		
			-1.160	-1.510	3	2.500		
Low level threshold output voltage	V_{OLA}		-1.110	-1.480	1		0.500	V
			-0.960	-1.465	2		0.500	
			-1.160	-1.510	3		0.500	
Power supply drain current	I_{EE} 4/	GND = 0.0 V, V_{CC} = +5.0 V, V_{EE} = -5.46 V,			1	-40		mA
					2, 3	-44		
High level input current	I_{IH}	V_{IH} = -0.780 V at +25°C -0.650 V at +125°C -0.840 V at -55°C			1		145	µA
					2, 3		225	
Short circuit output current	I_{OS}	GND = 0.0 V, V_{EE} = -5.46 V, V_{IL} = -1.950 V, V_{CC} = +5.0 V, V_{OUT} = 0.0 V			1, 3	-150	-60	mA
					2	-150	-60	
Reference bias supply voltage	V_{BB}	V_{EE} = -5.46 V, V_{CC} = +5.0 V, GND = 0.0 V			1	-1.37	-1.25	V
					2	-1.31	-1.19	
					3	-1.41	-1.27	
Low level output voltage	V_{OL2}	V_{EE} = -5.46 V, V_{CC} = +5.0 V, All inputs = -5.46 V, GND = 0.0 V			1, 3		0.5	V
					2		0.5	
Supply current high	I_{CCH}	V_{EE} = -5.2 V, V_{CC} = +5.5 V, GND = 0.0 V	Inverting inputs = -0.840 V		1		63	mA
			Inverting inputs = -0.780 V		2		63	
			Inverting inputs = -0.650 V		3		63	
Supply current low	I_{CCL}	Inverting inputs = -1.950 V, V_{CC} = +5.5 V, V_{EE} = -5.2 V, GND = 0.0 V			1, 2, 3		40	mA
Functional tests		See 4.3.1c			7			

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified			Group A subgroups	Limits		Unit
						Min	Max	
Cases E, F and X		Rapid tests 3/						
High level output voltage	V_{OH}	V_{EE} = -5.2 V, 2/ V_{CC} = +5.0 V, Load = -2 mA, GND = 0.0 V	V_{IH} = -0.791	V_{IL} = -1.950	1	2.500		V
			-0.662	-1.950	2	2.500		
			-0.852	-1.950	3	2.500		
Low level output voltage	V_{OL}		-0.791	-1.950	1		0.500	V
			-0.662	-1.950	2		0.500	
			-0.852	-1.950	3		0.500	
High level threshold output voltage	V_{OHA}		-1.121	-1.484	1	2.500		V
			-0.972	-1.469	2	2.500		
			-1.172	-1.514	3	2.500		
Low level threshold output voltage	V_{OLA}		-1.121	-1.484	1		0.500	V
			-0.972	-1.469	2		0.500	
			-1.172	-1.514	3		0.500	
Power supply drain current	I_{EE} 4/	GND = 0.0 V, V_{CC} = +5.0 V, V_{EE} = -5.46 V,			1	-39		mA
					2, 3	-43		
High level input current	I_{IH}	V_{IH} = -0.791 V at +25°C -0.662 V at +125°C -0.852 V at -55°C			1		130	µA
					2, 3		210	
Short circuit output current	I_{OS}	V_{EE} = -5.46 V, V_{IL} = -1.950 V, V_{CC} = +5.0 V, GND = 0.0 V, V_{OUT} = 0.0 V			1, 3	-150	-60	mA
					2	-150	-60	
Reference bias supply voltage	V_{BB}	V_{EE} = -5.46 V, V_{CC} = +5.0 V, GND = 0.0 V			1	-1.380	-1.260	V
					2	-1.321	-1.201	
					3	-1.421	-1.280	
Low level output voltage	V_{OL2}	V_{EE} = -5.46 V, V_{CC} = +5.0 V, All inputs = -5.46 V, GND = 0.0 V			1, 3		0.5	V
					2		0.5	
Supply current high	I_{CCH}	V_{EE} = -5.2 V, V_{CC} = +5.0 V, GND = 0.0 V	Inverting inputs = -0.791 V		1		63	mA
			Inverting inputs = -0.662 V		2		63	
			Inverting inputs = -0.852 V		3		63	
Supply current low	I_{CCL}	Inverting inputs = -1.950 V, V_{EE} = -5.2 V, V_{CC} = +5.0 V, GND = 0.0 V			1, 2, 3		40	mA
Functional tests		See 4.3.1c			7			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified			Group A subgroups	Limits		Unit
						Min	Max	
Case 2		Rapid tests 3/						
			V_{IH}	V_{IL}				
High level output voltage	V_{OH}	V_{EE} = -5.2 V 2/ V_{CC} = +5.0 V Load = -2 mA	-0.797	-1.950	1	2.500		V
			-0.668	-1.950	2	2.500		
			-0.858	-1.950	3	2.500		
Low level output voltage	V_{OL}	GND = 0.0 V	-0.797	-1.950	1		0.500	V
			-0.668	-1.950	2		0.500	
			-0.858	-1.950	3		0.500	
High level threshold output voltage	V_{OHA}	V_{EE} = -5.2 V 2/ V_{CC} = +5.0 V Load = -2 mA	-1.125	-1.485	1	2.500		V
			-0.977	-1.471	2	2.500		
			-1.177	-1.516	3	2.500		
Low level threshold output voltage	V_{OLA}	GND = 0.0 V	-1.125	-1.485	1		0.500	V
			-0.977	-1.471	2		0.500	
			-1.177	-1.516	3		0.500	
Power supply drain current	I_{EE} 4/	GND = 0.0 V, V_{CC} = +5.0 V, V_{EE} = -5.46 V,			1	-39		mA
					2, 3	-43		
High level input current	I_{IH}	V_{IH} = -0.797 V at +25°C -0.668 V at +125°C -0.858 V at -55°C			1		130	µA
					2, 3		210	
Short circuit output current	I_{OS}	GND = 0.0 V, V_{EE} = -5.46 V V_{IL} = -1.950 V, V_{CC} = +5.0 V V_{OUT} = 0.0 V			1, 3	-150	-60	mA
					2	-150	-60	
Reference bias supply voltage	V_{BB}	V_{EE} = -5.46 V V_{CC} = +5.0 V GND = 0.0 V			1	-1.380	-1.260	V
					2	-1.321	-1.201	
					3	-1.421	-1.280	
Low level output voltage	V_{OL2}	V_{EE} = -5.46 V, GND = 0.0 V All inputs = -5.46 V, V_{CC} = +5.0 V			1, 3		0.5	V
					2		0.5	
Supply current high	I_{CCH}	V_{EE} = -5.2 V V_{CC} = +5.0 V GND = 0.0 V	Inverting inputs = -0.797 V		1		63	mA
			Inverting inputs = -0.668 V		2		63	
			Inverting inputs = -0.858 V		3		63	
Supply current low	I_{CCL}	Inverting inputs = -1.950 V V_{EE} = -5.2 V, V_{CC} = +5.0 V GND = 0.0 V			1, 2, 3		40	mA
Functional tests		See 4.3.1c			7			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Cases E, F, 2 and X		AC tests				
Transition time	t_{TLH}, t_{THL}	V_{EE} = -3.2 V, V_{CC} = +5.0 V, $C_L \le 5$ pF,	9	0.30	1.30	ns
			10	0.30	2.00	
			11	0.30	1.40	
Propagation delay time	t_{PLH}, t_{PHL}	R_L = 100Ω, GND = 0.0 V, See figure 4.	9	0.85	3.20	ns
			10	0.90	3.50	
			11	0.80	2.90	
Functional tests		See 4.3.1c	7			

1/ The quiescent limits are determined after a device has reached thermal equilibrium. This is defined as the reading taken with the device in a socket with ≥ 500 LFPM of +25° C, +125° C or -55° C (as applicable) air blowing on the unit in a transverse direction with power applied for at least 4 minutes before the reading is taken. This method was used for theoretical limit establishment only. All devices shall be tested to the delta V (rapid test) conditions specified herein. The rapid test method is an equivalent method of testing quiescent conditions.

2/ The high and low level output current varies with temperature and shall be calculated using the following formulas: $I_{OH} = (-2\ V - V_{OH})/100\Omega$ and $I_{OL} = (-2\ V - V_{OL})/100\Omega$.

3/ The dc rapid test forcing functions and limits are used for all dc testing. These limits are determined for each device type based on the power dissipation and package type. The rapid test (delta V) limits and forcing functions are skewed allowing rapid testing to be performed at standard temperatures without the addition of delta T's.

4/ The I_{EE} limits, although specified in the minimum column, shall not be exceeded, in magnitude, as a maximum value.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

Case outlines	E	F and X	2
Terminal number	Terminal symbol		
1	V_{BB}	D_{OUT}	NC
2	$\overline{A}_{IN}$	$\overline{D}_{IN}$	V_{BB}
3	A_{IN}	D_{IN}	$\overline{A}_{IN}$
4	A_{OUT}	GND	A_{IN}
5	B_{OUT}	V_{BB}	A_{OUT}
6	$\overline{B}_{IN}$	$\overline{A}_{IN}$	NC
7	B_{IN}	A_{IN}	B_{OUT}
8	V_{EE}	A_{OUT}	$\overline{B}_{IN}$
9	V_{CC}	B_{OUT}	B_{IN}
10	$\overline{C}_{IN}$	$\overline{B}_{IN}$	V_{EE}
11	C_{IN}	B_{IN}	NC
12	C_{OUT}	V_{EE}	V_{CC}
13	D_{OUT}	V_{CC}	$\overline{C}_{IN}$
14	$\overline{D}_{IN}$	$\overline{C}_{IN}$	C_{IN}
15	D_{IN}	C_{IN}	C_{OUT}
16	GND	C_{OUT}	NC
17	- - -	- - -	D_{OUT}
18	- - -	- - -	$\overline{D}_{IN}$
19	- - -	- - -	D_{IN}
20	- - -	- - -	GND

NC = No connection

FIGURE 1. Terminal connections.

Inputs		Output
Noninverting	Inverting	
L	H	L
H	L	H
L	L	*
H	H	*
Open	Open	L
V_{EE}	V_{EE}	L
L	V_{BB}	L
H	V_{BB}	H
V_{BB}	L	H
V_{BB}	H	L

H = High level voltage
L = Low level voltage
* = Undetermined

FIGURE 2. Truth table.

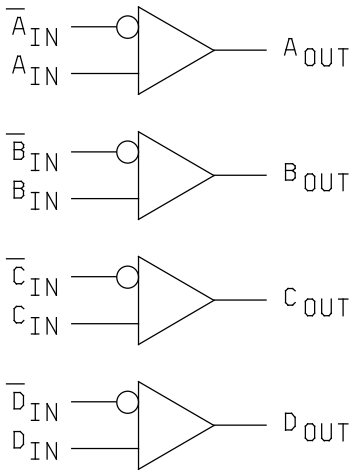
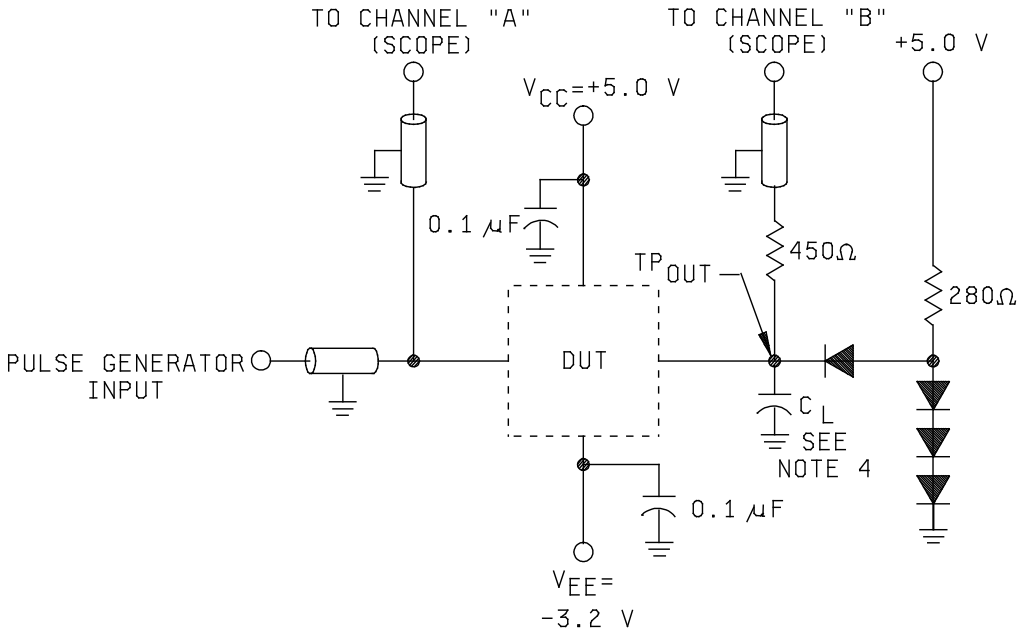
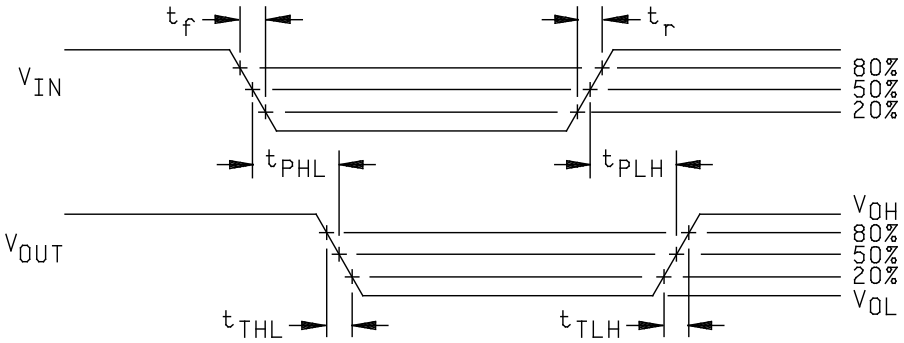


FIGURE 3. Logic diagram.





NOTES:
1. Each output is tested separately.
2. All input and output cables are equal lengths of 50 Ω coaxial cable.
3. All diodes are 1N3064 or equivalent.
4. C_L (test jig) ≤ 5 pF
5. Pulse generator characteristics:
   PRR = 1 MHz, t_r and t_f = 1.0 ns ± 0.2 ns, duty cycle = 50%.

FIGURE 4. Test circuit and switching waveforms.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1 and 7.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 13-06-24

Approved sources of supply for SMD 5962-87508 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8750801EA	57300	AS10H525C16/883C
	60264	MTL10H525EA
5962-8750801FA	60264	MTL10H525FA
	3/	10H525/BFAJC
5962-87508012A	57300	AS10H525EC20/883C
	60264	MTL10H5252A
5962-8750801XA	57300	AS10H525F16/883C

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ No longer available from the approved source of supply

Vendor CAGE number	Vendor name and address
60264	Minco Technology Labs, Inc. 1805 Rutherford Lane. Austin, TX 78754-5101
57300	Micross Components 7725 N. Orange Blossom Trail Orlando, FL 38210-2696