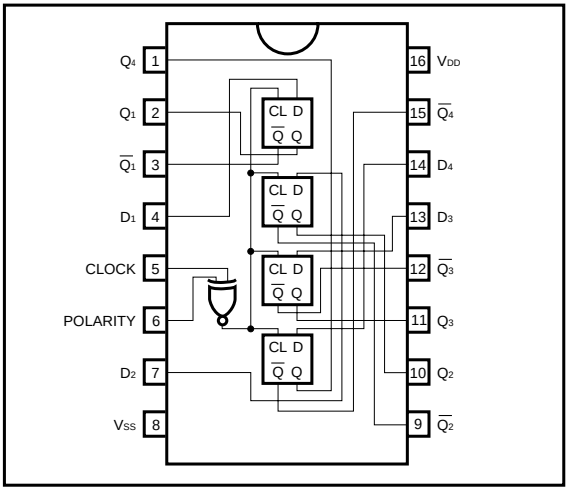
Quad D latch
BU4042B

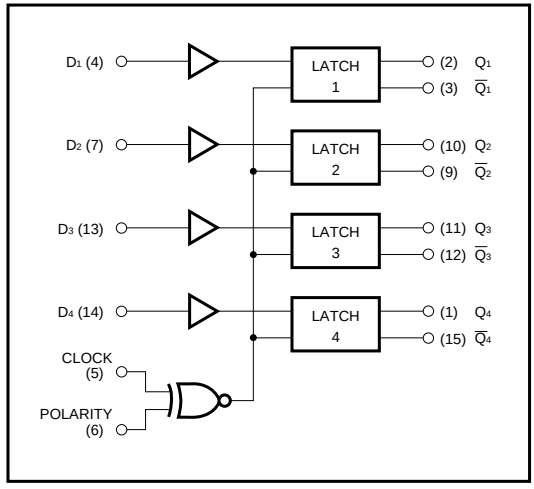
The BU4042B is a four-circuit D latch with a common clock line and separate data input terminals.
When the polarity input is set to “H”, input (D) is presented to output (Q) as is, as long as the clock input is rising, and when the clock input falls, output (Q) holds input (D) at that point. While the clock input is falling, output (Q) does not change even if input (D) changes.
Also, if the polarity input is set to “L”, input (D) is presented to output (Q) as is, as long as the clock input is at “L” level, and when the clock input goes to “H” level, latching takes place.

●Features
1) Low power dissipation.
2) Wide range of operating power supply voltages.
3) High input impedance.
4) High fan-out.
5) Direct drive of 2 L-TTL inputs and 1LS-TTL input.

●Block diagram



●Logic circuit diagram



●Truth table

CLOCK	POLARITY	Q
L	L	D
H	L	LATCH
H	H	D
L	H	LATCH

●Absolute maximum ratings (Ta = 25°C, V_{SS} = 0V)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}	– 0.3 ~ + 18	V
Power dissipation	Pd	1000 (DIP)	mW
Operating temperature	Topr	– 40 ~ + 85	°C
Storage temperature	Tstg	– 55 ~ + 150	°C
Input voltage	V_{IN}	– 0.3 ~ V_{DD} + 0.3	V

●Electrical characteristics

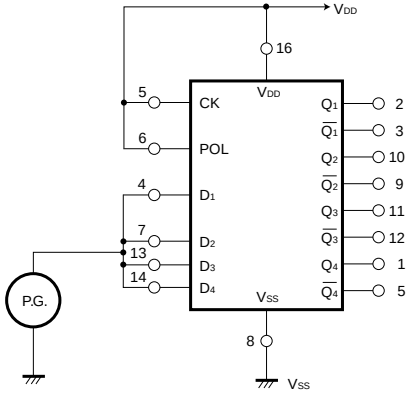
DC characteristics (unless otherwise noted, Ta = 25°C, V_{SS} = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	V_{DD} (V)	Conditions
Input high level voltage (DATA)	V_{IH}	3.5	—	—	V	5	—
		7.0	—	—		10	
		11.0	—	—		15	
Input high level voltage (CLOCK POLARITY)	V_{IH}	3.5	—	—	V	5	—
		7.0	—	—		10	
		11.25	—	—		15	
Input low level voltage (DATA)	V_{IL}	—	—	1.5	V	5	—
		—	—	3.0		10	
		—	—	4.0		15	
Input low level voltage (CLOCK POLARITY)	V_{IL}	—	—	1.5	V	5	—
		—	—	3.0		10	
		—	—	3.75		15	
Input high level current	I_{IH}	—	—	0.3	μA	15	V_{IH} = 15V
Input low level current	I_{IL}	—	—	– 0.3	μA	15	V_{IL} = 0V
Output high level voltage	V_{OH}	4.95	—	—	V	5	I_O = 0mA
		9.95	—	—		10	
		14.95	—	—		15	
Output low level voltage	V_{OL}	—	—	0.05	V	5	I_O = 0mA
		—	—	0.05		10	
		—	—	0.05		15	
Output high level current	I_{OH}	– 0.16	—	—	mA	5	V_{OH} = 4.6V
		– 0.4	—	—		10	V_{OH} = 9.5V
		– 1.2	—	—		15	V_{OH} = 13.5V
Output low level current	I_{OL}	0.44	—	—	mA	5	V_{OL} = 0.4V
		1.1	—	—		10	V_{OL} = 0.5V
		3.0	—	—		15	V_{OL} = 1.5V
Static current dissipation	I_{DD}	—	—	4.0	μA	5	V_I = V_{DD} or GND
		—	—	8.0		10	
		—	—	16.0		15	

Switching characteristics (unless otherwise noted, Ta = 25°C, C_L = 50pF, V_{SS} = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	V_{DD} (V)	Conditions	Measurement circuit
Output rise time	t_{TLH}	—	180	—	ns	5	—	Fig.1
		—	90	—		10		
		—	65	—		15		
Output fall time	t_{THL}	—	100	—	ns	5	—	Fig.1
		—	50	—		10		
		—	40	—		15		
Propagation delay time D→Q, $\overline{Q}$	t_{PLH} t_{PHL}	—	220	—	ns	5	—	Fig.1
		—	90	—		10		
		—	70	—		15		
Propagation delay time CLOCK→Q, $\overline{Q}$	t_{PLH} t_{PHL}	—	220	—	ns	5	—	Fig.2
		—	90	—		10		
		—	70	—		15		
Minimum clock pulse width	t_{WH} t_{WL}	—	150	—	ns	5	—	Fig.2
		—	50	—		10		
		—	40	—		15		
Hold time	t_H	—	50	—	ns	5	—	Fig.2
		—	25	—		10		
		—	20	—		15		
Setup time	t_{SU}	—	50	—	ns	5	—	Fig.2
		—	20	—		10		
		—	5	—		15		
Input capacitance	C_{IN}	—	5	—	pF	—	—	—

●Measurement circuits



Note: Connect C_L = 50pF to each of the output pins.

Fig. 1 (a) Switching characteristics measurement circuit Ⅰ

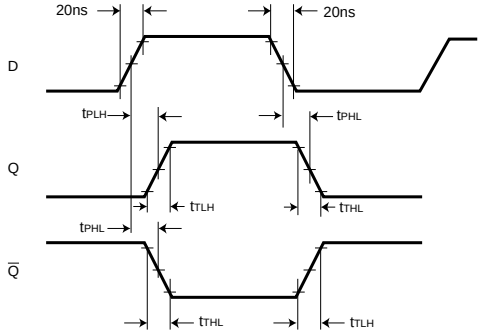
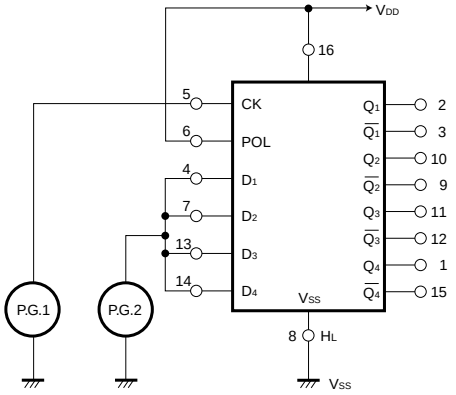


Fig. 1 (b) Switching time measurement waveform Ⅰ



Note : Connect C_L = 50pF to each of the output pins.

Fig. 2 (a) Switching characteristics measurement circuit Ⅱ

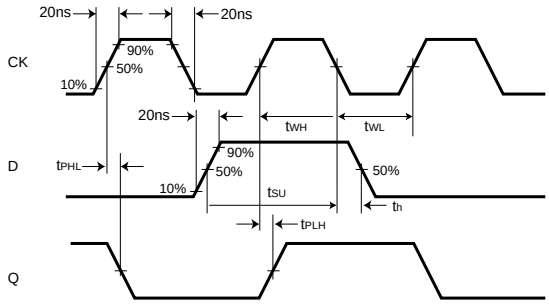


Fig. 2 (b) Switching time measurement waveform Ⅱ

●Electrical characteristic curve

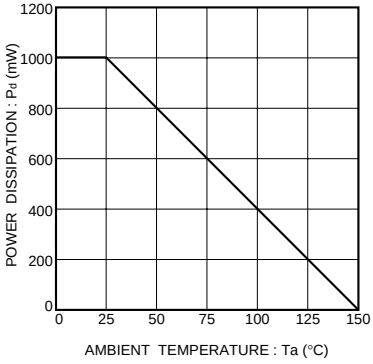


Fig.3 Power dissipation vs. Ta

●External dimensions (Units: mm)