

54LS395A
Shift Register

4-Bit Cascadable Shift Register With 3-State Outputs

Military Logic Products

Product Specification

FEATURES

- 4-bit parallel load shift register
- Independent 3-State buffer outputs
- Separate Q₃ output for serial expansion
- Asynchronous master reset

DESCRIPTION

The 54LS395 is a 4-bit Shift Register with serial and parallel synchronous operating modes and four 3-State buffer outputs. The shifting and loading operations are controlled by the state of the Parallel Enable (PE) input. When PE is High, data is loaded from the Parallel Data inputs (D₀ - D₃) into the register synchronous with the High-to-Low transition of the Clock input (CP). When PE is Low, the

data at the Serial Data input (D_S) is loaded into the Q₀ flip-flop, and the data in the register is shifted one bit to the right in the direction (Q₀→Q₁→Q₂→Q₃) synchronous with the negative clock transition. The PE and Data inputs are fully edge-triggered and must be stable only one setup prior to the High-to-Low transition of the clock.

The Master Reset (MR) is an asynchronous active-Low input. When Low, the MR overrides the clock and all other inputs and clears the register.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, or large capacitive loads. The active-Low Output Enable (OE) controls all four 3-State buffers independent of the register

operation. The data in the register appears at the outputs when OE is Low. The outputs are in the High impedance "off" state, which means they will neither drive nor load the bus when OE is High. The output from the last stage is brought out separately. This output (Q₃) is tied to the Serial Data input (D_S) of the next register for serial expansion applications. The Q₃ output is not affected by the 3-State buffer operation.

ORDERING INFORMATION

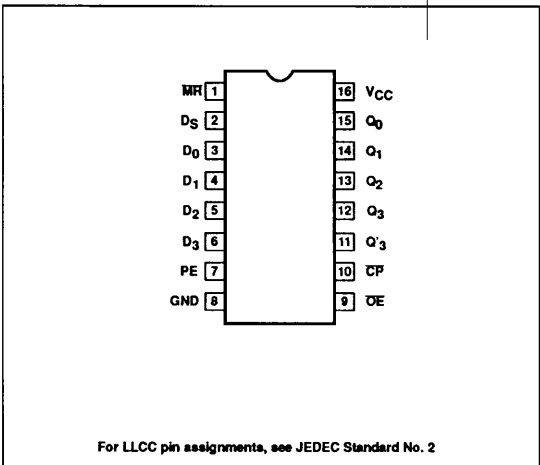
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54LS395A/BEA
16-Pin Ceramic FlatPack	54LS395A/BFA
16-Pin Ceramic LLCC	54LS395A/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

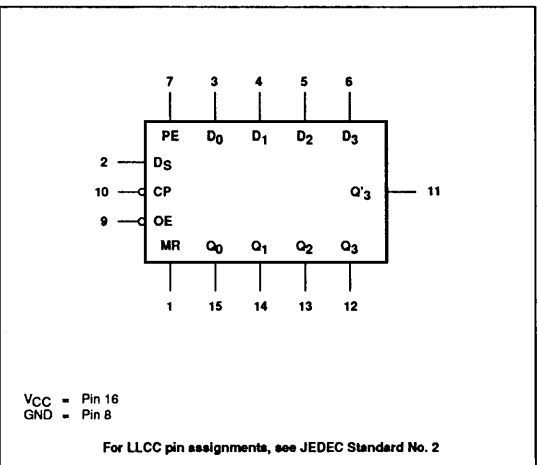
PINS		DESCRIPTION	54LS
All	Inputs		1LSUL
Q ₀ - Q ₃	Outputs		30LSUL
Q ₃	Output		10LSUL

NOTE: Where a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



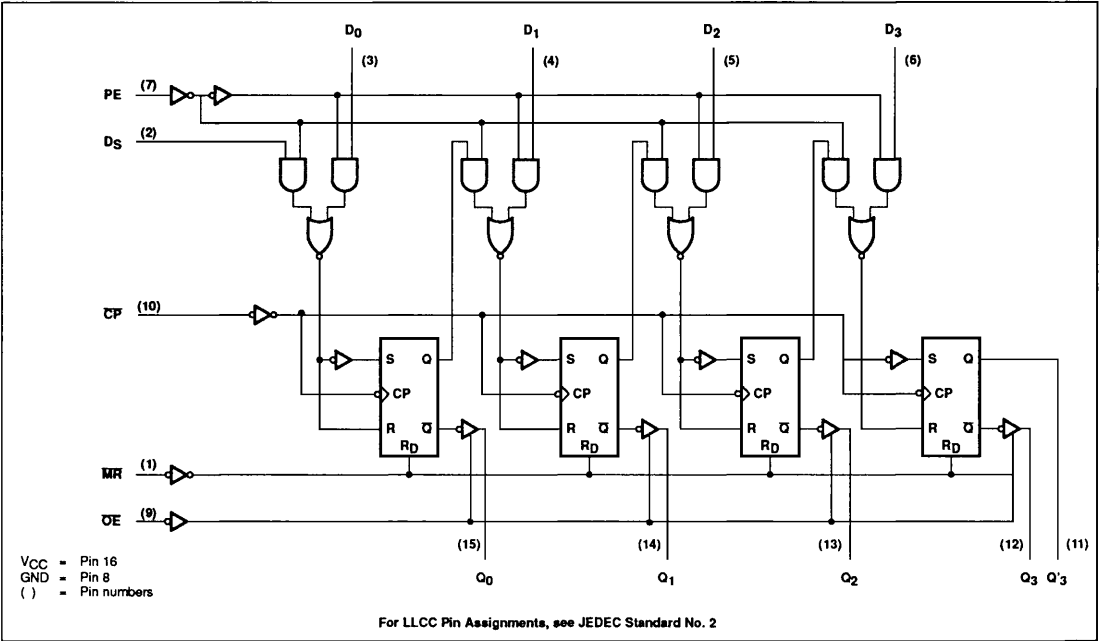
LOGIC SYMBOL



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LOGIC DIAGRAM



FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS					OUTPUTS			
	MR	CP	PE	DS	D _n	Q ₀	Q ₁	Q ₂	Q ₃
Reset (clear)	L	X	X	X	X	L	L	L	L
Shift right	H	↓	l	l	X	L	q ₀	q ₁	q ₂
	H	↓	l	h	X	H	q ₀	q ₁	q ₂
Parallel load	H	↓	h	X	l	L	L	L	L
	H	↓	h	X	h	H	H	H	H

3-STATE BUFFER OPERATING MODES	INPUTS		OUTPUTS	
	OE	Q _n (Register)	Q ₀ , Q ₁ , Q ₂ , Q ₃	Q' ₃
Read	L	L	L	L
	L	H	H	H
Disable buffers	H	L	(Z)	L
	H	H	(Z)	H

H = High voltage level
h = High voltage level one setup time prior to the High-to-Low clock transition
L = Low voltage level
l = Low voltage level one setup time prior to the High-to-Low clock transition
q_n = Lower case letters indicate the state of the referenced output one setup time prior to the High-to-Low clock transition
X = Don't care
(Z) = High impedance "off" state
↓ = High-to-Low transition

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ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to + V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current				
	Q_3			-400	μA
	$Q_0 - Q_3$			-1.0	mA
I_{OL}	Low-level output current				
	Q_3			4	mA
	$Q_0 - Q_3$			12	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT
			Min	Typ ²	Max	
V_{OH}	High-level output voltage	$V_{CC} = \text{Min}, V_{IH} = \text{Min},$ $V_{IL} = \text{Max}, I_{OH} = \text{Max}$				
		Q_3	2.5	3.4		V
		Q_0, Q_1, Q_2, Q_3	2.4	3.1		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{Min}, V_{IH} = \text{Min}, V_{IL} = \text{Max}, I_{OL} = \text{Max}$ Q_0, Q_1, Q_2, Q_3		0.25	0.4	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{Min}, I_I = I_{IK}$			-1.5	V
I_{OZH}	Offstate output current, High-level voltage applied	$V_{CC} = \text{Min}, V_{IH} = \text{Min}, V_O = 2.7V$ Q_0, Q_1, Q_2, Q_3			20	μA
I_{OZL}	Offstate output current, Low-level voltage applied	$V_{CC} = \text{Min}, V_{IH} = \text{Min}, V_O = 0.4V$ Q_0, Q_1, Q_2, Q_3			-20	μA
I_{IH2}	Input current at maximum input voltage	$V_{CC} = \text{Max}, V_I = 7.0V$			0.1	mA
I_{IH1}	High-level input current	$V_{CC} = \text{Max}, V_I = 2.7V$			20	μA
I_{IL}	Low-level input current	$V_{CC} = \text{Max}, V_I = 0.4V$			-0.4	mA
I_{OS}	Short-circuit output current ³	$V_{CC} = \text{Max}$				
		Q_3	-20		-100	mA
		Q_0, Q_1, Q_2, Q_3	-30		-130	mA
I_{CC}	Supply current ⁴ (total)	$V_{CC} = \text{Max}$				
		Condition 1		19	34	mA
		Condition 2		19	31	mA

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AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C _L = 50pF		
			Min	Max	
f _{MAX}	Maximum Clock frequency	Waveform 1	30		MHz
t _{PLH} t _{PHL}	Propagation delay Clock to buffer outputs	Waveform 1		30 30	ns ns
t _{PLH} t _{PHL}	Propagation delay Clock to Q ₃ output	Waveform 1		30 30	ns ns
t _{PHL}	Propagation delay, $\overline{\text{MR}}$ to output	Waveform 2		35	ns
t _{PZH}	Enable time to High level	Waveform 3		25	ns
t _{PZL}	Enable time to Low level	Waveform 4		25	ns
t _{PHZ}	Disable time from High level	Waveform 3, C _L = 5pF ⁵		17	ns
t _{PLZ}	Disable time from Low level	Waveform 4, C _L = 5pF ⁵		20	ns
t _{PHZ}	Disable time from High level	Waveform 3, C _L = 50pF		33	ns
t _{PLZ}	Disable time from Low level	Waveform 4, C _L = 50pF		22	ns

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_W	Clock pulse width	Waveform 1	20		ns
t_W	Master reset pulse width	Waveform 2	25		ns
t_S	Setup time, data to clock	Waveform 5	20		ns
t_h	Hold time, data to clock	Waveform 5	10		ns
t_S	Setup time, PE to clock	Waveform 5	40		ns
t_h	Hold time, PE to clock	Waveform 5	10		ns
t_{rec}	Recovery time, $\overline{\text{MR}}$ to clock	Waveform 2	30		ns

AC ELECTRICAL CHARACTERISTICS $T_A = -55^\circ\text{C}$ and $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V}^6$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 50\text{pF}$		
			Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to buffer outputs	Waveform 1		39 39	ns ns
t_{PLH} t_{PHL}	Propagation delay Clock to Q_3 output	Waveform 1		39 39	ns ns
t_{PHL}	Propagation delay, $\overline{\text{MR}}$ to output	Waveform 2		46	ns
t_{PZH}	Enable time to High level	Waveform 3		33	ns
t_{PZL}	Enable time to Low level	Waveform 4		33	ns
t_{PHZ}	Disable time from High level	Waveform 3, $C_L = 5\text{pF}^5$		22	ns
t_{PLZ}	Disable time from Low level	Waveform 4, $C_L = 5\text{pF}^5$		26	ns
t_{PHZ}	Disable time from High level	Waveform 3, $C_L = 50\text{pF}$		43	ns
t_{PLZ}	Disable time from Low level	Waveform 4, $C_L = 50\text{pF}$		29	ns

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AC SETUP REQUIREMENTS $T_A = -55^\circ\text{C}$ and $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_W	Clock pulse width	Waveform 1	20		ns
t_W	Master reset pulse width	Waveform 2	25		ns
t_S	Setup time, data to clock	Waveform 5	20		ns
t_h	Hold time, data to clock	Waveform 5	10		ns
t_S	Setup time, PE to clock	Waveform 5	40		ns
t_h	Hold time, PE to clock	Waveform 5	10		ns
t_{rec}	Recovery time, MR to clock	Waveform 2	30		ns

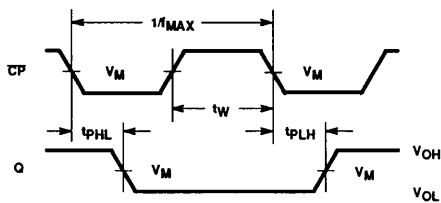
NOTES:

- For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with D_S and Master Reset at $\geq 4.0\text{V}$. The Data inputs grounded and outputs open under the following conditions: *Condition 1*: OE at $\geq 4.0\text{V}$. A momentary 3V, then ground, applied to CP. *Condition 2*: Ground OE and CP inputs.
- Guaranteed by the 50pF limits, but not tested.
- These parameters are guaranteed, but not tested.

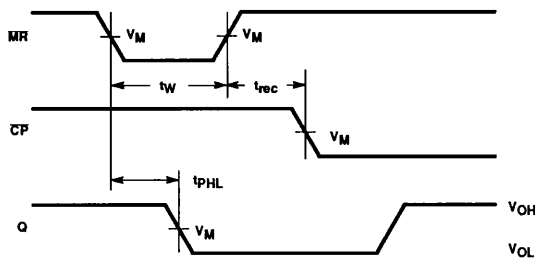
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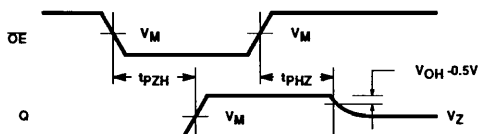
AC WAVEFORMS



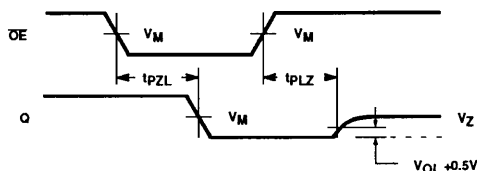
Waveform 1. Clock to Output Delays and Clock Pulse Width



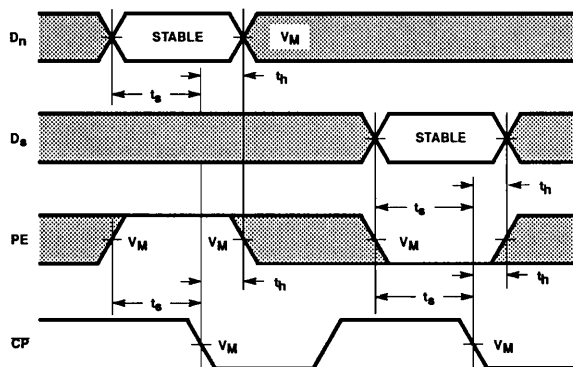
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Waveform 3. 3-State Enable Time to High Level and Disable Time from High Level



Waveform 4. 3-State Enable Time to Low Level and Disable Time from Low Level



Waveform 5. Parallel Enable and Data Setup and Hold Times

FAMILY	V _M	V _{MZL}	V _{MZH}	V _Z
54LSXXX	1.3V	0.7V	1.9V	1.45V

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TEST CIRCUIT AND WAVEFORM

