Features

- Using external 32.768kHz quartz crystal
- Supports I^2C-Bus's high speed mode (400 kHz)
- Includes time (Hour/Minute/Second) and calendar (Year/Month/Date/Day) counter functions (BCD code)
- Automatic power-fail detect and switch circuitry of battery backup
- Operating range: 2.0V to 5.5V
- Software clock calibration
- Ultra-low battery supply current of 1μA

Ordering Information

Part Number	Package
PT7C4300W	8-Pin SOIC
PT7C4300WE	Lead free 8-Pin SOIC

Description

The PT7C4300 serial real-time clock is a low-power clock/calendar with a programmable square-wave output.

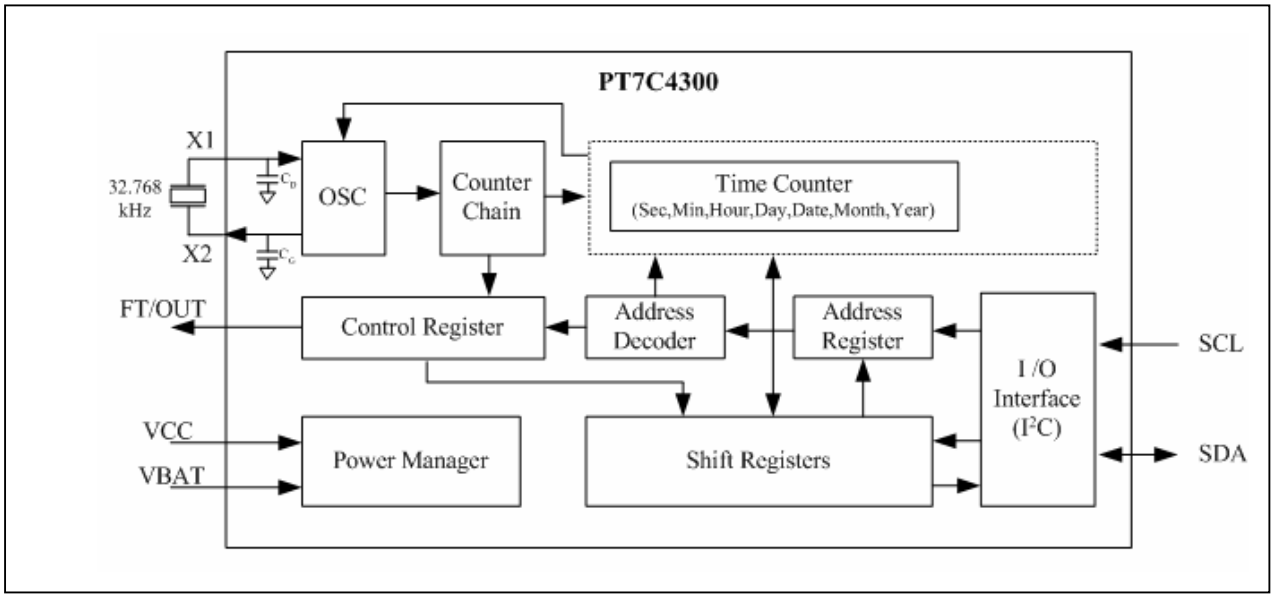
Address and data are transferred serially via a 2-wire bidirectional bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in the 24-hour format indicator.

Table 1 shows the basic functions of PT7C4300. More details are shown in section: overview of functions.

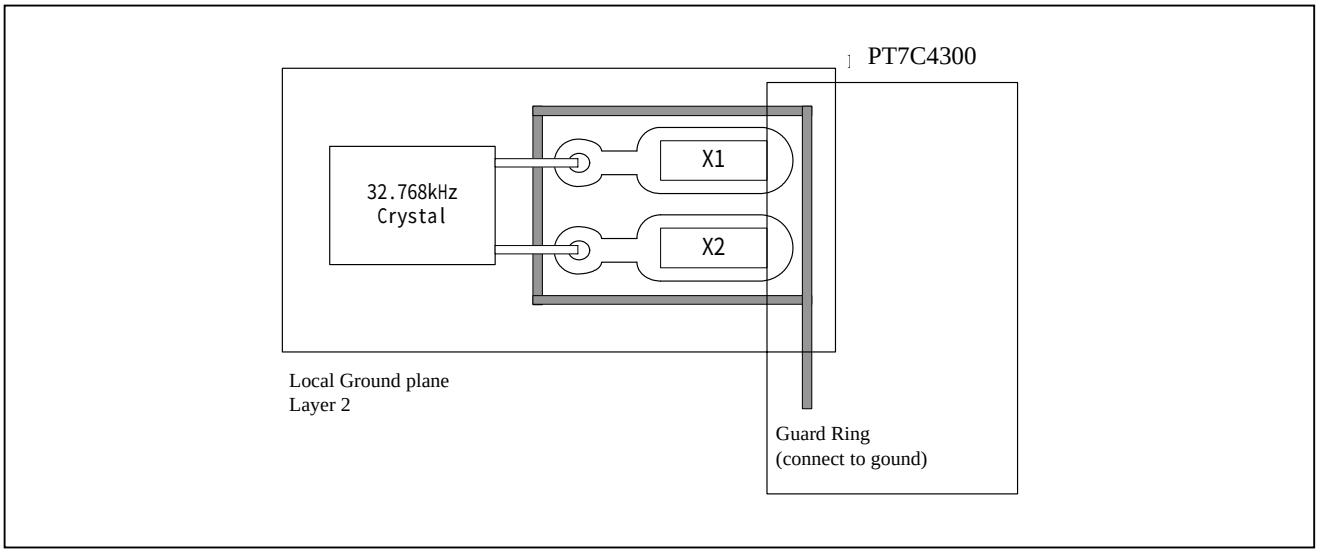
Table 1. Basic functions of PT7C4300

Item	Function			PT7C4300
1	Oscillator	Source: Crystal: 32.768kHz		√
		Oscillator enable/disable		√
		Oscillator fail detect		-
2	Time	Time display	12-hour	-
			24-hour	√
		Century bit		√
		Time count chain enable/disable		√
3	Programmable square wave output (Hz)			512Hz
4	Programmable high/low level output			√
5	Communication	2-wire I^2C bus		√
		3-wire bus		-
		Burst mode		-
6	Battery backup			√
7	Clock calibration			√

Function Block



Recommended Layout for Crystal

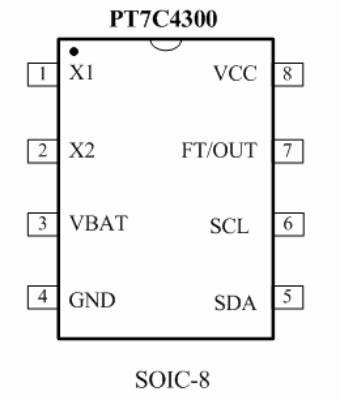


Crystal Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Nominal Frequency	f_O		32.768		kHz
Series Resistance	ESR			40	kΩ
Load Capacitance	C_L		12.5		pF

The crystal, traces and crystal input pins should be isolated from RF generating signals.

Pin Configuration



Pin Description

Pin no.	Pin	Type	Description
1	X1	I	**Oscillator Circuit Input.** Together with X1, 32.768kHz crystal is connected between them. Or external clock input.
2	X2	O	**Oscillator Circuit Output.** Together with X1, 32.768kHz crystal is connected between them.
3	VBAT	P	**Battery Supply Voltage.**
4	GND	P	**Ground.**
5	SDA	I/O	**Serial Data Input/Output.** SDA is the input/output pin for the 2-wire serial interface. The SDA pin is open-drain output and requires an external pull-up resistor.
6	SCL	I	**Serial Clock Input.** SCL is used to synchronize data movement on the I^2C serial interface.
7	FT/OUT	O	**Frequency Test / Output Driver.** Open drain. 512Hz output when Frequency Test is selected. Output DC level by register selection. Frequency Test is prior.
8	VCC	P	**Supply Voltage.**

Function Description

Overview of Functions

1. Clock function

CPU can read or write data including the year (last two digits), month, date, day, hour, minute, and second. Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2100.

2. Interface with CPU

Data is read and written via the I^2C bus interface using two signal lines: SCL (clock) and SDA (data).

Since the output of the I/O pin SDA is open drain, a pull-up resistor should be used on the circuit board if the CPU output I/O is also open drain.

The SCL's maximum clock frequency is 400 kHz, which supports the I^2C bus's high-speed mode.

3. Oscillator enable/disable

Oscillator and time count chain can be enabled or disabled at the same time by ST bit.

4. Calibration function

With the calibration bits properly set, accuracy PT7C4300 can be improved to better than ±2 ppm at 25°C.

Registers

1. Allocation of registers

Addr. (hex) *1	Function	Register definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	Seconds (00-59)	ST*2	S40	S20	S10	S8	S4	S2	S1
01	Minutes (00-59)	×	M40	M20	M10	M8	M4	M2	M1
02	Hours (00-23)	CEB*3	CB*3	H20	H10	H8	H4	H2	H1
03	Days of the week (01-07)	×	×	×	×	×	W4	W2	W1
04	Dates (01-31)	×	×	D20	D10	D8	D4	D2	D1
05	Months (01-12)	×	×	×*8	MO10	MO8	MO4	MO2	MO1
06	Years (00-99)	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
07	Control*3	OUT*4	FT*5	S*6	Calibration*7				

Caution points:

*1. PT7C4300 uses 3 bits for address. That is if write data to 08H, the data will be written to 00H address register.

*2. Stop bit. When this bit is set to 1, oscillator and time count chain are both stopped.

*3. CEB: Century Enable Bit. CB: Century Bit.

*4. Control FT/OUT pin output DC level when 512Hz square wave is disabled.

*5. Frequency Test. 512Hz square wave output is enabled at FT/OUT pin, which is using for frequency test.

*6. Sign Bit. “1” indicates positive calibration; “0”indicates negative calibration.

*7. Using for modifying count frequency. If 20ppm is wanted to slow down the count frequency, 10 (01010) should be loaded. Calibration will not affect FT/OUT output frequency.

*8. Don’t care.

2. Control and status register

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
07	Control	OUT	FT	S	Calibration				
	(default)	0	0	1	1	1	1	1	1

a) OUT

- **OUT:** Set pin 7 output DC level..

OUT	Data	Description
Read / Write	1	Set high level at pin 7. Default
	0	Set low level at pin 7.

b) 512Hz output

- **FT:** 512Hz square wave output Enable bit, using for Frequency Test.

FT	Data	Description
Read / Write	0	Disable 512Hz output at pin 7. Default
	1	Enable 512Hz output at pin 7.

c) Calibration bits

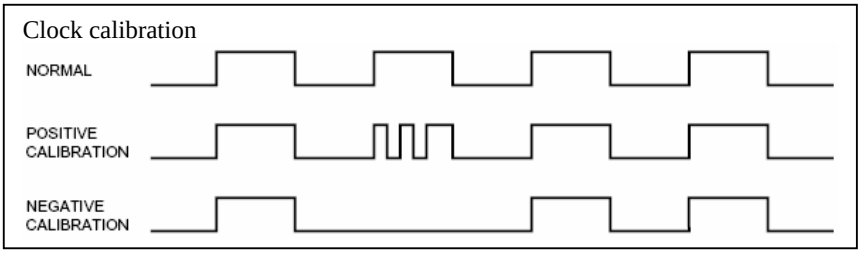
- **S:** Sign bit.

S	Data	Description
Read / Write	1	Indicate positive calibration. Default
	0	Indicate negative calibration.

Calibration:

Calibration occurs within a 64minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on. Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or –2.034 ppm of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768Hz, each of the 31 increments in the Calibration byte would represent +10.7 or –5.35 seconds per month which corresponds to a total range of +5.5 or –2.75 minutes per month.

For example, a reading of 512.01024Hz would indicate a +20 ppm oscillator frequency error, requiring a –10 (XX001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency.



3. Time Counter

Time digit display (in BCD code):

- Second digits: Range from 00 to 59 and carried to minute digits when incremented from 59 to 00.
- Minute digits: Range from 00 to 59 and carried to hour digits when incremented from 59 to 00.
- Hour digits: See description on the /12, 24 bit. Carried to day and day-of-the-week digits when incremented from 11 p.m. to 12 a.m. or 23 to 00.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
00	Seconds	ST	S40	S20	S10	S8	S4	S2	S1
	(default)	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
01	Minutes	×*2	M40	M20	M10	M8	M4	M2	M1
	(default)	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
02	Hours	CEB*3	CB*3	H20	H10	H8	H4	H2	H1
	(default)	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

*** Note 1:** ST bit: Stop oscillation and time count chain.

*** Note 2:** Do not care.

*** Note 3:** Century Enable Bit and Century Bit.

4. Days of the week Counter

The day counter is a divide-by-7 counter that counts from 00 to 06 and up 06 before starting again from 00. Values that correspond to the day of week are user defined but must be sequential (i.e., if 0 equals Sunday, then 1 equals Monday, and so on). Illogical time and date entries result in undefined operation.

The day counter is a divide-by-7 counter that counts from 01 to 07 and up 07 before starting again from 01. Values that correspond to the day of week are user defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
03	Days of the week	×	×	×	×	×	W4	W2	W1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

5. Calendar Counter

The data format is BCD format.

- Day digits: Range from 1 to 31 (for January, March, May, July, August, October and December).
  Range from 1 to 30 (for April, June, September and November).
  Range from 1 to 29 (for February in leap years).
  Range from 1 to 28 (for February in ordinary years).
  Carried to month digits when cycled to 1.
- Month digits: Range from 1 to 12 and carried to year digits when cycled to 1.
- Year digits: Range from 00 to 99 and 00, 04, 08, … , 92 and 96 are counted as leap years.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
04	Dates (01-31) (default)	× Undefined	× Undefined	D20 Undefined	D10 Undefined	D8 Undefined	D4 Undefined	D2 Undefined	D1 Undefined
05	Months (01-12) (default)	× Undefined	× Undefined	× Undefined	M10 Undefined	M8 Undefined	M4 Undefined	M2 Undefined	M1 Undefined
06	Years (00-99) (default)	Y80 Undefined	Y40 Undefined	Y20 Undefined	Y10 Undefined	Y8 Undefined	Y4 Undefined	Y2 Undefined	Y1 Undefined

Communication

1. I^2C Bus Interface

a) Overview of I^2C-BUS

The I^2C bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data signals, acknowledge signals, and so on. Both the SCL and SDA signals are held at high level whenever communications are not being performed. The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level. During data transfers, data changes that occur on the SDA line are performed while the SCL line is at low level, and on the receiving side the data is captured while the SCL line is at high level. In either case, the data is transferred via the SCL line at a rate of one bit per clock pulse. The I^2C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device and the receiving device responds to communications only when its slave address matches the slave address in the received data.

b) System Configuration

All ports connected to the I^2C bus must be either open drain or open collector ports in order to enable AND connections to multiple devices.
SCL and SDA are both connected to the VDD line via a pull-up resistance. Consequently, SCL and SDA are both held at high level when the bus is released (when communication is not being performed).

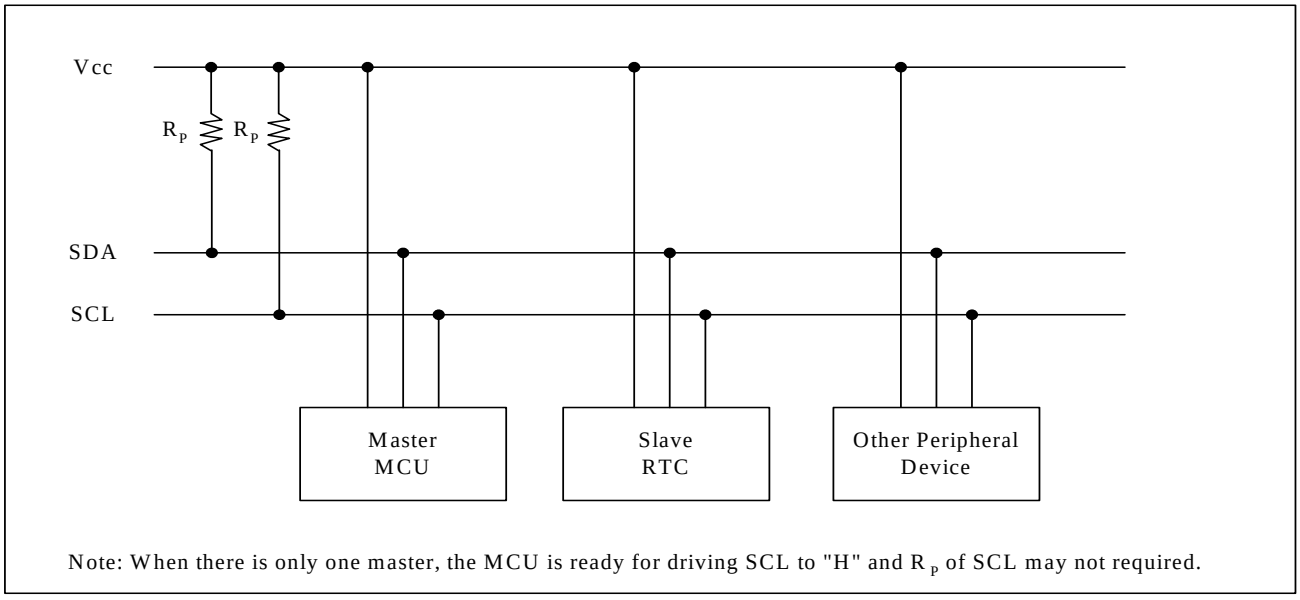


Fig.1 System configuration

c) Starting and Stopping I^2C Bus Communications

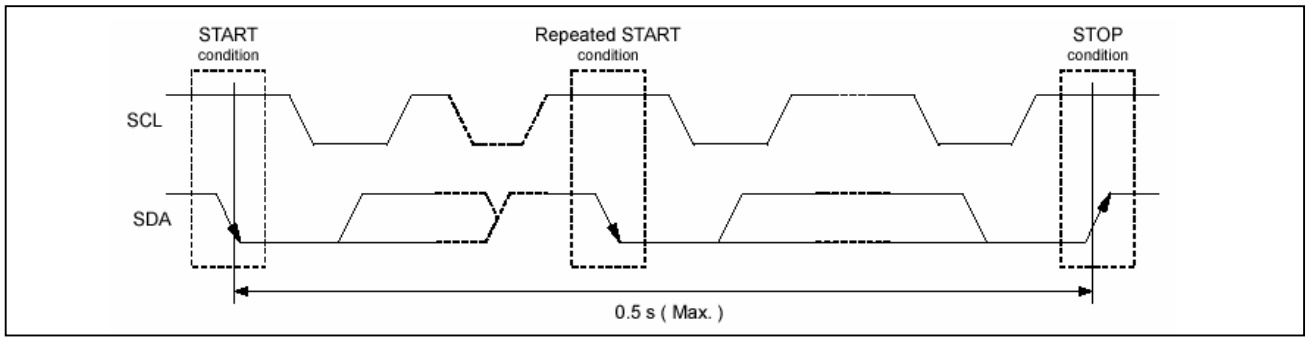


Fig.2 Starting and stopping on I^2C bus

START condition, repeated START condition, and STOP condition

- START condition
  SDA level changes from high to low while SCL is at high level
- STOP condition
  SDA level changes from low to high while SCL is at high level
- Repeated START condition (RESTART condition)
  In some cases, the START condition occurs between a previous START condition and the next STOP condition, in which case the second START condition is distinguished as a RESTART condition. Since the required status is the same as for the START condition, the SDA level changes from high to low while SCL is at high level.

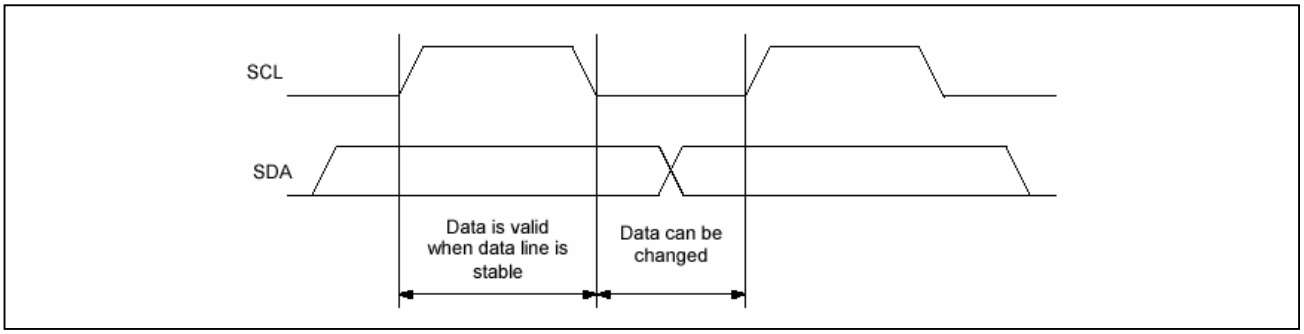
d) Data Transfers and Acknowledge Responses during I^2C-BUS Communication

- **Data transfers**

Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition.

The address auto increment function operates during both write and read operations.

Updating of data on the transmitter (transmitting side)'s SDA line is performed while the SCL line is at low level.
The receiver (receiving side) captures data while the SCL line is at high level.

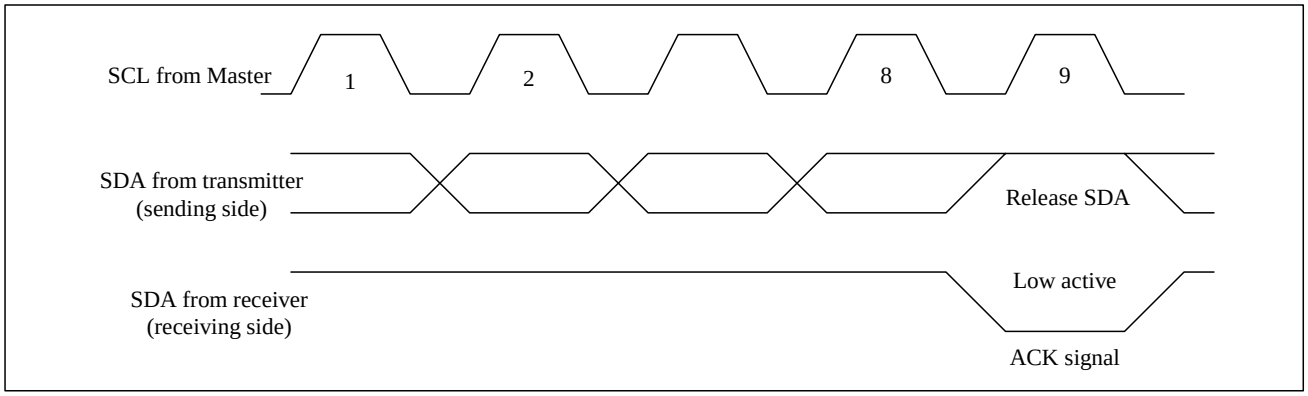


***Note**: with caution that if the SDA data is changed while the SCL line is at high level, it will be treated as a START, RESTART, or STOP condition.

- **Data acknowledge response (ACK signal)**

When transferring data, the receiver generates a confirmation response (ACK signal, low active) each time an 8-bit data segment is received. If there is no ACK signal from the receiver, it indicates that normal communication has not been established. (This does not include instances where the master device intentionally does not generate an ACK signal.)

Immediately after the falling edge of the clock pulse corresponding to the 8th bit of data on the SCL line, the transmitter releases the SDA line and the receiver sets the SDA line to low (= acknowledge) level.



After transmitting the ACK signal, if the Master remains the receiver for transfer of the next byte, the SDA is released at the falling edge of the clock corresponding to the 9th bit of data on the SCL line. Data transfer resumes when the Master becomes the transmitter.

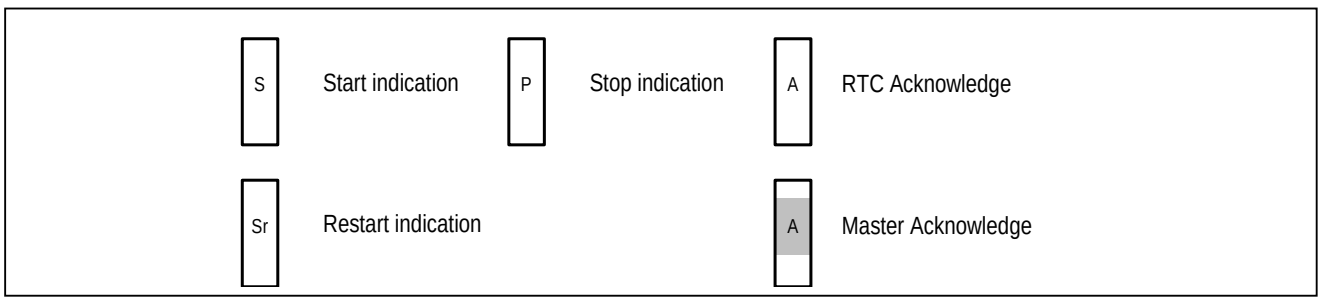
When the Master is the receiver, if the Master does not send an ACK signal in response to the last byte sent from the slave, that indicates to the transmitter that data transfer has ended. At that point, the transmitter continues to release the SDA and awaits a STOP condition from the Master.

e) Slave Address

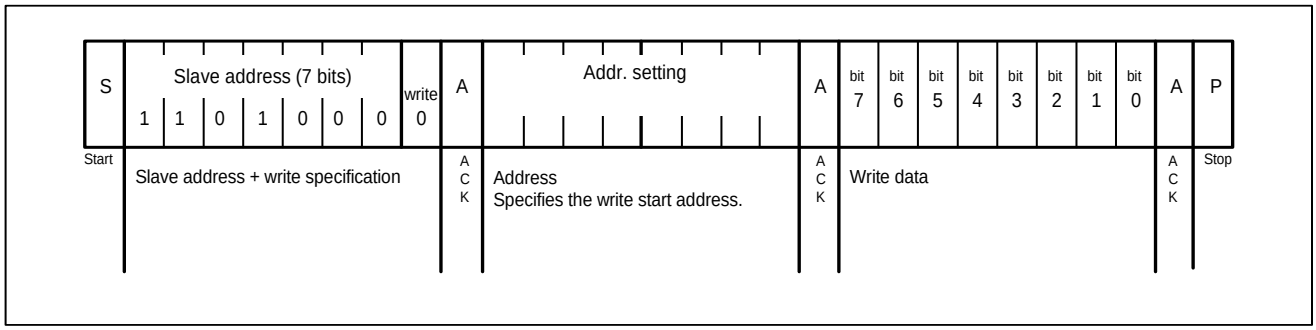
The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device.
All communications begin with transmitting the [START condition] + [slave address (+ R/$\overline{W}$ specification)]. The receiving device responds to this communication only when the specified slave address it has received matches its own slave address.
Slave addresses have a fixed length of 7 bits. See table for the details.
An R/$\overline{W}$ bit is added to each 7-bit slave address during 8-bit transfers.

Operation	Transfer data	Slave address							R / $\overline{W}$ bit
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Read	D1 h	1	1	0	1	0	0	0	1 (= Read)
Write	D0 h								0 (= Write)

2. I²C Bus's Basic Transfer Format

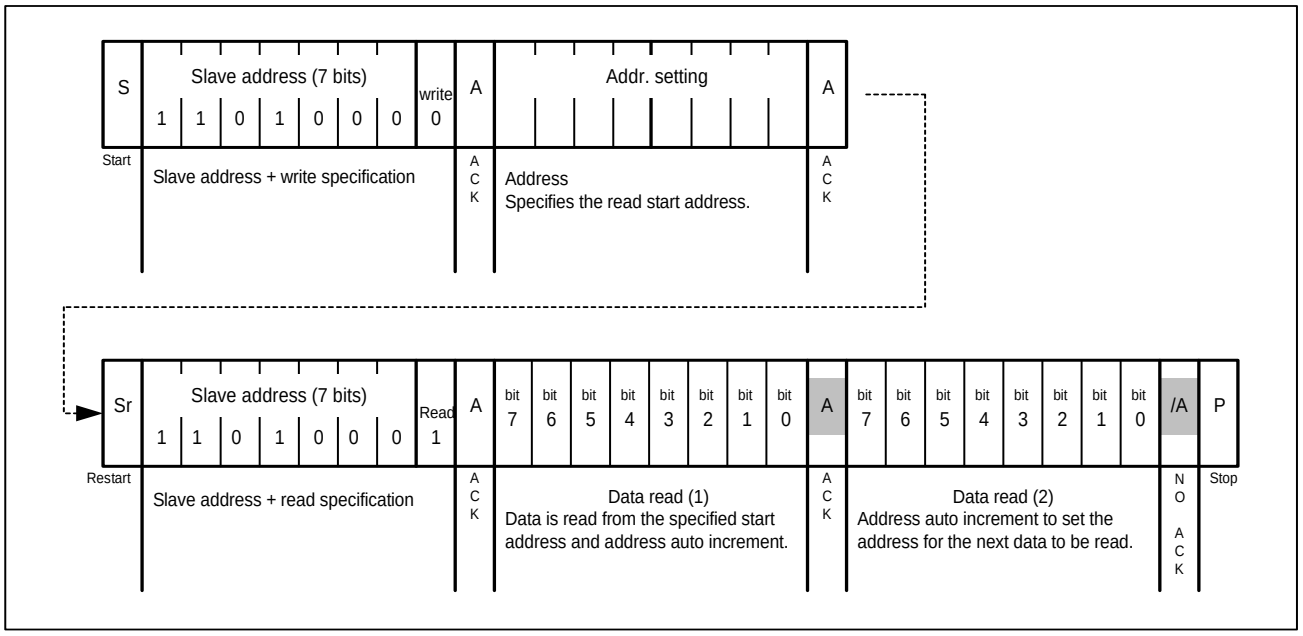


a) Write via I²C bus

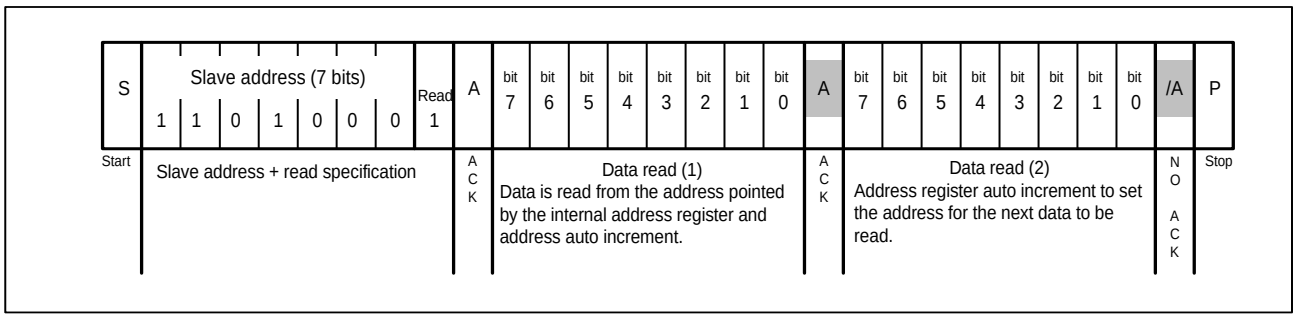


b) Read via I²C bus

- **Standard read**



- **Simplified read**

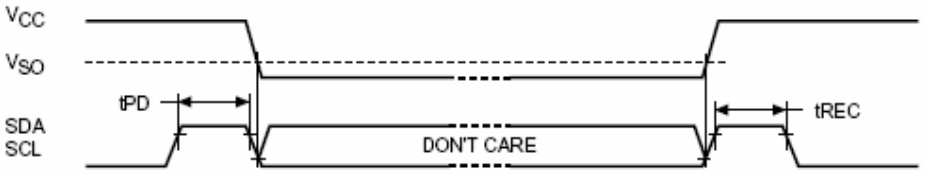


Note:

1. The above steps are an example of transfers of one or two bytes only. There is no limit to the number of bytes transferred during actual communications.
2. 49H, 4AH are used as test mode address. Customer should not use the addresses.

3. Data Retention Mode

With valid VCC applied, the PT7C4300 can be accessed as described above with READ or WRITE Cycles. Should the supply voltage decay, the PT7C4300 will automatically deselect, write protecting itself when VCC falls.



Sym.	Parameter	Min	Max	Unit
tPD	SCL and SDA at VIH before Power Down	0		ns
tREC	SCL and SDA at VIH after Power Up	10		μs

Note: 1. Valid for Ambient Operating Temperature: T_A = –40 to 85°C; VCC = 2.0 to 5.5V (except where noted).
2. VCC fall time should not exceed 5mV/μs.

Maximum Ratings

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Vcc to GND)	-0.3V to +6.5V
DC Input (All Other Inputs except Vcc & GND)	-0.3V to (V_{cc}+0.3V)
DC Output Voltage (SDA, /INTA, /INTB pins)	-0.3V to +6.5V
Power Dissipation	320mW (Depend on package)

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Description	Min	Type	Max	Unit
V_{CC}	Power voltage	2.0	-	5.5	V
V_{IH}	Input high level	0.7 V_{CC}	-	V_{CC}+0.3	
V_{IL}	Input low level	-0.3	-	0.3 V_{CC}	
T_A	Operating temperature	-40	-	85	ºC

DC Electrical Characteristics

(Unless otherwise specified, V_{CC} = 2.0 ~ 5.5 V, T_A = -40 °C to +85 °C.)

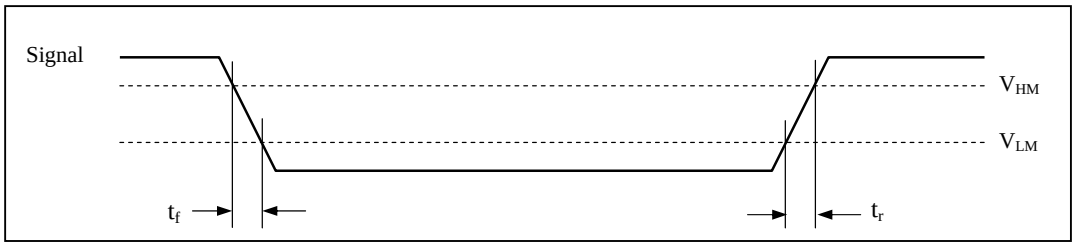
Sym.	Item	Pin	Condition	Min	Typ	Max	Unit
V_{CC}	Supply voltage	V_{CC}		2.0		5.5	V
V_{BAT}[1]	Supply voltage	V_{BATT}		2.5	3	3.5	V
V_{SO}[2]	Condition for V_{CC} switch to V_{BAT}	-	-	-	V_{CC} < V_{BAT} - 0.1v	-	V
	Condition for V_{BAT} switch to V_{CC}	-	-		V_{CC} > V_{BAT}		
I_{CC}	Current consumption	V_{CC}	Switch freq. = 100kHz			300	µA
I_{ST}	Standby current	V_{CC}	SDA, SCL = V_{CC} – 0.3V			150	µA
I_{BAT}	Current consumption	V_{BAT}	OSC on, V_{CC} = 0V, V_{BAT} = 3V, T_A=25°C		650	800	nA
V_{IL}	Low-level input voltage			-0.3		$0.3V_{CC}$	V
V_{IH}	High-level input voltage			$0.7V_{CC}$		V_{CC} +0.5	
V_{OL}	Low-level output voltage	SDA	I_{OL} = 3mA			0.4	V
I_{IL}	Input leakage current	SCL	$0<V_{IN}<V_{CC}$			±1	µA
I_{OZ}	Output current when OFF	SDA	$0<V_{OUT}<V_{CC}$			±1	µA

Note:

1. After switchover (V_{SO}), V_{BAT}(min) can be 2.0V for crystal with R_S=40kΩ.
2. Switch-over and deselect point.

AC Electrical Characteristics

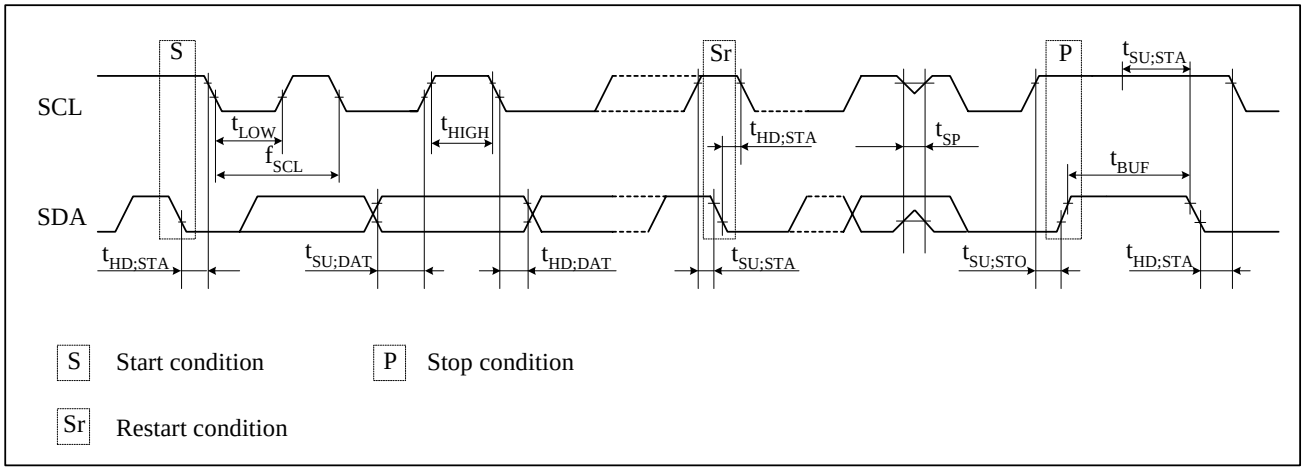
Sym	Description	Value	Unit
V_{HM}	Rising and falling threshold voltage high	0.8 V_{CC}	V
V_{HL}	Rising and falling threshold voltage low	0.2 V_{CC}	V



Over the operating range

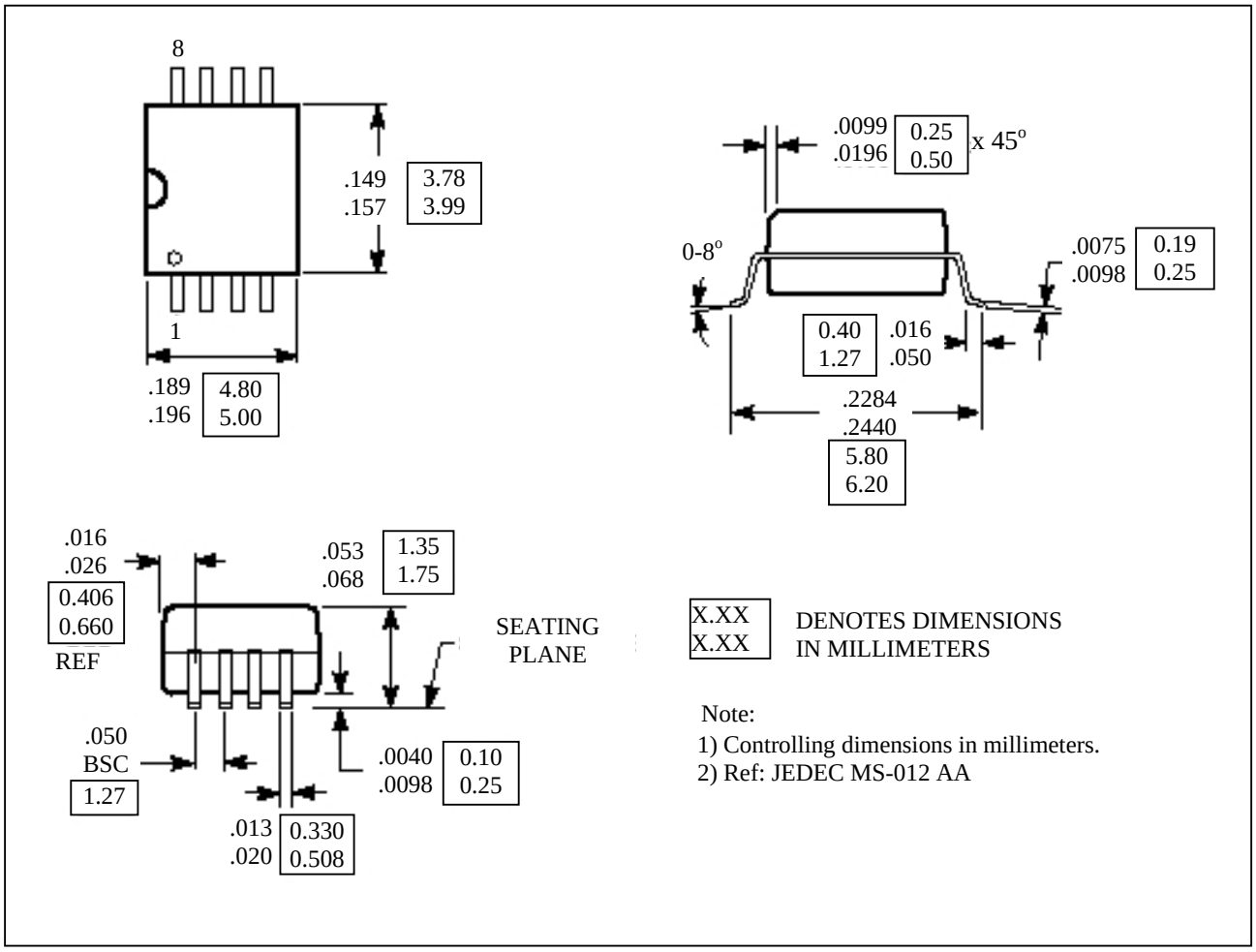
Symbol	Item	Min.	Typ.	Max.	Unit
f_{SCL}	SCL clock frequency			400	kHz
$t_{SU;STA}$	START condition set-up time	0.6			µs
$t_{HD;STA}$	START condition hold time	0.6			µs
$t_{SU;DAT}$	Data set-up time (RTC read/write)	200			ns
$t_{HD;DAT1}$	Data hold time (RTC write)	35			ns
$t_{HD;DAT2}$	Data hold time (RTC read)	0			µs
$t_{SU;STO}$	STOP condition setup time	0.6			µs
t_{BUF}	Bus idle time between a START and STOP condition	1.3			µs
t_{LOW}	When SCL = "L"	1.3			µs
t_{HIGH}	When SCL = "H"	0.6			µs
t_r	Rise time for SCL and SDA			0.3	µs
t_f	Fall time for SCL and SDA			0.3	µs
t_{SP}*	Allowable spike time on bus			50	ns
C_B	Capacitance load for each bus line			400	pF

*** Note:** Only reference for design.



Mechanical Information

W/WE 8-Pin SOIC



Notes

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