Signetics

74199
Shift Register

8-Bit Parallel-Access Shift Register
Product Specification

Logic Products

FEATURES
- **Buffered clock and control inputs**
- **Shift right and parallel load capability**
- **Fully synchronous data transfers**
- **J-$\overline{K}$ (D) inputs to first stage**
- **Clock enable for hold (do nothing) mode**
- **Asynchronous Master Reset**

DESCRIPTION

The functional characteristics of the '199 8-Bit Parallel-Access Shift Register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
74199	35MHz	90mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74199N

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74
All	Inputs	1ul
$Q_0 - Q_7$	Parallel outputs	10ul

NOTE:
A 74 unit load (ul) is understood to be 40μA I_{IH} AND −1.6mA I_{IL}.

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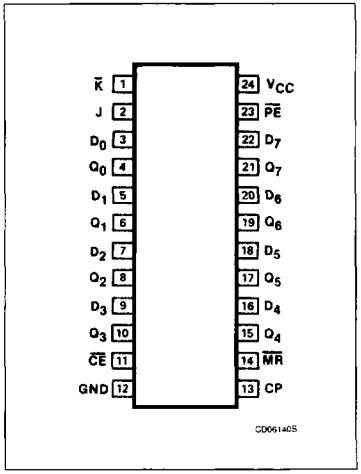
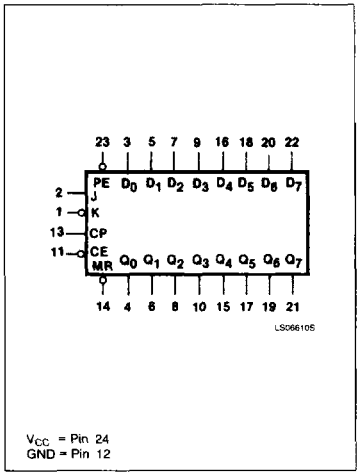
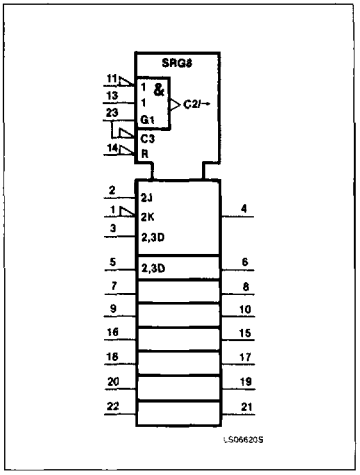
PIN CONFIGURATION



LOGIC SYMBOL

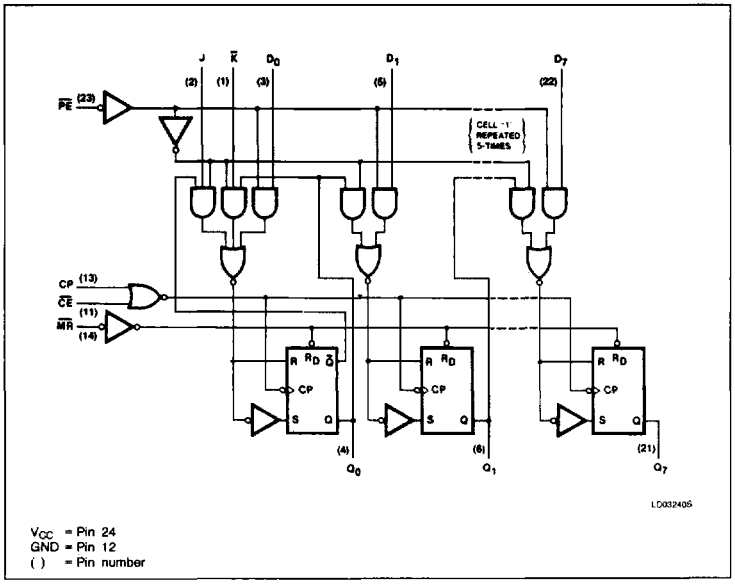


LOGIC SYMBOL (IEEE/IEC)



Shift Register | 74199

LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS							OUTPUTS				
	$\overline{MR}$	CP	$\overline{CE}$	$\overline{PE}$	J	$\overline{K}$	D_n	Q_0	Q_1	.....	Q_6	Q_7
Reset (clear)	L	X	X	X	X	X	X	L	L	.....	L	L
Shift, set first stage	H	↑	l	h	h	h	X	H	q_0	.....	q_5	q_6
Shift, reset first stage	H	↑	l	h	l	l	X	L	q_0	.....	q_5	q_6
Shift, toggle first stage	H	↑	l	h	h	l	X	$\overline{q}_0$	q_0	.....	q_5	q_6
Shift, retain first stage	H	↑	l	h	l	h	X	q_0	q_0	.....	q_5	Q_6
Parallel load	H	↑	l	l	X	X	d_n	d_0	d_1	.....	d_6	d_7
Hold (do nothing)	H	↑	h[a]	X	X	X	X	q_0	q_1	.....	q_6	q_7

H = HIGH voltage level steady state.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
X = Don't care
$d_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH clock transition.
↑ = LOW-to-HIGH clock transition.

NOTE:
a. The LOW-to-HIGH transition of $\overline{CE}$ should only occur while CP is HIGH for conventional operation.

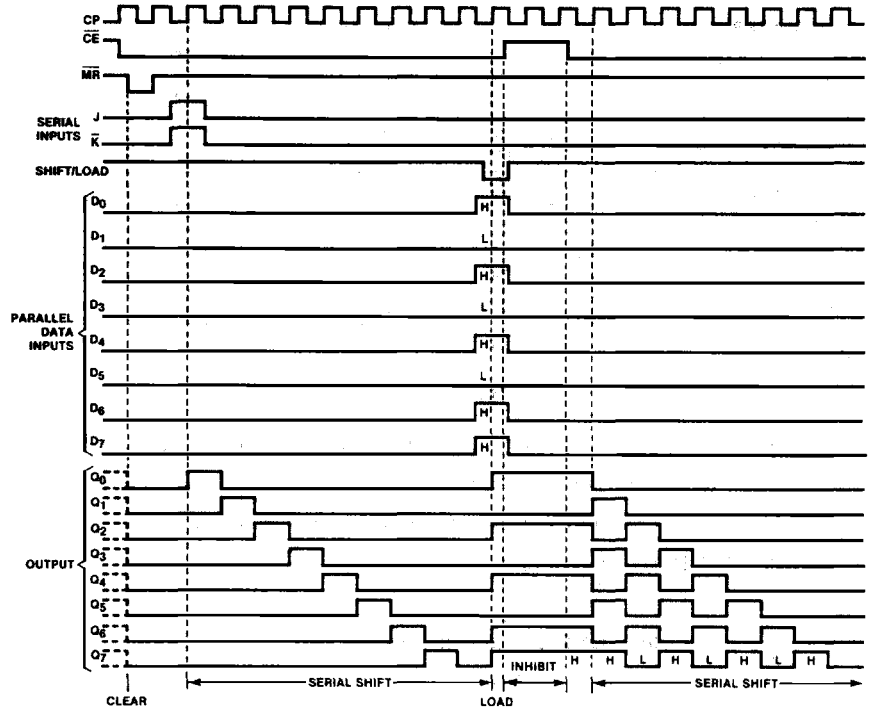
The '199 operates in two primary modes: shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q_0) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is HIGH, and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_3$ following each LOW-to-HIGH clock transition. The J and $\overline{K}$ inputs provide the flexibility of the J-K type input for special applications and, by tying the two pins together, the simple D-type input for general applications. The device appears as eight common clocked D flip-flops when the $\overline{PE}$ input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs ($D_0 - D_7$) is transferred to the respective $Q_0 - Q_7$ outputs.

All parallel and serial data transfers are synchronous, occuring after each LOW-to-HIGH clock transition. The '199 utilizes edge-triggering, therefore, there is no restriction on the activity of the J, $\overline{K}$, D_n, and $\overline{PE}$ inputs for logic operation, other than the set-up and release time requirements.

The clock input is a gated OR structure which allows one input to be used as an active-LOW Clock Enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of $\overline{CE}$ input should only take place while the CP is HIGH for conventional operation.

A LOW on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

TYPICAL CLEAR, LOAD, RIGHT-SHIFT, LEFT-SHIFT, INHIBIT AND CLEAR SEQUENCES



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			−12	mA
I_{OH}	HIGH-level output current			−800	V
I_{OL}	LOW-level output current			16	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]	74199			UNIT
			Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	2.4	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX		0.2	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V			1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V			40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V			−1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX	−18		−57	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX		90	127	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with $\overline{R}$, J and D inputs at 4.5V, momentary ground clock, then apply 4.5V, ground $\overline{CE}$, $\overline{MR}$ and $\overline{PE}$.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

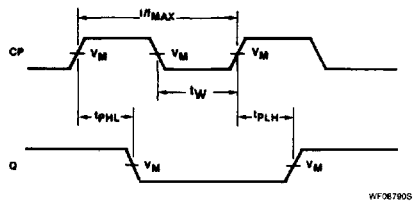
PARAMETER		TEST CONDITIONS	74		UNIT
			C_L = 15pF, R_L = 400Ω		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		26 30	ns
t_{PHL}	Propagation delay $\overline{MR}$ to output	Waveform 2		35	ns

Per industry convention, f_{MAX} is the worst case of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SET-UP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

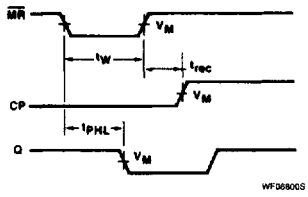
PARAMETER		TEST CONDITIONS	74		UNIT
			Min	Max	
t_W	Clock pulse width	Waveform 1	20		ns
t_W	$\overline{MR}$ pulse width	Waveform 2	20		ns
t_s	Set-up time, J, $\overline{K}$ and data to clock	Waveform 3	20		ns
t_h	Hold time, J, $\overline{K}$ and data to clock	Waveform 3	0		ns
t_s	Set-up time, $\overline{CE}$ to clock	Waveform 3	30		ns
t_h	Hold time, $\overline{CE}$ to clock	Waveform 3	0		ns
t_s	Set-up time, $\overline{PE}$ to clock	Waveform 3	30		ns
t_h	Hold time, $\overline{PE}$ to clock	Waveform 3	0		ns
t_{rec}	Recovery time, $\overline{MR}$ to clock	Waveform 2	30		ns

AC WAVEFORMS

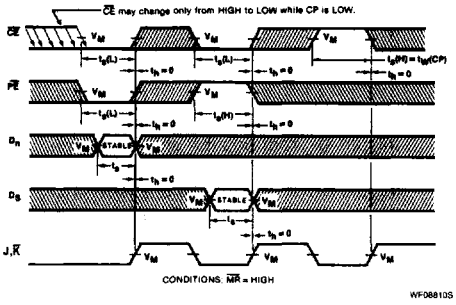


The number of clock pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the appropriate Truth Tables.

Waveform 1. Clock To Output Delays And Clock Pulse Width



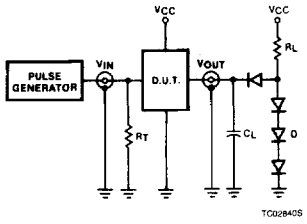
Waveform 2. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time



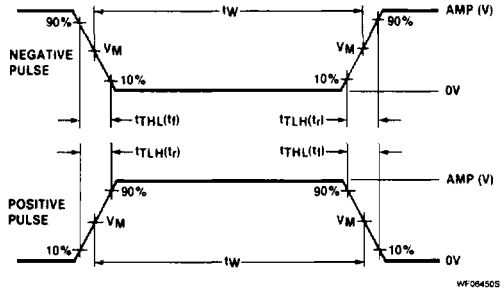
For all waveforms, V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.
The shaded areas indicate when the input is permitted to change for predictable performances.

Waveform 3

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Totem-Pole Outputs



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

DEFINITIONS
R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns