SK10/100EL91W
Triple PECL to ECL/LVECL and LVPECL to ECL/LVECL Translator

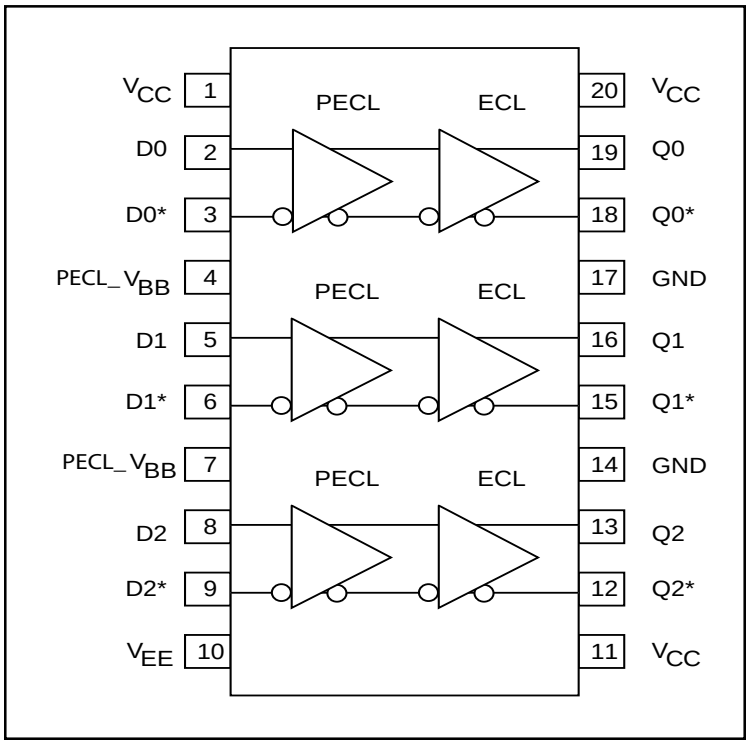
Description

The SK10/100EL91W is a triple PECL to ECL/LVECL and LVPECL to ECL/LVECL translator. It is fully compatible with MC100EL91 and MC100LVEL91. The SK10/100EL91W provides a V_{BB} output for single-ended use or DC bias for AC coupling to the device. V_{BB} is an output pin and should be used as a bias for the EL91W as its current source/sink capability is limited. Whenever used, the V_{BB} output pin should be bypassed to V_{CC} via a 0.01 µF capacitor.

To accomplish levels of translation, the EL91W requires three power rails, V_{CC}, V_{EE} and GND. Please refer to the Function Table below for more details. V_{CC} supply should be connected to the positive supply, and V_{EE} should be connected to the negative supply.

The GND pins are connected to the system ground plane. Both V_{CC} and V_{EE} pins should be bypassed to ground via a 0.01 µF capacitor. Under open input conditions, the D* input will be biased at $V_{CC}/2$, and the D input will be pulled to GND. This condition will force the Q output to low, ensuring stability.

Functional Block Diagram



Features

- Extended Supply Voltage Range (V_{EE} = –5.5V to –3.0V and V_{CC} = 3.0V to 5.5V)
- High Bandwidth Output Transition
- 620 ps Propagation Delay
- V_{BB} Output
- Internal Input Pulldown Resistors
- New Differential Input Common Mode Range
- Fully Compatible with MC100EL91 and MC100LVEL91
- ESD Protection of >4000V
- Industrial Temperature Range: –40°C to +85°C
- Available in 20 Pin SOIC Package

Pin Names

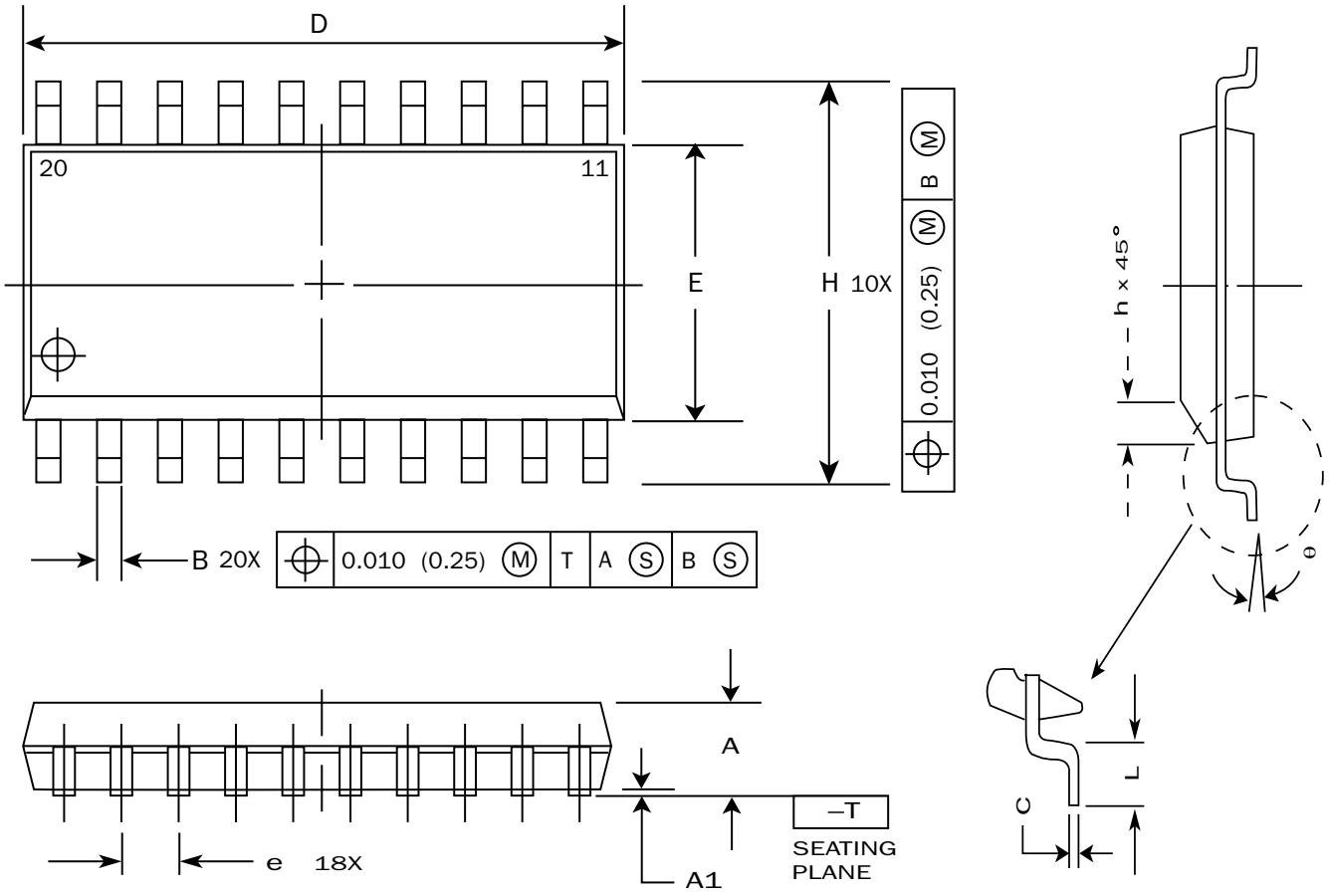
Pin	Function
Dn, Dn*	Differential PECL/LVPECL Inputs
Qn, Qn*	Differential ECL/LVECL Outputs
PECL_V_{BB}	PECL/LVPECL Reference Voltage Output

Function	VCC	VEE
LVPECL-to-ECL	3.3V	-5.0V
LVPECL-to-LVECL	3.3V	-3.3V
PECL-to-ECL	+5.0V	-5.0V
PECL-to-LVECL	+5.0V	-3.3V

Function Table

Package Information

20 Pin SOIC Package



DIM	Millimeters	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

NOTES:
1. Dimensions and tolerances per ASME Y14.5M, 1994.
2. Controlling dimension: millimeters.
3. Dimensions D and E do not include mold protrusion.
4. Maximum mold protrusion 0.15 per side.
5. Dimension B does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.13 total in excess of B dimension at maximum material condition.

DC Characteristics *(continued)*

SK10/100EL91W PECL/LVPECL Input DC Electrical Characteristics *(Notes 1, 2, 6)*

(V_{CC} = 3.0V to 5.5V; V_{EE} = –5.5V to –3.0V; VOUT loaded 50Ω to GND – 2.0V)

Symbol	Characteristic	TA = - 40 °C		TA = 0 °C		TA = + 25 °C		TA = + 85 °C		Unit	Condition
		Min	Max	Min	Max	Min	Max	Min	Max		
I_{IN}	Input Current	-150	150	-150	150	-150	150	-150	150	µA	
V_{IH}	Input HIGH Voltage 10EL	3770 2070	4110 2410	3830 2130	4160 2460	3870 2170	4190 2490	3940 2240	4280 2580	mV mV	V_{CC} = 5.0V V_{CC} = 3.3V
V_{IH}	Input HIGH Voltage 100EL	3835 2135	4120 2420	3835 2135	4120 2420	3835 2135	4120 2420	3835 2135	4120 2420	mV mV	V_{CC} = 5.0V V_{CC} = 3.3V
V_{IL}	Input LOW Voltage 10EL	3050 1350	3500 1800	3050 1350	3520 1820	3050 1350	3520 1820	3050 1350	3555 1855	mV mV	V_{CC} = 5.0V V_{CC} = 3.3V
V_{IL}	Input LOW Voltage 100EL	3190 1490	3525 1825	3190 1490	3525 1825	3190 1490	3525 1825	3190 1490	3525 1825	mV mV	V_{CC} = 5.0V V_{CC} = 3.3V
V_{BB}	Reference Output Voltage 10EL	3570 1870	3700 2000	3620 1920	3730 2030	3650 1950	3750 2050	3690 1990	3810 2110	mV mV	V_{CC} = 5.0V V_{CC} = 3.3V
V_{BB}	Reference Output Voltage 100EL	3620 1920	3740 2040	3620 1920	3740 2040	3620 1920	3740 2040	3620 1920	3740 2040	mV mV	V_{CC} = 5.0V V_{CC} = 3.3V
I_{CC}	Power Supply Current	3	10	3	10	3	10	3	10	mA	

SK10/100EL91W ECL/LVECL Output DC Electrical Characteristics *(Notes 1, 2)*

(V_{CC} = 3.0V to 5.5V; V_{EE} = –5.5V to –3.0V; VOUT loaded 50Ω to GND – 2.0V)

Symbol	Characteristic	TA = - 40 °C		TA = 0 °C		TA = + 25 °C		TA = + 85 °C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage 10 EL 100 EL	 –1080 –1085	 –890 –880	 –1020 –1025	 –840 –880	 –980 –1025	 –810 –880	 –910 –1025	 –720 –880	 mV mV
V_{OL}	Output LOW Voltage 10 EL 100 EL	 –1950 –1830	 –1650 –1555	 –1950 –1810	 –1630 –1620	 –1950 –1810	 –1630 –1620	 –1950 –1810	 –1595 –1620	 mV mV
I_{EE}	Power Supply Current 10 EL 100 EL	 16 16	 33 36	 16 16	 33 36	 16 16	 33 36	 16 16	 33 36	 mA mA

AC Characteristics

SK10/100EL91W AC Electrical Characteristics

(V_{CC} = 3.0V to 5.5V; V_{EE} = –5.5V to –3.0V; VOUT loaded 50Ω to GND – 2.0V)

Symbol	Characteristic	TA = - 40 °C		TA = 0 °C		TA = + 25 °C		TA = + 85 °C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{skew}	Output to Output Skew	21	32	21	32	21	32	21	32	ps
t_{PHL} t_{PLH}	Propagation Delay (Diff)[3]	440	666	460	717	471	742	492	786	ps
t_{PLH} t_{PHL}	Propagation Delay (SE)[3]	450	713	470	755	480	773	550	808	ps
t_r , t_f	Output Rise/Fall Times (20% to 80%)	287	597	287	597	287	597	287	597	ps
V_{CMR}	Common Mode Range[5]	GND + 1.2	V_{CC}	GND + 1.2	V_{CC}	GND + 1.2	V_{CC}	GND + 1.2	V_{CC}	V
V_{PP}	Minimum Peak-to-Peak Input[4]	150	1000	150	1000	150	1000	150	1000	mV

Notes:

1. 10EL circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to GND –2.0V.
2. 100K circuits are designed to meet the DC specification shown in the table where transverse airflow greater than 500 lfpm is maintained.
3. Duty cycle skew is the difference between T_{PLH} and T_{PHL} propagation delay through a device.
4. Minimum input swing for which parameters are guaranteed.
5. CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the high level falls within the specified range and the peak-to-peak voltage lies between $VPP_{(min)}$ and 1V. The lower end of the CMR range varies 1:1 with GND and is equal to GND + 1.2V.
6. For standard ECL DC specifications, refer to the ECL Logic Family Standard DC Specifications Data Sheet.
7. For ordering description, see HPP Part Ordering Information Data Sheet.

Ordering Information

Ordering Code	Package ID
SK10EL91WD	20-SOIC
SK10EL91WDT	20-SOIC
SK100EL91WD	20-SOIC
SK100EL91WDT	20-SOIC
SK10EL91WU	Die
SK100EL91WU	Die

Application Notes

AN1002 - Interfacing Between ECL / LVECL / PECL / LVPECL - to - TTL / LVTTL / CMOS / LVCMOS
AN1003 - Termination Techniques for ECL / LVECL / PECL / LVPECL Devices
AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL
AN1006 - Designing with 10K and 100K ECL / PECL Devices

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