TM4256FL8, TM4256GU8
262,144 BY 8-BIT DYNAMIC RAM MODULES

T-46-23-17

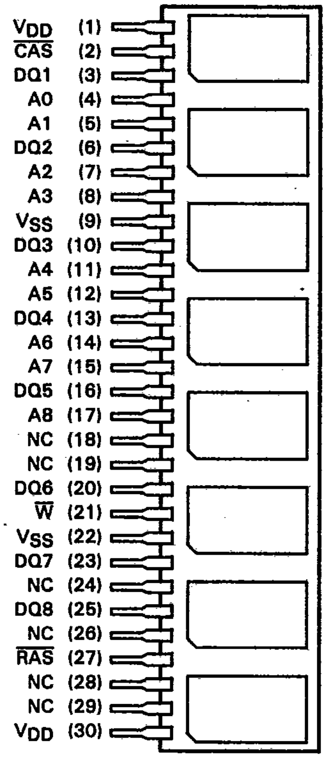
OCTOBER 1985—REVISED FEBRUARY 1988

- **262,144 × 8 Organization**
- **Single 5-V Supply (10% Tolerance)**
- **30-Pin Single-In-line Package (SIP)**
  - **—Pinned Module for Through-Hole Insertion (TM4256FL8)**
  - **—Leadless Module for Use with Sockets (TM4256GU8)**
- **Utilizes Eight 256K Dynamic RAMs in Plastic Chip Carrier**
- **Long Refresh Period . . . 4 ms (256 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Outputs**
- **Performance of Unmounted RAMs**

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TMS4256-10	100 ns	50 ns	200 ns
TMS4256-12	120 ns	60 ns	230 ns
TMS4256-15	150 ns	75 ns	260 ns

- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines**
- **Low Power Dissipation**
- **Operating Free-Air Temperature . . . 0°C to 70°C**

TM4256FL8 . . . L SINGLE-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE TM4256FL8	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ8	Data In/Data Out
NC	No Connection
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM4256__8 series are 2048K, dynamic random-access memory modules organized as 262,144 × 8 bits in a 30-pin single-in-line package comprising eight TMS4256FML, 262,144 × 1 bit dynamic RAMs in 18-lead plastic chip carriers mounted on top of a substrate together with decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.3 inch board spacing, the TM4256__8 has a density of ten devices per square inch (approximately 4 × the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated through-holes, a cost savings can be realized.

Each TMS4256FML is described in its data sheet and is fully electrically tested and processed according to TI MIL-STD-883B flows (as amended for commercial applications) prior to assembly. After assembly onto the SIP, a further set of electrical tests is performed.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

The TM4256__8 features $\overline{\text{RAS}}$ access times of 100 ns, 120 ns, and 150 ns maximum.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{\text{RAS}}$ in order to retain data. $\overline{\text{CAS}}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM4256__8 is rated for operation from 0°C to 70°C.

presence detect

This feature is included on the TM4256GU8 to allow for hardware presence detection of the memory module. The $\overline{\text{PRD}}$ pin for each module in the system should be pulled high through a pull-up resistor, resulting in a logic one when no module is present. When a module is present, $\overline{\text{PRD}}$ is a logic zero as this pin is connected to V_{SS} on the module. $\overline{\text{PRD}}$ can be used only to detect a module's presence, not its functionality. In a system not requiring presence detect, it is recommended that this pin be left as a no connect; this allows the use of either type of module without adverse effects.

operation

The TM4256FL8 and TM4256GU8 operate as eight TMS4256FMLs connected as shown in the functional block diagram. Refer to the TMS4256 data sheet for details of operation.

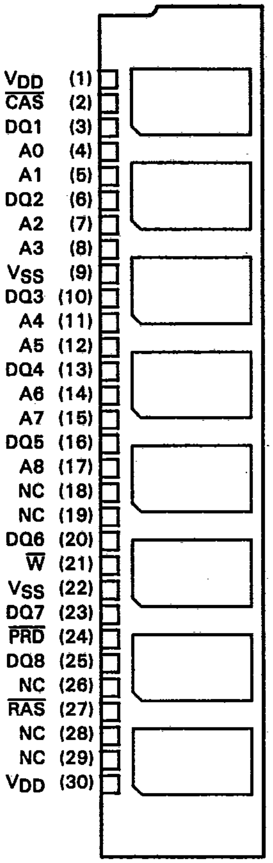
specifications

For TMS4256FML electrical specifications, refer to the TMS4256 data sheet.

single-in-line package and components

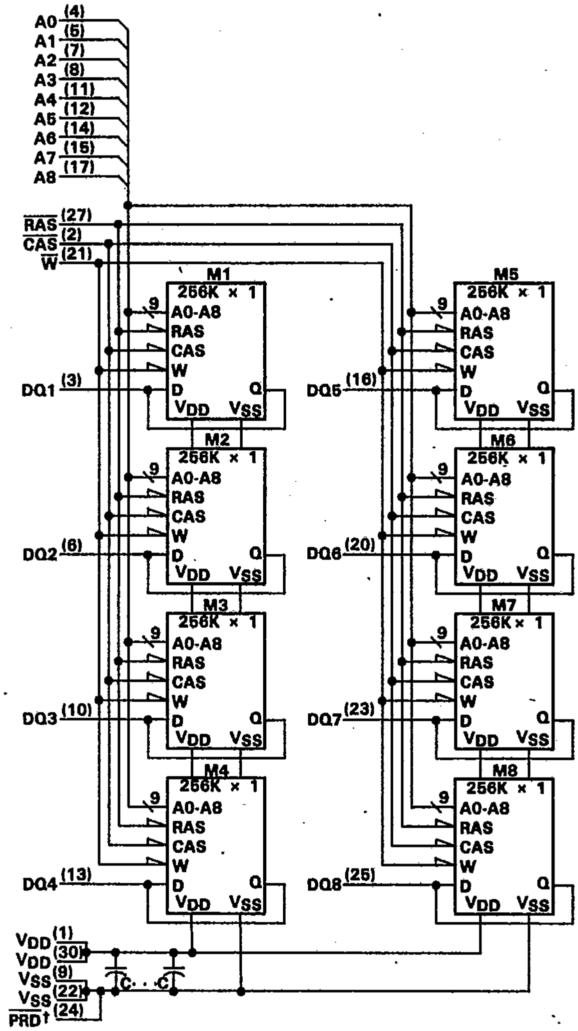
PC substrate: 1,27 mm (0.05 inch) nominal thickness epoxy-glass
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze
Contact area for socketable devices: Nickel plate and solder plate on top of copper

TM4256GU8 . . . U SINGLE-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE TM4256GU8	
A0-A8	Address Inputs
$\overline{\text{CAS}}$	Column-Address Strobe
DQ1-DQ8	Data In/Data Out
NC	No Connection
$\overline{\text{PRD}}$	Presence Detect (V_{SS})
$\overline{\text{RAS}}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{\text{W}}$	Write Enable

functional block diagram



†Not available on the TM4256FL8.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin including V_{DD} supply (see Note 1) .... −1 V to 7 V
Short circuit output current for any output .... 50 mA
Power dissipation .... 8 W
Operating free-air temperature range .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM4256__8-10		TM4256__8-12		UNIT
			MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4	V_{DD}	2.4	V_{DD}	V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA	0	0.4	0	0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V		±10		±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high		±10		±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle All outputs open		560		520	mA
I_{DD2}‡	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		36		36	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		464		424	mA
I_{DD4}‡	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		400		360	mA

‡I_{DD1}-I_{DD4} are measured with M1-M8 in the same mode (i.e., operating, standby, refresh, page mode).

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM4256__8-15		UNIT
			MIN	MAX	
V_{OH}	High-level output voltage	$I_{OH} = -5$ mA	2.4	V_{DD}	V
V_{OL}	Low-level output voltage	$I_{OL} = 4.2$ mA	0	0.4	V
I_I	Input current (leakage)	$V_I = 0$ V to 6.5 V, $V_{DD} = 5$ V, All other pins = 0 V		±10	μA
I_O	Output current (leakage)	$V_O = 0.4$ V to 5.5 V, $V_{DD} = 5$ V, $\overline{CAS}$ high		±10	μA
I_{DD1}[†]	Average operating current during read or write cycle	t_c = minimum cycle All outputs open		480	mA
I_{DD2}[†]	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		36	mA
I_{DD3}[†]	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		384	mA
I_{DD4}[†]	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		320	mA

[†] I_{DD1}-I_{DD4} are measured with M1-M8 in the same mode (i.e., operating, standby, refresh, page mode).

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		40	pF
$C_{i(DQ)}$	Input capacitance, data inputs		12	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ input		40	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		56	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ input		40	pF
$C_{o(VDD)}$	Decoupling capacitance	0.8		μF

Designing and Manufacturing Surface Mount Assemblies

T-90-20

Elizabeth Gunther, Charles Hutchins, and Paul Peterson

The competitive nature of the semiconductor industry has driven vendors to minimize the size of electronic components, so that more functions can be achieved in a given volume. In addition, improved electrical performance, decreased mass, and the potential for lower system cost are all by-products of compacted packaging and circuitry which hold interest to component manufacturers and users alike.

Surface Mount Technology (SMT) offers an excellent method of reducing component size. A typical memory array can be reduced to 50 percent of its original PWB size with single-sided mounting, and 25 to 30 percent with double-sided mounting. Logic designs cannot achieve the same dramatic reduction, but decreases up to 40 to 60 percent can be achieved for single-sided and double-sided assemblies respectively.

The key design and manufacturing process issues must be understood in order to fully reap the benefits of Surface Mount Technology. This article gives a general overview of the key aspects of design, process, and manufacturing of surface mounted assemblies, and offers surface mount as an opportunity to lower a system's cost without sacrificing reliability.

Components

Most surface mount components are at least one-third the size of the comparable through-hole mounted device (Figure 1). The 68-pin chip carrier is approxmiately one square inch, while the 64-pin DIP is approximately three square inches. The 20-pin chip carrier is slightly larger than 0.1 square inch, while the 20-pin DIP is 0.3 square inch. Similarly, other IC packages are reduced to approximately one-third the size of comparable lead count packages. The passive components occupy approximately one-tenth the board area, and this is why they have been used in most small consumer products built in the last couple of years.

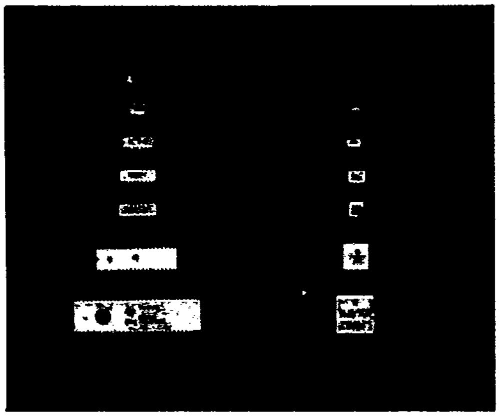


Figure 1. Component Site Reduction

There were many references in the recent past to problems with component availability, cost, and standardization. This area of SMT has probably received more attention than any other. Several recent magazine articles now state that significantly more components (particularly actives) are now available and that cost parity has been achieved on most of them. The effort by various industry committees on standardization has also been effective.

Thus, although more needs to be accomplished in these areas, a designer can begin a project with confidence that there will be no insurmountable barriers in this area. There are several consultants and subcontract assembly companies to assist in this effort. It is strongly recommended that all new designs utilize some form of SMT, particularly when space is an important consideration.

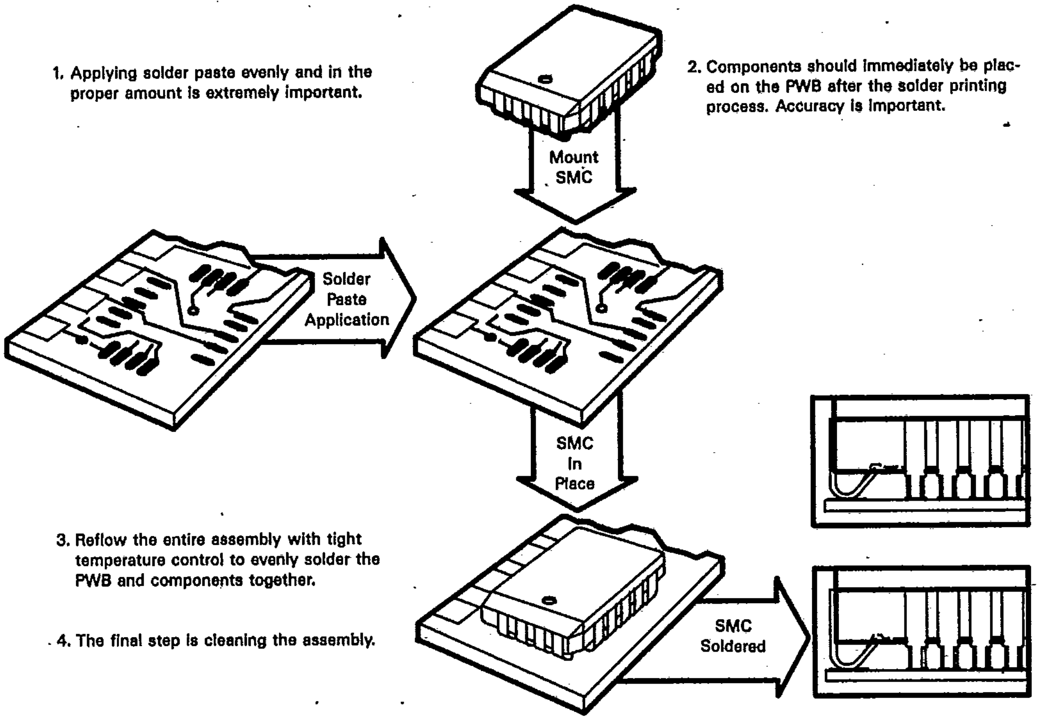
Process

The process to manufacture a surface mount assembly (SMA) is very simple. It consists of four basic steps, as shown in Figure 2. First, the solder paste is screened on the PWB. Then the component is placed on the board, with due care to get it positioned correctly. Typical geometries require placement accuracy of less than plus/minus 4 mils. Next the solder is reflowed with either a vapor phase or infrared system. Finally, the assembly is cleaned and is now ready for test. This process, although simple in concept, relies on board and component planarity and solderability. These are easily achievable with the chip carriers and memory modules we will discuss later.

Texas Instruments has installed a Surface Mount Technology Center at its plant in Houston, Texas. At this center, we have a complete and flexible engineering line to assist our customers in converting to Surface Mount Technology.

The engineering line is equipped with a screen printer, pick and place system, vapor phase reflow, and clean-up station that will easily handle PWBs up to 9″ × 10″. Larger boards up to 14″ × 16″ can be processed with some additional care. TI uses this engineering line to produce its prototype and demo boards. It is also available to any of TI's customers, free of charge, for use in building test or prototype boards.

The effectiveness of the assembly process can be characterized by the number of unacceptable solder joints formed during the process. Unacceptable joints are defined by their electrical and mechanical (strength and reliability) characteristics. The major problem is open solder joints, followed by bridging and misregistration.



1. Applying solder paste evenly and in the proper amount is extremely important.
2. Components should immediately be placed on the PWB after the solder printing process. Accuracy is important.
3. Reflow the entire assembly with tight temperature control to evenly solder the PWB and components together.
4. The final step is cleaning the assembly.

Figure 2. Basic Process Steps

Open circuits are detected at electrical test and are the first defects detected after soldering. At Texas Instruments, 10 PPM or less is the desirable defect level. Several factors that contribute to open solder joints were identified during production start-up. Lead tip planarity of the J-leaded plastic chip carriers is the most important factor in obtaining acceptable process yields. Lead position, lead finish, solder paste composition, and PWB solderability affect process yield as well.

Experiments in which lead tip planarity was confined to specific limits between 1 to 7 mils indicate that a 2 mil planarity requirement produces acceptable results with the process currently in use. Little gain in yield was noted at a 1 mil planarity requirement.

Another interesting result showed that silver in the process, either as a lead finish or in the solder paste, improves yields significantly. One explanation may have to do with the dynamics of the solder during the reflow process as they are affected by the different surface forces acting in the silver and non-silver process.

Design

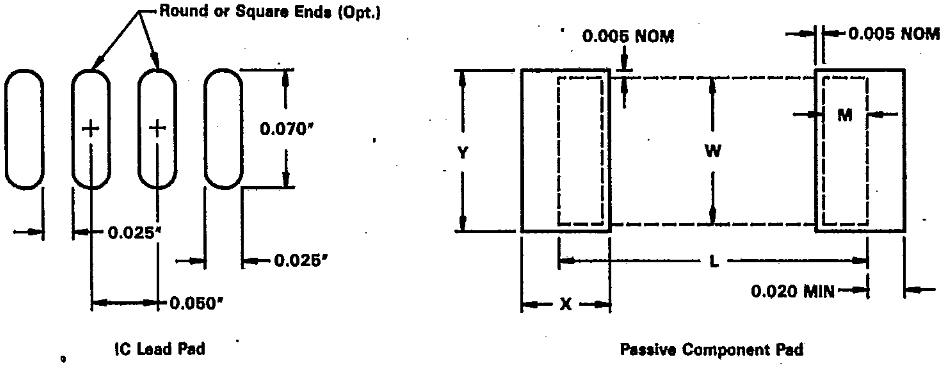
The design of the PWB, in addition to providing the component interconnections, will provide the proper amount and correct placement of solder paste for a strong fillet formation. The wave soldering process, by comparison, provides a semi-infinite amount of solder, whereas the SMT process will provide only a predetermined amount. Thus, the component connection pad must be correctly placed and be of the proper size.

Further, consideration must be given for inspection, testing, and rework. The density achievable can lead to severe problems at these points if understanding and due care are not exercised in the design. The project team should include members from manufacturing, testing, QA, and purchasing, in addition to the design engineers, from the start. The design and processing of test boards is strongly recommended to provide experience and direction for the major project.

A very practical set of design guidelines is given in Figure 3. These have been used on a number of SMT designs and have given good results. With proper manufacturing techniques as described later, a high yield can be achieved. Component spacings should be approximately equal to the height of the tallest component. This allows an angle of 45 degrees for visual inspection of test probes.

Figure 4 shows the standard footprint for all Small Outline (SO) packages. The larger and more important fillet of an SO package is on the inside of the gull-wing lead. The solder pad, or land, should therefore be designed to extend slightly under the body of the package in order to optimize this fillet. From Table 1 we can see all packages have 50 mil centers with 25 mil spacings between lands. This allows the designer enough space to put traces between pads, and also reduces the occurrence of solder bridging of adjacent lands. Table 1 also summarizes the suggested land lengths and placement, depending on the terminal count of the SO. While not an absolute solution, these land sizes offer a conservative design solution that will meet most vendors' specifications and provide a mechanically and electrically sound solder joint.

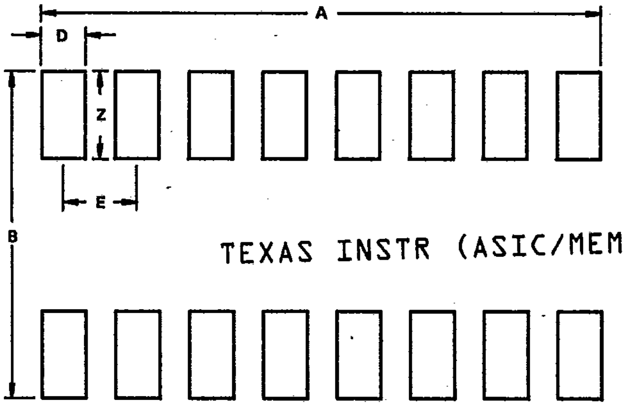
● Geometries	
• Trace Width/Space	**8/8 MIL Min., 10/10 MIL Typ.**
• IC Lead Solder Pad Size	**25 ± 5 MIL × 70 ± 10 MIL**
• Via Hole Size	**20 MIL DIA**
• Via Pad Size	**40 MIL DIA**
• Cap/Resistor Pad Size	**W = MAX Dimensions of Component** **L = 20 MIL Beyond Metallization** **10 MIL Inside Metallization**
• Solder Mask	**5 MIL Larger than IC/Component Pad**



IC Lead Pad

Passive Component Pad

Figure 3. PWB Design Guidelines



TEXAS INSTR (ASIC/MEMORY) 25E D

Figure 4. Standard SOIC Footprint

Table 1. SOIC Footprint Dimensions

No. of Terminals	A	B	Z	D	E
8	.175	.250	.050	.025	.050
14	.325	.250	.050	.025	.050
16	.375	.250	.050	.025	.050
20	.475	.430	.070	.025	.050
24	.575	.430	.070	.025	.050

Test	4164A PLCC	4164 DIP	Units
Life Test, 125°C	42	64	Fits*—60% UCL
85°C/85% RH	0.17	0.37	%/1000 Hours
Autoclave	0.17	0.96	%/240 Hours
T/C−65/150	0.52	1.44	%/1000 Cycles
T/C 0/125	0.0	0.0	%/2000 Cycles

*Derated to 55°C Assuming 0.5EV Activation Energy

Figure 5. Failure Rate Comparison
4164A PLCC VS DIP

Manufacturing

The SMT manufacturing area must have the following basic equipment:

- Solder Paste Printer
- Component Pick and Place Machine
- Solder Paste Reflow Machine
- Clean-up System
- Inspection/Process Control Aids
- Electrical Test

The criteria for choosing the above is determined mainly by the size(s) and quantity of PWBs per month, the gross number of components per PWB, and the number of different components per PWB.

The size of the largest PWB is an important criterion in the choice of all of the major items. The printer, pick and place, reflow, and clean-up must all be able to handle it with no difficulty or process nonuniformity. The number and size of the various PWBs that may be produced will secondarily be considered for ease of set up and changeover in the printer and pick and place. The pick and place machine(s) will probably be the most expensive item in the list above and therefore, should get the most attention.

The gross number of components and PWBs will provide data for choosing the pick and place. Component per hour placement speed should be checked in actual operation, as the interrelationship may affect ultimate speed. The number of different components per board will determine how many feeders and what types of feeders will be required. This is a very key issue, as well as the accuracy of placement.

Reflow

The solder reflow is easily achieved with any of the commercially available equipment. Subtle differences between vapor phase, either batch or in-line, and infrared are overshadowed by the choice of solder paste and the solderability/planarity issue. A batch vapor phase is extremely flexible for different sizes of boards with different component counts. The in-line vapor phase is a good choice for a more automated processing line with standard or similar sized boards. The infrared has the advantage of being less expensive to operate, but requires more alteration to set up the time-temperature profile for a different size PWB. This would be a minimal problem on a manufacturing line building high volumes of the same board.

Clean-up

The most popular flux for SMT is the mildly activated rosin flux (RMA). This was developed in the days of vacuum tube assembly when clean-up was next to impossible. It is noncorrosive but provides sufficient fluxing action for good quality components and PWBs. Thus it is the preferred choice for SMAs with small spacings under most passives and SOICs, where complete cleaning is difficult. A mild solvent, such as Freon TMS, is generally sufficient to achieve a good visual cleanup, and there are several systems available that provide hot vapor, spray, or ultrasonic de-fluxing.

Reliability

With the smaller surface mount packages, there is some concern about component reliability. Texas Instruments addressed the overall DRAM reliability issue several years ago. Through an extensive task force effort, the major problems of the life test, humidity performance, and temperature cycle were identified. The best solutions to these problems required several changes in the design and process of the silicon chip. In doing so, the reliability of the DRAM chip became independent of the package used. Thus, the 64K DRAM in the plastic chip carrier package performs equivalently to the same chip in a DIP as shown in Figure 5. Similar data is available on most semiconductor ICs.

An additional reliability concern originates in the surface mount solder reflow process, which submits components to higher reflow temperatures more suddenly than the wave-soldering methods of DIP components, with oftentimes repeated reflow cycles for rework and repair.

The best method for resolving this issue involves comparing the temperature-time differential of the vapor phase or infrared solder reflow process to the standard temperature cycling reliability tests to which surface mount components are routinely submitted. Figures 6 and 7 show temperature profiles of the vapor phase and infrared solder reflow processes. In the vapor phase process, the maximum temperature change with time is:

$$\frac{215^\circ C - 25^\circ C}{45\ \text{sec}} = \frac{190^\circ C}{45\ \text{sec}}$$

equaling approximately 4°C/sec. The infrared solder reflow method submits the ICs to a similar, yet less severe temperature over time change of 3°C/second. Comparing these temperature profile ramp-ups to that which a surface mount component undergoes in a temperature cycling reliability test proves that there should be no concern over damage to the component during reflow. In the temp cycling test, the surface mount components were submitted to 1000 cycles of sudden cycling from 150°C to −65°C within three seconds. This represents a temperature-time differential of:

$$\frac{150^\circ C-(-65^\circ C)}{3} = \frac{215^\circ C}{3\ \text{sec}} = \frac{70^\circ C}{\text{sec}}$$

with less than 0.5 percent failures.

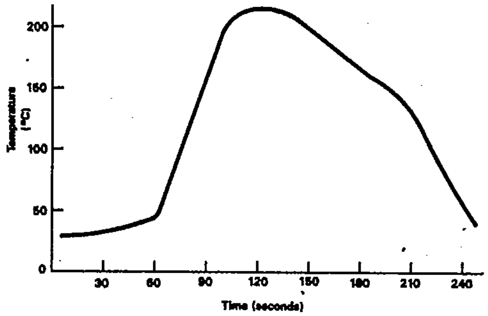


Figure 6. Typical Temperature Profile for In-Line Vapor Phase Reflow

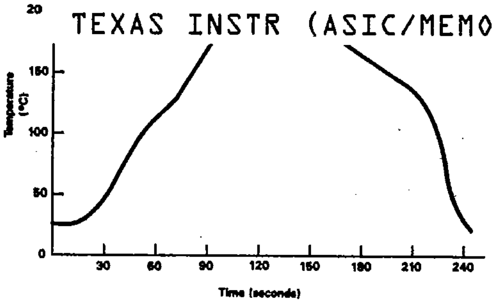


Figure 7. Typical IR Reflow System Profile

Since the surface mounted components were able to withstand a 70°C/second temperature change of 1000 cycles, they should be able to withstand the less severe conditions of a 4°C/second damage during reflow without reliability degradation.

Another concern in the solder reflow processing of surface mount components is the dwell time in reflow temperatures of 215°C or above. The dwell time for a small PWB populated with surface mount devices is about 20 seconds. For a larger board of about 10″×12″ up to 50 seconds is needed for reflow. A generalized component degradation curve, relating accumulated time and temperature, can be assumed to exist. The shape of the curve for this discussion is assumed to be a decaying parabolic for simplicity and conservatism. There are two generally known points of this curve. The flame retardant mold compound (FRMC) of a plastic package starts to break down at 300°C in two to three seconds. Also, the molding and curing of a surface mount device is performed over several hours at 175°C. These two points are shown on the generalized curve shown in Figure 8, with the "safe" region being the area under the curve. Two points that fall within this region are the industry standard practice of solder dipping leads of several types of ICs, and of the soldering plastic devices on the bottom with Type III surface mount assembly, each submerges the component for three to four seconds in a solder wave.

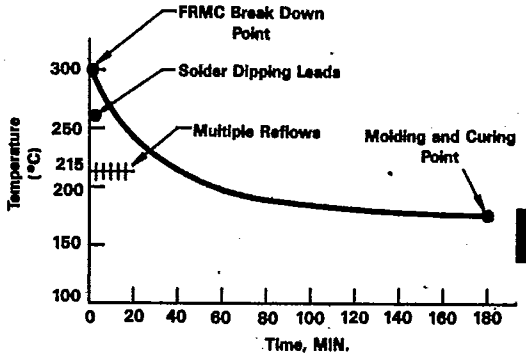


Figure 8. General Plastic Degradation Curve

Summary

Surface mount assembly techniques provide a significant advantage in cost, volume, and reliability over the current "thru-hole" technology. These are well documented, and the manufacturing equipment and related products are becoming readily available to support new production lines. Also, as experience grows, improved products and ideas are developed from the cooperative efforts of vendors and users in standardization organizations and in problem-solving sessions. The broad selection of package types and product technologies available now are sufficient to begin conversion of existing electronic system products for size reduction or feature enhancement. Definitely, new products should be designed with surface mount technology.