5/10

3539 Static RAMs

256 X 8 N-MOS TTL In/Out

Features

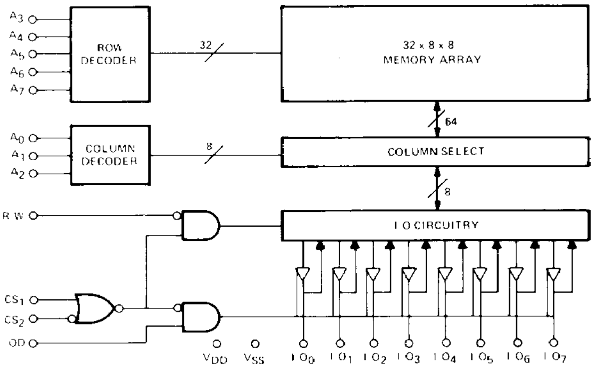
- 256 words X 8 bits
- 500 nSec maximum access time
- Less that 400 mW power (Standard device)
- Less than 210 mW power (Low Power device)
- Single +5V power supply
- Two separate Chip Select inputs
- Separate Output Disable function
- Ideal replacement for 2111 and 2112 RAMs
- Fully compatible with all GTE byte-wide RAMs

TS per IC Mstr

General Description

The GTE 3539 Static RAM is a 2048-bit (256 X 8) memory device with a maximum access time of 400 nanoseconds. The 3539 is ideally suited for byte-oriented small memory applications and as a functional replacement for 2111 and 2112 Static RAMs. Complimentary Chip Select (CS and $\overline{CS}$) inputs are provided, in addition to a separate Output Disable ($\overline{OD}$) function which allows gating output data onto the I/O bus on command. An 8-bit common I/O bus allows convenient interfacing to byte-wide design applications. The 3539 is available in 400 and 500 nanoseconds access times, and a choice of Standard (400 mW max.) or Low Power (210 mW max.) configurations. The 3539 is available in a standard 22-pin plastic or cerdip package.

Block Diagram



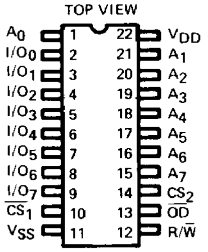
Truth Table

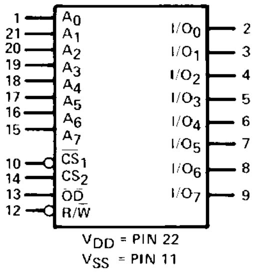
$\overline{CS_1}$	CS_2	$\overline{OD}$	$R/\overline{W}$	STATUS	I/O BUS MODE
H	X	X	X	DESELECTED	HI Z
X	L	X	X	DESELECTED	HI Z
L	H	L	L	WRITE MODE	OUTPUT DISABLED DATA CAN BE WRITTEN
L	H	H	L	WRITE MODE	OUTPUT ENABLED DATA CAN NOT BE WRITTEN
L	H	L	H	READ MODE	OUTPUT DISABLED DATA CAN NOT BE READ
L	H	H	H	READ MODE	OUTPUT ENABLED DATA CAN BE READ

X · IRRELEVENT STATE

Pin Configuration and Logic Symbol

A_n	Address Inputs
CS_n	Chip Select Inputs
$\overline{OD}$	Output Disable
$R/\overline{W}$	Read/Write Control Input
I/O_n	Data Bus Pins
V_{DD}	+5 V Power Supply
V_{SS}	0 V Power Supply





Specifications

	Max. Access Time (nSec)	Max. Cycle Time (nSec)	Max. I_{DD} Supply Current (mA)
3539-1	400	400	75
L3539-1	400	400	40
3539-2	500	500	75
L3539-2	500	500	40

Microcircuits 5-39 ORIG

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T-2551 GTE

Recommended Operating Conditions (T_{AMB} = 0°C to +70°C)

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Input High Level	V_{IH}	2.4	–	V_{DD}	V
Input Low Level	V_{IL}	-0.5	–	0.8	V

DC Characteristics (Full Operating Voltage & Temperature Range Unless Otherwise Noted)

PARAMETER	SYMBOL	MIN	MAX	UNITS	CONDITIONS
Input HIGH Voltage	V_{IH}	2.2	–	V	
Input LOW Voltage	V_{IL}	–	0.65	V	
Output HIGH Voltage	V_{OH}	2.2	–	V	$I_{OH} = -100\,\mu A$
Output LOW Voltage	V_{OL}	–	0.4	V	I_{OL} = 1.6 mA
Bus HIGH Current	I_{BH}	–	10	μA	$V_{IN} = V_{DD}$, Chip Deselected
Bus LOW Current	I_{BL}	–	-10	μA	V_{IN} = .4 V, Chip Deselected
Input Leakage Current	I_{LI}	-10	10	μA	$V_{SS} \leqslant V_{IN} \leqslant V_{DD}$ (All Inputs Except Data In)
Power Supply Current 3539-1,2	I_{DD}	–	75	mA	V_{DD} = 5.25 V
Power Supply Current L3539-1,2	I_{DD}	–	40	mA	V_{DD} = 5.25 V

Read Cycle — AC Characteristics (Full Operating Voltage and Temperature Range)

CHARACTERISTICS	SYMBOL	3539-1/L3539-1		3539-2/L3539-2		UNITS
		MIN	MAX	MIN	MAX	
Access Time	T_A	–	400	–	500	nS
Cycle Time	T_C	400	–	500	–	nS
Chip Select Delay Time	T_{CD}	–	100	–	100	nS
Output Enable Time	T_{OE}	–	200	–	225	nS
Output Disable Time	T_{OD}	–	150	–	150	nS

Write Cycle — AC Characteristics (Full Operating Voltage and Temperature Range)

CHARACTERISTICS	SYMBOL	3539-1/L3539-1		3539-2/L3539-2		UNITS
		MIN	MAX	MIN	MAX	
Cycle Time*	T_C	400	–	500	–	nS
Address to Write Delay Time	T_{AW}	25	–	25	–	nS
Data Set-Up Time	T_{DS}	200	–	250	–	nS
Data Hold Time	T_{DH}	0	–	0	–	nS
Write Recovery Time	T_{WR}	25	–	25	–	nS
Write Pulse Width	T_{WW}	150	–	175	–	nS
Chip Select to Write Set Up Time	T_{CSW}	125	–	150	–	nS
Chip Select Delay Time	T_{CD}	–	100	–	100	nS
Chip Select to Write Hold Time	T_{CH}	0	–	0	–	nS
Output Disable Time	T_{OD}	–	150	–	150	nS

*$T_C = (T_{AW} + T_{WW} + T_{WR})$ or $(T_{OD} + T_{DS})$, whichever is relevant.

Capacitance

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Input Capacitance	C_{IN}	–	–	5	pF	V_{IN} = 2.4V
Output Capacitance	C_{OUT}	–	–	10	pF	

Absolute Maximum Ratings

(See Note 1) (Referenced to Gnd)

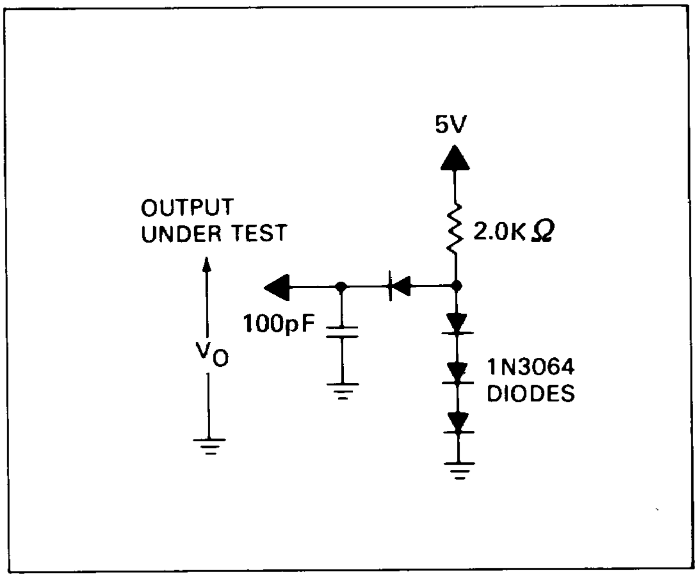
RATING	VALUE	UNIT
Voltage On Any Pin With Respect To GND	−0.5 to +7	VDC
Power Dissipation	1.6 (Note 2)	W
Operating Ambient Temperature Range	0 to +70	°C
Storage Temperature	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages.

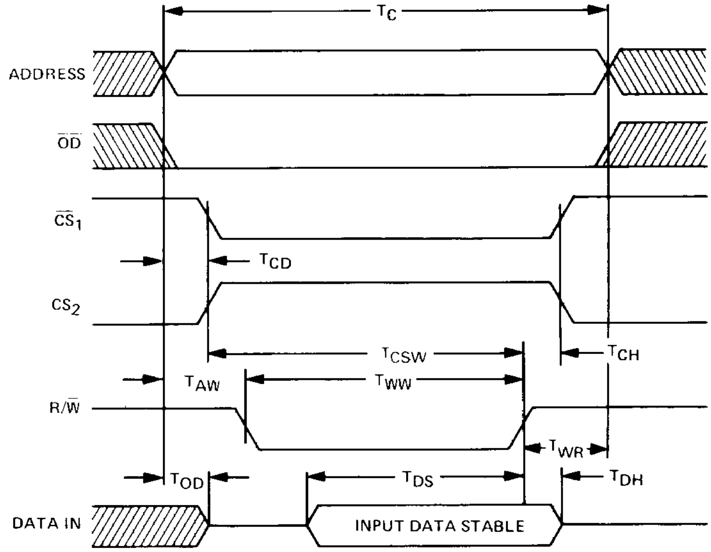
NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended or maximum voltages for extended periods of time could affect device reliability.

NOTE 2: At 25°C Ambient. Derate 13.5 mw/ C.

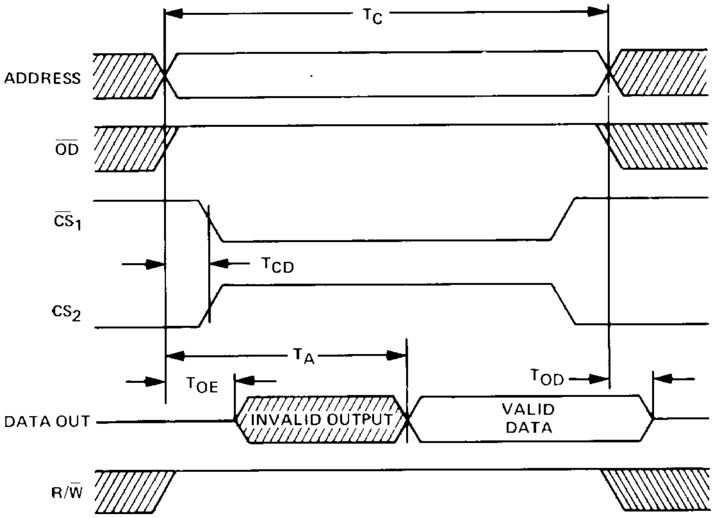
Test Output Load



Write Cycle



Read Cycle



Functional Description:

The GTE 3539 uses a multiplexed Input/Output (I/O) structure, allowing the device to be packaged in a 22-pin DIP. The I/O network is controlled by the Read/$\overline{\text{Write}}$ ($R/\overline{W}$), Output Disable ($\overline{OD}$), and two Chip Select ($\overline{CS}_1$ and CS_2) inputs.

The I/O network is in a high impedance state and the $R/\overline{W}$ input disabled whenever $\overline{CS}_1$ is HIGH or CS_2 is LOW. When $\overline{CS}_1$ is LOW and CS_2 is HIGH the circuit will read or write, depending on the $\overline{OD}$ and $R/\overline{W}$ inputs.

When $\overline{OD}$ is HIGH, the eight I/O pins are in the Output mode, so that the $R/\overline{W}$ input should be HIGH to force the chip into a read mode. However, when $R/\overline{W}$ is HIGH, the $\overline{OD}$ can be used as a chip select input, turning the outputs off when it goes LOW.

When the $R/\overline{W}$ and $\overline{CS}_1$ are LOW and CS_2 is HIGH, the circuit is in the write mode. $\overline{OD}$ must be LOW to turn off the output structures. Data is then entered from the I/O pins. The $\overline{OD}$ is used to turn off the output structures independent of the Chip Select, allowing input data to be entered at the I/O ports sooner than if the I/O were controlled by $R/\overline{W}$. Output data is not inverted by the 3539. The output buffers will each drive one standard TTL load +100pF.

The eight address inputs specify which location of the memory array will be selected for the read or write operations. Each control, address and I/O input is directly TTL-compatible.