Contents

The S-7040D decoder IC has been designed in accordance with the CCIR* Radio Paging Code Number 1 (POCSAG** code). The S-7040D can be used for display pager since It processes the POCSAG signal internally and sends the decoded data to an external microprocessor. Furthermore the S-7040D can also be used for tone-only pager without a microprocessor. Eight kinds of paging tone cadences are generated for valid pagings to make the user know which information is received. The S-7040D has a battery saving function which drives signal receiving circuit intermittently.

* CCIR: International Radio Consultative Committee

** POCSAG: Post Office Code Standardization Advisory Group

■ Features

- Operating voltage : 1.7 to 3.6 V (3.0 V typ.)
- Current consumption : 50 μA max. (3.0 V)
- Data rate :512/1200 bps selectable (76kHz crystal)
  512bps (32kHz crystal)
- User address : 4 (2addresses/frame)
- User frame : 2
- Four cadences per an address
- External elements:
  Crystal oscillator (32 KHz/76 KHz), C_G, R_F
- Direct interface to IDROM (S-29131A / S-2913)
- 3 paging signals : Tone, LED, Vibrator
- CPU direct interface
  CPU control output and reference clock output for CPU (32 KHz or 76 KHz)

■ Functions

- Power on clearing
- BCH correction up to 2 bits
- Battery saving
- Battery low alert
- Extended function

■ Dimensions

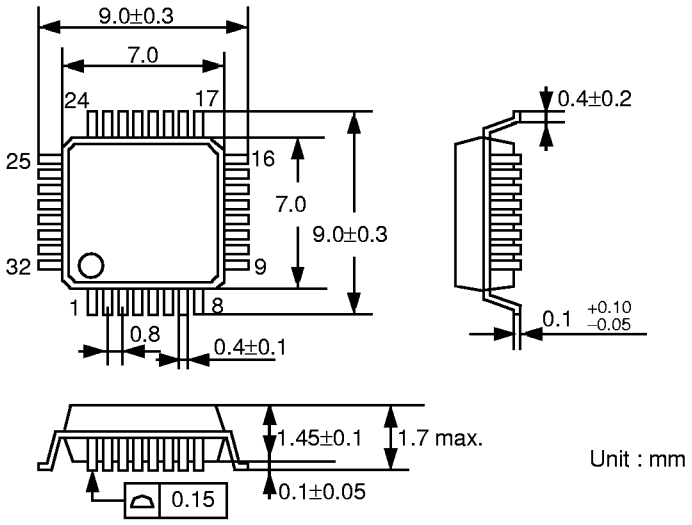


Figure 1

■ Block Diagram

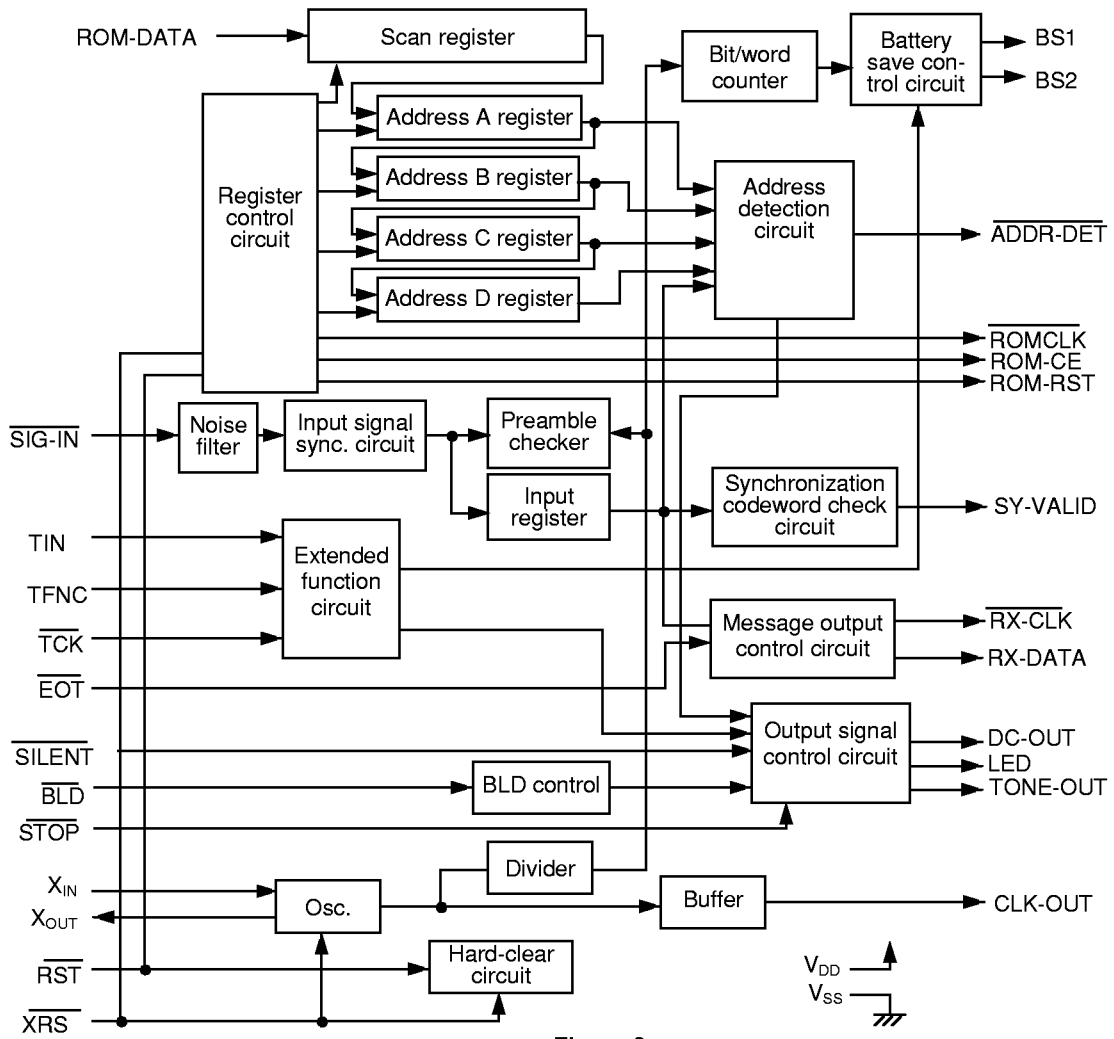


Figure 2

■ Pin Configuration

32-pin QFP

Top view

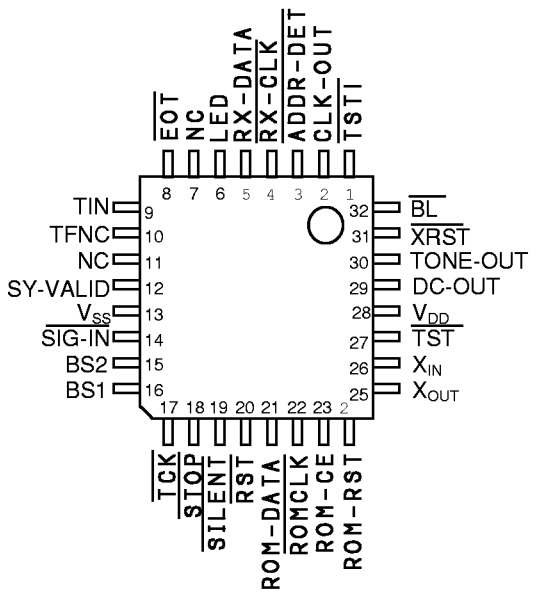


Figure 3

■ Pin Description

Table 1

Pin#	Name	In/Out	Description	Reset	Pull-up
1	$\overline{\text{TST1}}$	In	Test mode set pin. Ordinarily "H" or "OPEN".		O
2	CLK-OUT	Out	System clock output pin. Clock of oscillation circuit is buffered and transmitted.		
3	$\overline{\text{ADDR-DET}}$	Out	This pin will go "L" when programmed address is detected and will go "H" after output of received data.	H	
4	$\overline{\text{RX-CLK}}$	Out	Timing clock for received data output. Serial output of received data is enabled in synchronous to falling edge of the clock.	H	
5	RX-DATA	Out	Output pin for received data.	L	
6	LED	Out	Timing signal output pin for LED driving.	L	
7	—	—	Not connected (NC)	—	—
8	$\overline{\text{EOT}}$	In	This pin finishes message reception. A pulse signal input to this pin terminates reception forcibly.		O
9	TIN	In	Extended data input pin.		O
10	TFNC	In	Input pin for extended mode selection.		O
11	—	—	Not connected (NC)	—	—
12	SY-VALID	Out	This pin will go "H" when sync-code is detected and will go back "L" when the detection is failed. "H" is held during retry. This pin indicates that message reception is possible.	L	
13	V_{SS}	—	Negative power supply terminal.	—	—
14	$\overline{\text{SIG-IN}}$	In	Input pin for serial data (NRZ signal) from RF circuit (logic inversion is enabled by register). This pin has noise reduction circuit. Duty cycle of 25 to 75% is required.		
15	BS2	Out	Output pin for quick charge signal to RF circuit reference voltage.	L	
16	BS1	Out	Output pin for control signal of RF circuit power supply.	L	
17	$\overline{\text{TCK}}$	In	Extended clock input pin.		O
18	$\overline{\text{STOP}}$	In	External control to this pin inhibits TONE-OUT and LED output.		O
19	$\overline{\text{SILENT}}$	In	LED or vibrator is selected for call device when this pin is set "L" while TONE-OUT output for call is suppressed.		O
20	$\overline{\text{RST}}$	In	Input pin for reset with pull-up. Power on clear is enabled by attaching a condenser.		O
21	ROM-DATA	In	Input pin for IDROM data.		
22	$\overline{\text{ROMCLK}}$	Out	Output pin for IDROM synchronization clock.	Z	
23	ROM-CE	Out	Output pin for IDROM chip enable.	PL	
24	ROM-RST	Out	Output pin for IDROM reset.	Z	
25	X_{OUT}	Out	Output pin for crystal oscillator.		
26	X_{IN}	In	Input pin for crystal oscillator.		
27	$\overline{\text{TST2}}$	In	Input pin for test. Ordinarily "H" or "OPEN".		O
28	V_{DD}	—	Positive power supply terminal.	—	—
29	DC-OUT	Out	Timing signal output pin for vibrator control.	L	
30	TONE-OUT	Out	Output pin for paging tone. Tone frequencies are 2.7 KHz /3.2 KHz.	L	
31	$\overline{\text{XRST}}$	In	Input pin for oscillation control. "H" to this pin enables oscillation. "L" disables oscillation and resets the internal circuit. IDROM data is fetched after recovery. Connect to V_{DD} when the pin is not used. No pull-up.		
32	BLD	In	This pin samples detection signal for voltage lowering of battery. Two continual detection of "L" leads to BLD tone output.		

Note
1. Reset means the state of each pin when $\overline{\text{RST}}$="L". Z stands for high impedance and PL for pull-down.
2. "O" in pull-up column means that the pin is pulled up to V_{DD}.

■ Electrical Characteristics

Table 2

(V_{DD} = 3.0V, V_{SS} = 0V, Ta = 25°C unless otherwise specified.)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Circuit	Note
Operating voltage	V_{DD}	Ta=-10°C~+70°C		1.7	3.0	3.6	V	①	1
Oscillation start voltage	V_{DOB}	Ta=-10°C~+70°C		2.0	—	3.6	V	①	2
Total average standby current consumption	I_N	f_O=32768 Hz	V_{DD}= 1.7 V	—	4	15	µA	①	3
			V_{DD}=3.0 V	—	20	40			
		f_O=76800 Hz	VDD= 1.7 V	—	5	20			
			V_{DD}=3.0 V	—	25	50			
Total leakage current	I_S	V_{DD}= 3.0 V		—	0.1	1.0	µA		—
TONE-OUT/LED output current	I_{OH1}	V_{DD}= 1.9 V, V_{OH}= 1.6 V		—	—	-500	µA		4
	I_{OL1}	V_{DD}= 1.9 V, V_{OL}= 0.3 V		500	—	—			
DC-OUT output current	I_{OH2}	V_{DD}= 1.9 V, V_{OH}= 1.6 V		—	—	-1000	µA		4
	I_{OL2}	V_{DD}= 1.9 V, V_{OL}= 0.3 V		1000	—	—			
Output voltage	V_{OH}	I_{OH}=-50 µA , V_{DD}=3.0 V (*)		2.90	—	—	V		—
	V_{OL}	I_{OL}=50 µA, V_{DD}=3.0 V (*)		—	—	0.10			
Input voltage	V_{IH}	V_{DD}= 1.7~3.6 V		0.8×V_{DD}	—		V	②	—
	V_{IL}	V_{DD}= 1.7~3.6 V		—	—	0.2×V_{DD}			
Input current	V_{IN}	V_{IN}=V_{DD} or V_{SS}	No pull-up nor pull-down	—	—	±0.1	µA	③	—
Pull-up current	I_{R1}	V_{IL}=0 V (**)		-20	-10	-5	µA	④	—
	I_{R2}	V_{IH}=2.8 V (**)		-100	-50	-25			
Pull-down current	I_{R3}	V_{IH}=3.0 V (***)		20	10	5	µA		—
Power on capacitance	C_{PON}	External capacitance for power on clear		100	1000	10000	pF	—	—
$\overline{RST}$ pulse width	t_{RST}	Forcible signal input		10	—	—	µs	—	—
STOP pulse width	t_{STOP}			10	—	—	ms	—	
$\overline{SILENT}$ pulse width	t_{SLNT}			10	—	—	ms	—	—
$\overline{EOT}$, TFNC, TIN, $\overline{TCK}$ pulse width	t_{CHAT}	76kHz/32kHz		30/70	—	—	µs	—	—
Frequency to IC deviation	Δf/ΔIC			—	—	±50	ppm	—	5
Frequency to voltage deviation	Δf/ΔV			—	—	±8	ppm	—	6
Recommended equivalent resistance	CI			—	—	45	kΩ	—	—

* CLK-OUT, $\overline{ADDR\text{-}DET}$, $\overline{RX\text{-}CLK}$, RX-DATA, SY-VALID, BS1, BS2, $\overline{ROMCLK}$, ROM-CE, ROM-RST

** $\overline{BLD}$, TFNC, $\overline{EOT}$, $\overline{STOP}$, $\overline{SILENT}$, $\overline{RST}$, $\overline{TST1}$, $\overline{TIN}$, $\overline{TCK}$

*** ROM-CE

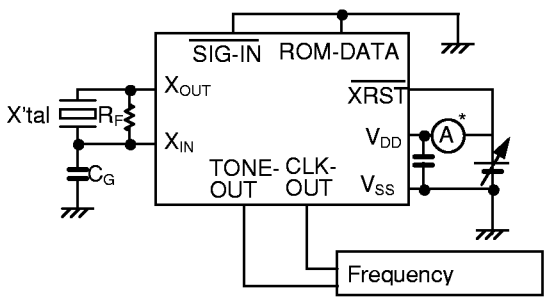
Notes:

1. Power supply voltage during frequency output from TONE-OUT is stable when $\overline{TCK}$=low. A capacitor of 0.2 µF or more must be connected between V_{DD} and V_{SS}.
2. Voltage where 32 KHz or 76 KHz from CLK-OUT pin can be counted within 10 seconds after power on.
3. Pull-up current is excluded. Measured under the condition that $\overline{SIG\text{-}IN}$ and ROM-DATA are connected to VSS, $\overline{XRST}$ to VDD, other pins are open and the oscillation circuit operates.
4. Current flowing into the IC is defined to be positive.
5. $$\Delta f/\Delta IC = \frac{f(V_{DD}=3.0\ V) - f_0}{f_0} \times 10^6\ (ppm)$$ f_0: Average frequency when V_{DD} is 3.0 V
6. $$\Delta f/\Delta V = \frac{f_1(V_{DD}=3.0\ V) - f_2(V_{DD}=2.9\ V)}{f_1(V_{DD}=3.0\ V)} \times 10^6\ (ppm)$$
7. When a trimmer capacitor is used, it should be inserted in CG side.
8. Recommended external parts

Crystal (C_L=12pF)	R_F	C_G
Seiko Instruments Inc. DS-VT-200 (32768 Hz)	10 MΩ	24 pF
Seiko Instruments Inc. DS-VTC-200 (76800 Hz)	10 MΩ	24 pF

■ Test Circuits

①

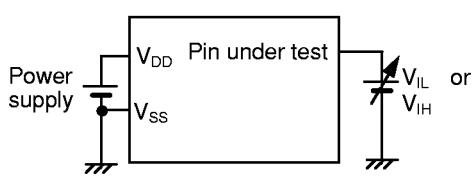


External crystal

Crystal	R_F	C_G
32768 Hz	10 MΩ	24 pF
76800 Hz	10 MΩ	24 pF

Parameter	Measuring method
Current consumption	Connects $\overline{\text{SIG-IN}}$ and ROM-DATA to V_{SS}, $\overline{\text{XRST}}$ to VDD and sets other pins open. Inserts an ammeter to the position shown by *.
Oscillation start voltage	Connect a frequency counter to the CLKOUT pin.
Power supply voltage	Connect a frequency counter to the TONEOUT pin.

②



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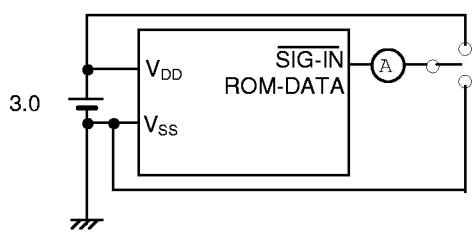

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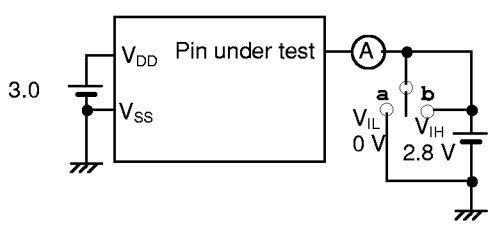


Switch **a** when I_{R1} is measured.
Switch **b** when I_{R2} is measured.

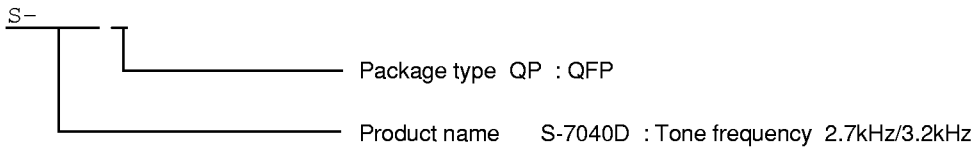
Figure 4

■ Absolute Maximum Ratings

Table 3

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{DD}	-0.3 to 5.0	V
Input voltage	V_{IN}	V_{SS}-0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	V_{SS} to V_{DD}	V
Storage temperature	T_{stg}	-40 to +125	°C
Operating temperature	T_{opr}	-10 to +70	°C

■ Ordering Information



■ POCSAG Signal Code Format

Transmission format of POCSAG signal code conforms with CCIR recommendation 584 which is shown in Figure 5. Transmission unit of a POCSAG signal is called block. A block comprises a preamble and one or more batches following the preamble.

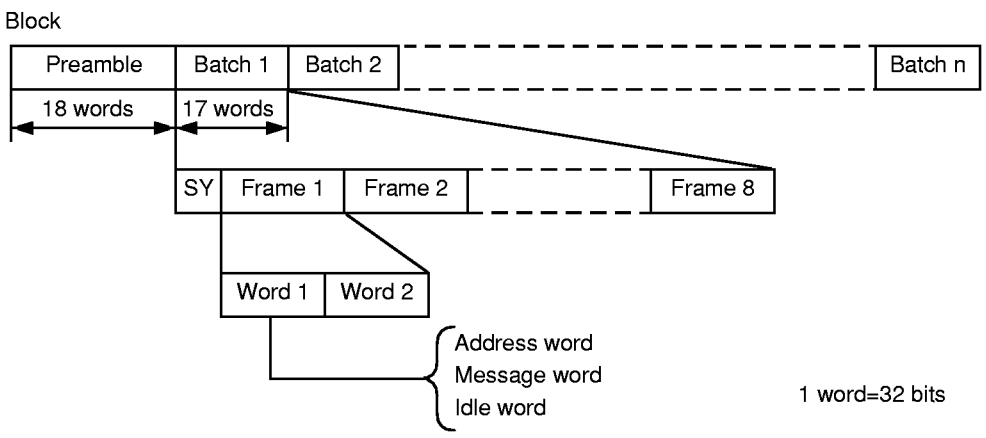
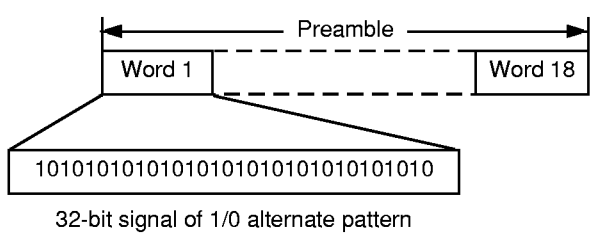


Figure 5 POCSAG code format

1. Preamble

   Preamble at the beginning of a block gives notice that a POCSAG signal is sent to the S-7040D. A preamble consists of at least 576 bits (18 words) alternate signals of 1 and 0. Once preamble is received, the S-7040D starts synchronization between the internal circuit and the POCSAG signal.
   Acceptable duty ratio of preamble ranges from 25% to 75%.



32-bit signal of 1/0 alternate pattern

32 bits×18 words=576 bits

Figure 6 Preamble configuration

2. Batch

   A batch, which is transmitted just after a preamble, contains information in a POCSAG signal and consists of a synchronization code (SY) and eight frames.
   When the S-7040D recognizes preamble and SY as part of POCSAG signal, the decoder regards the following signal as POCSAG data and receives a frame. The S-7040D receives only a selected frame in a batch, frame whose number was assigned in ID-ROM in advance, and BS1 pin goes high only when a selected frame comes.

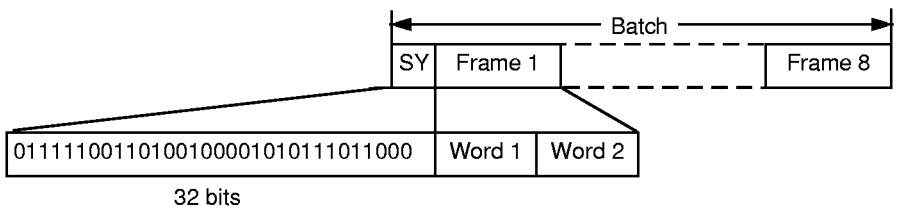


Figure 7 Batch configuration

Synchronization code (SY): 32-bit signal shown in Figure 7. When the SY is received after a preamble, the S-7040D considers them as a POCSAG code.

Frame: One frame consists of two words and a word consists of 32 bits. There are three types of words: address word, message word and idle word.

3. Word types
Three types of words are used as shown in Figure 8.

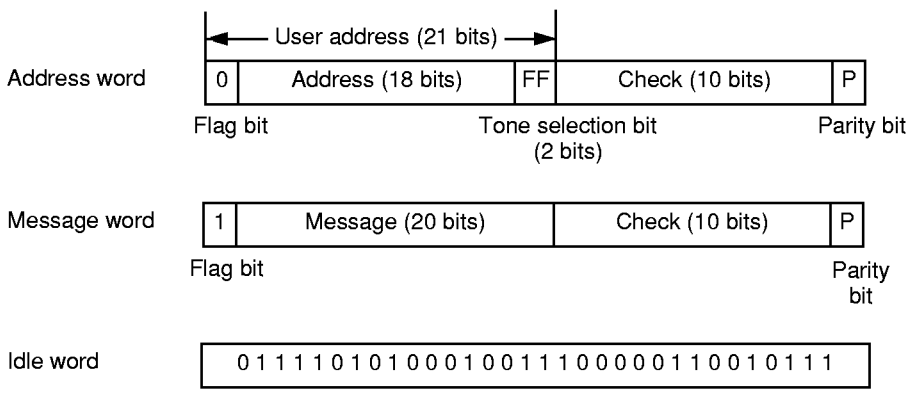


Figure 8 Kinds of words

The address word is sent first, then message word(s) follows in case of a display pager. Two or more message words can be sent continuously. (Tone-only pagers need no messages; idle words are used instead.) A flag bit determines whether the word is an address word or a message word. 0 shows an address word, and 1 shows a message word. The actual information is the address and tone selection bits (FF) in an address word and the message in a message word.

Address word: Each pager is distinguished by the data. An address should always be sent prior to information. Of the 21 bits in a user address, 18 bits are used for the actual address. Two tone selection bits select the calling tone (see "■ Basic Operation 6.1 Tone"). Check bits perform BCH check (see "Internal Functions 3. BCH decode function").

Message word: Of the 32 bits in a message word, 20 bits are used for the actual message. Even if a message is long enough to exceed a batch, subsequent message words are also received in the next batch until an address word is detected when a flag bit becomes 0. Thus plural message words can be sent continuously. A synchronization code (SY) must be inserted to continue message from frame 8 (last frame of a batch) to the next batch. The S-7040D gives the content of these message words to a CPU.

Idle word: If a batch does not have any information to send, idle words fill the blank portion of the batch. The Idle word cannot be assigned as an ID code.

■ Flow Chart

Flow charts for POCSAG signal process are shown in figures 9 and 10. These flow charts show the operations from power on to signal output for tone-only pager and display pager respectively.

1. Tone-only pager

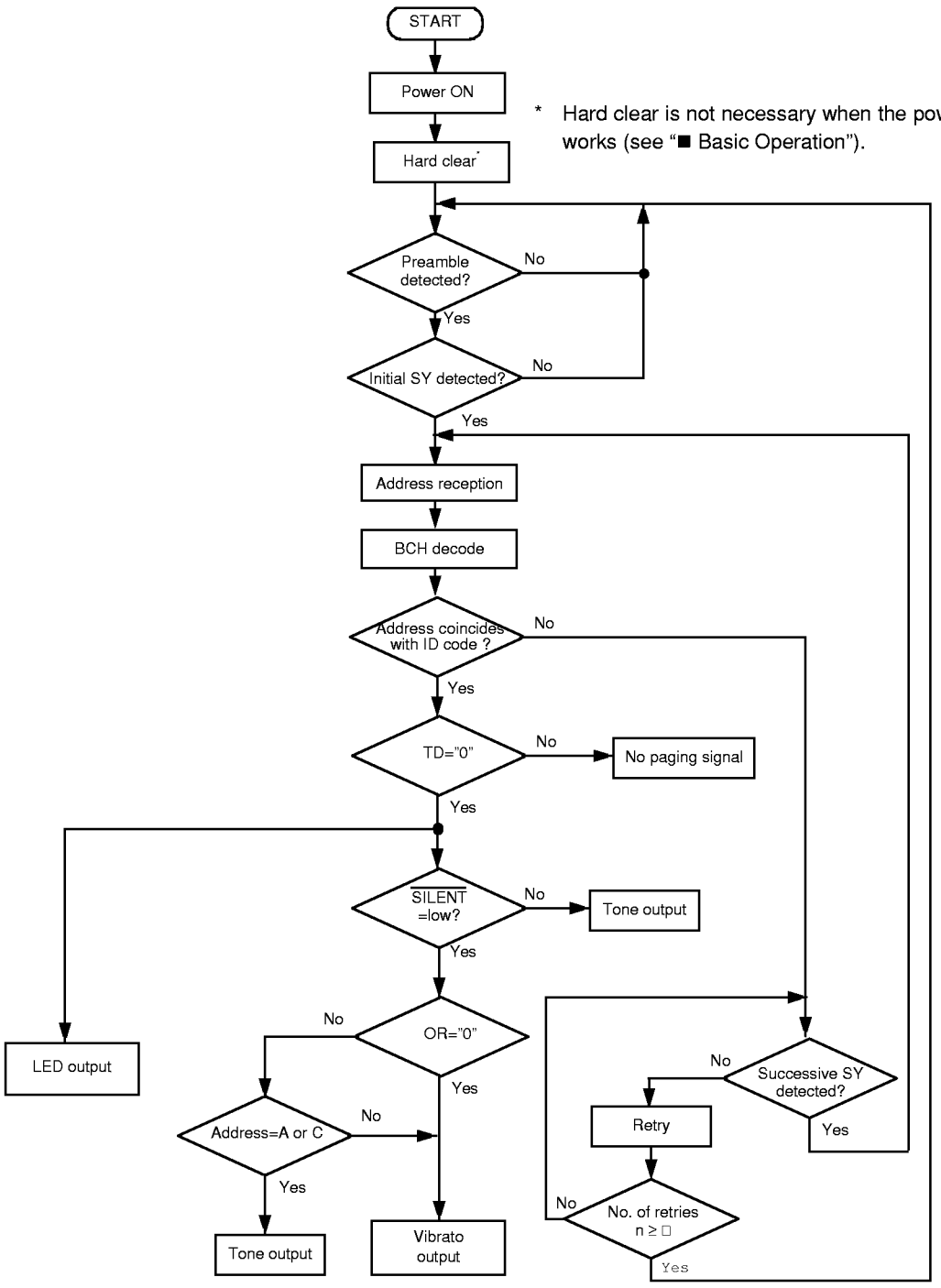


Figure 9

2. Display pager

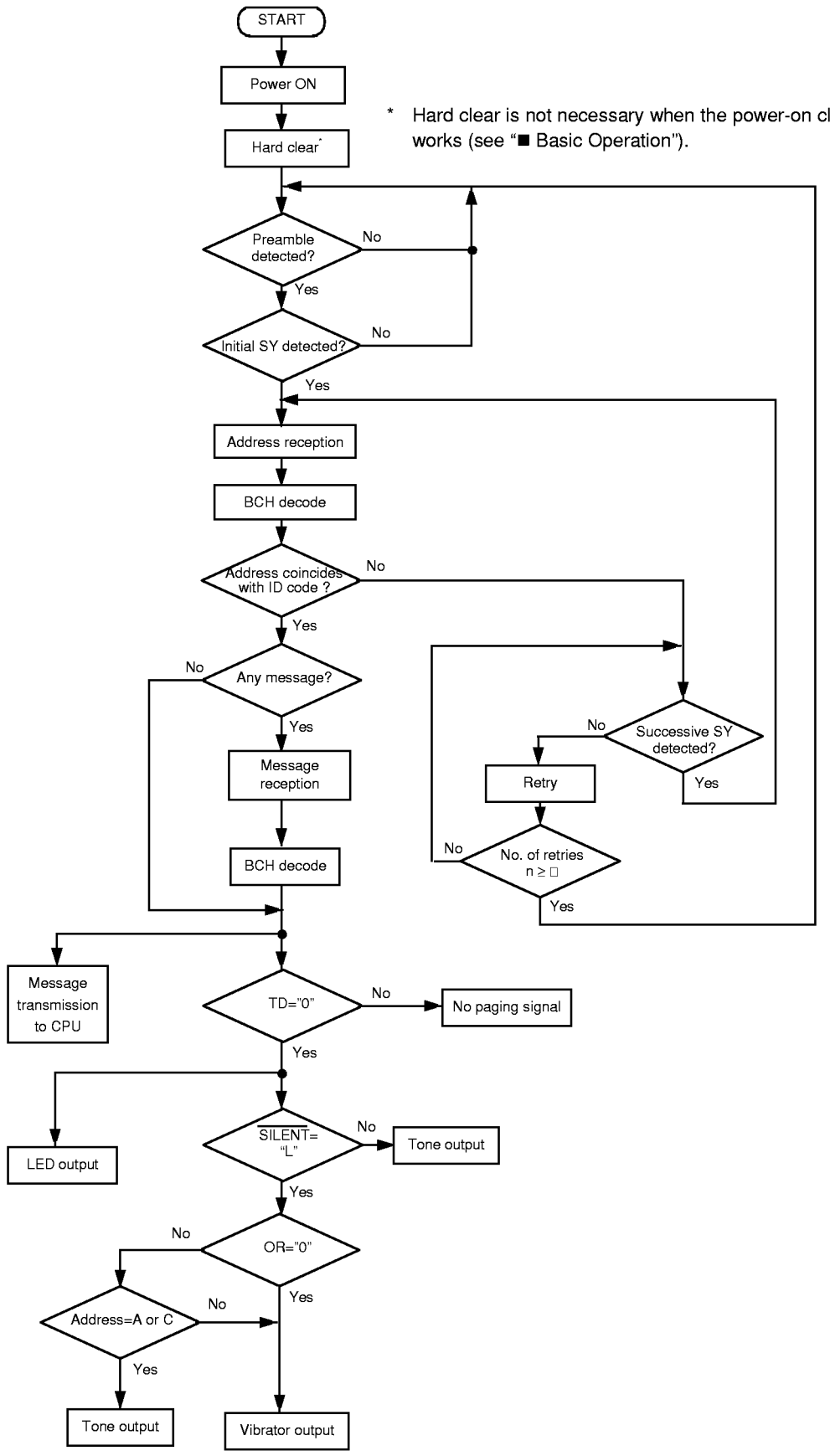


Figure 10

■ Basic Operation

1. Hard clear
   The internal circuit is initialized by setting the $\overline{RST}$ pin to low. Then ID-ROM data are fetched in the S-7040D 500msec after the rising edge of reset signal. The initial tone is transmitted immediately after ID-ROM read (see "6.1 Tone"). The initial tone stops automatically after two seconds. POCSAG signal can be received 1sec (512bps) or 426msec (1200bps) after ID-ROM read.
   The internal circuit is automatically initialized at power on when a capacitor whose capacitance is 100pF to 0.01ƒÊF is connected between $\overline{RST}$ pin and V_{SS} pin.

2. Detection of preamble
   Preamble detection mode starts when the hard clear is completed or when the synchronization code is not detected even if the detection is repeated over the defined number of retries. When the decoder receives 12 consecutive bits consisting of an alternate pattern of 1, 0, 1, 0 in this mode, it regards the signal as preamble.
   The S-7040D drives the RF circuit intermittently to save power consumption. When BS1 pin is high, the RF power is turned on to detect preamble. When the BS1 pin is low, preamble is not detected. Once preamble is detected, the BS1 pin holds high to detect synchronization code(SY). Figure 11 shows the BS1 timing and preamble.

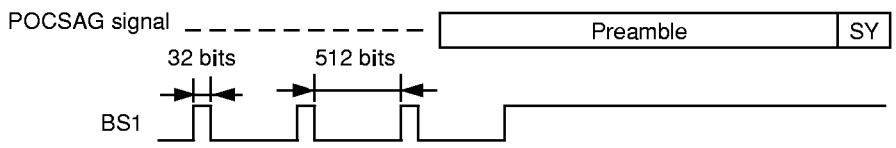


Figure 11 BS1 Timing and preamble

3. Detection of synchronization code(SY)
   After detecting preamble, the S-7040D enters synchronization code(SY) detection mode. The first SY detected after the preamble is called the initial SY. When another batch continues, an SY is inserted between the batches and the SY is called successive SY.

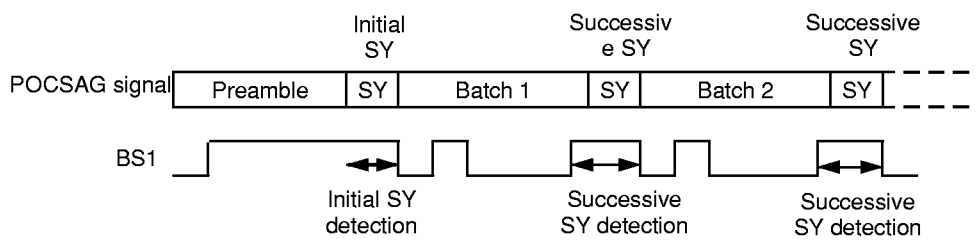


Figure 12 Initial SY and successive SY

3.1 Initial SY detection mode
Detection of the initial SY following preamble is performed during initial SY detection mode. The S-7040D compares the received data with the SY data kept in the S-7040D (see Fig.7). Receiving one bit of data the S-7040D compares the 32-bit data including this bit and those 31 bits received before it with the defined SY. If 30 or more bits coincide, the SY is considered to be detected. Even if the radio wave is disturbed by noise, SY can be detected as long as the number of fault bits is less than 2.
If SY is not detected after comparing 49 words (about 1.5K bits) in initial SY detection mode, the S-7040D returns to the preamble detection mode.

3.2 Successive SY detection mode

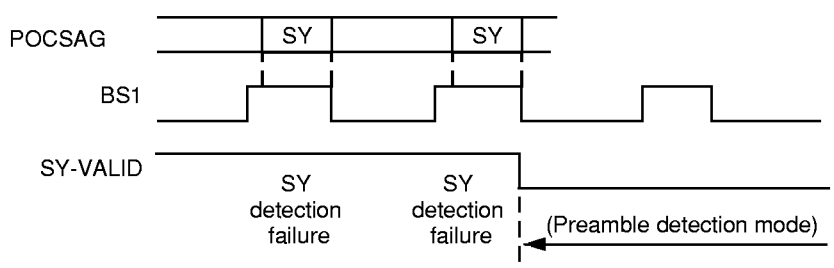
After the initial SY, successive SY is sent at the head of each batch. After the time for 8-frame (16-word) data, the S-7040D enters automatically successive SY detection mode. Since the signal is already synchronized, BS1 goes high in time with 32-bit output for successive SY and the S-7040D compares SY. In the same way as in initial SY detection mode, SY is detected even if the data contains up to two fault bits.
When SY is detected, the bit/word counter is reset and processing of data in the next batch follows.
When SY is not detected, the S-7040D retries SY detection for the number of times specified in ID-ROM plus one. When the S-7040D fails to detect SY during these retires, it returns to preamble detection mode.
When the S-29131A is used for ID-ROM, bits R3 to R0 specifies the number for retry (see (see "■ Circuit Design 1. Interface to ID-ROM" for bit configuration of ID-ROM).

Table 4 Setup of the number for retry

R3	R2	R1	R0	The number of retries
0	0	0	0	1
1	0	0	0	9
1	1	1	1	16

If data is found to have consecutive 12-bit alternate pattern such as 1, 0, 1, 0 during the final retry, the S-7040D regards it as a preamble and enters the initial SY detection mode (see Figure 13).

(1) Case in which the S-7040D detects no SY and returns to the preamble detection mode



(2) Case in which the S-7040D detects preamble in the final retry

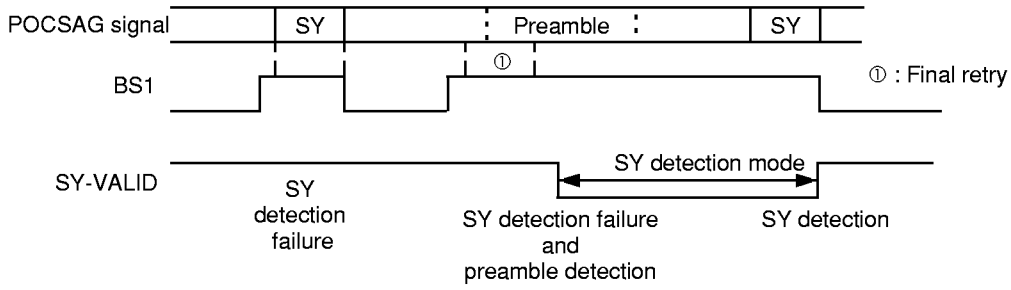


Figure 13 Operation for successive SY detection failure

4. Address detection
After finishing the SY detection, the S-7040D receives its own assigned frame. An address word is placed at the beginning of the frame. As shown in Figure 14 the latter 11 bits of the address word are check bits, and are used for error detection using BCH code (see (see "■ Internal Functions 3. BCH decode function"). The S-7040D compares the none erroneous address word with the fore addresses written in ID-ROM, and if they coincide, then receives a message word. Erroneous address words are ignored. If plural addresses are received at the same time, address A has priority over address B and address C has priority over address D. Only preferred address is received.

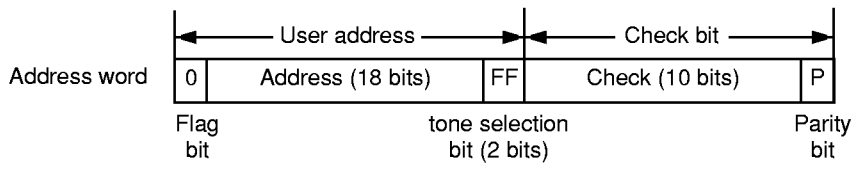


Figure 14 Address word configuration

5. Message detection
When an address word is detected, a message word is subsequently received. The S-7040D sends the message word to CPU, and the message is then sent to the pager display. The decoder continues to detect message words until an address or an idle word is detected.
As shown in figure 15, the latter 11 bits of the message word are check bits, and are used for error detection with BCH decode (see "■ Internal Functions 3. BCH decode function"). If an error is found, the message word is sent to CPU with error information (see table 5 "Error processing").

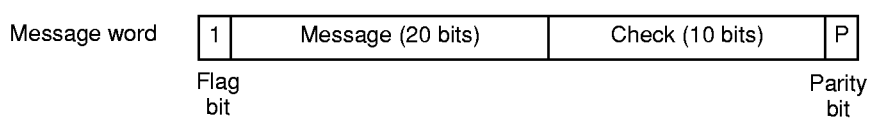


Figure 15 Message word configuration

When the S-7040D detects SY between message words, the following message is sent to the CPU again after SY is detected. If synchronization is failed at SY detection, message detection is terminated and ADDR-DET returns high.

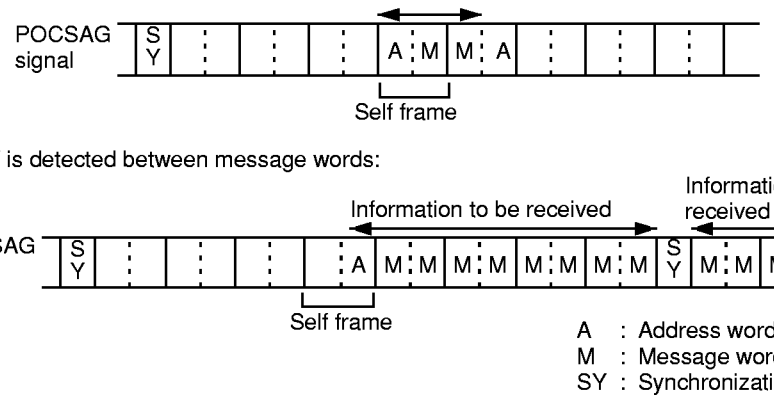


Figure 16 Information to be received

6. Paging signal
When the S-7040D detects an address (receives a call), not only by sending a message to a CPU but also by tone, light and vibration it notifies that the wearer is paged. 3 pins, TONE-OUT, DC-OUT (vibrator output) and LED, are assigned for paging signals. These signals are also transmitted at supply voltage lowering and after initialization. When the ID-ROM "TD" bit is set "1", no paging signal is transmitted.

6.1 Tone

Tone signal is transmitted from TONE-OUT pin at the end of pager initialization, address detection and supply voltage lowering respectively.

Completion of initialization:

A tone is transmitted just after ID-ROM read following power-on clear or hard clear. This is called the initial tone and lasts 2 seconds at 2.7kHz single tone. Setting the $\overline{\text{STOP}}$ pin to low makes the initial tone stop. Setting the $\overline{\text{SILENT}}$ pin to low changes tone output to vibrator output.

Address reception:

When address reception is completed, a tone is transmitted for 20 seconds. The waveform varies with contents of the tone selection bits. The transmission starts when the received data output is finished and 125msec after returning of the $\overline{\text{ADDR-DET}}$ pin to "H". The tone stops by setting $\overline{\text{STOP}}$ pin to low for longer than 10msec. 4 types of tone are assigned to each pair of addresses (A, C) and (B, D). When the decoder receives the next address during tone output, the tone output changes by the $\overline{\text{ADDR-DET}}$ timing.
The S-7040D has a single tone of 2.7kHz and a mixed tone of 2.7kHz and 3.2kHz. ID-ROM TM bit decides which pair of addresses single tone is assigned to (see "■ Circuit Design 1. Interface to ID-ROM").

Supply voltage lowering:

When $\overline{\text{BLD}}$ pin goes low due to power supply voltage drop, Two 2.7kHz single tone outputs are transmitted at intervals of 32 seconds. This is called "BLD tone". The tone continues until $\overline{\text{STOP}}$ pin is set low for longer than 5.3s at 512bps or 2.3s at 1200bps.

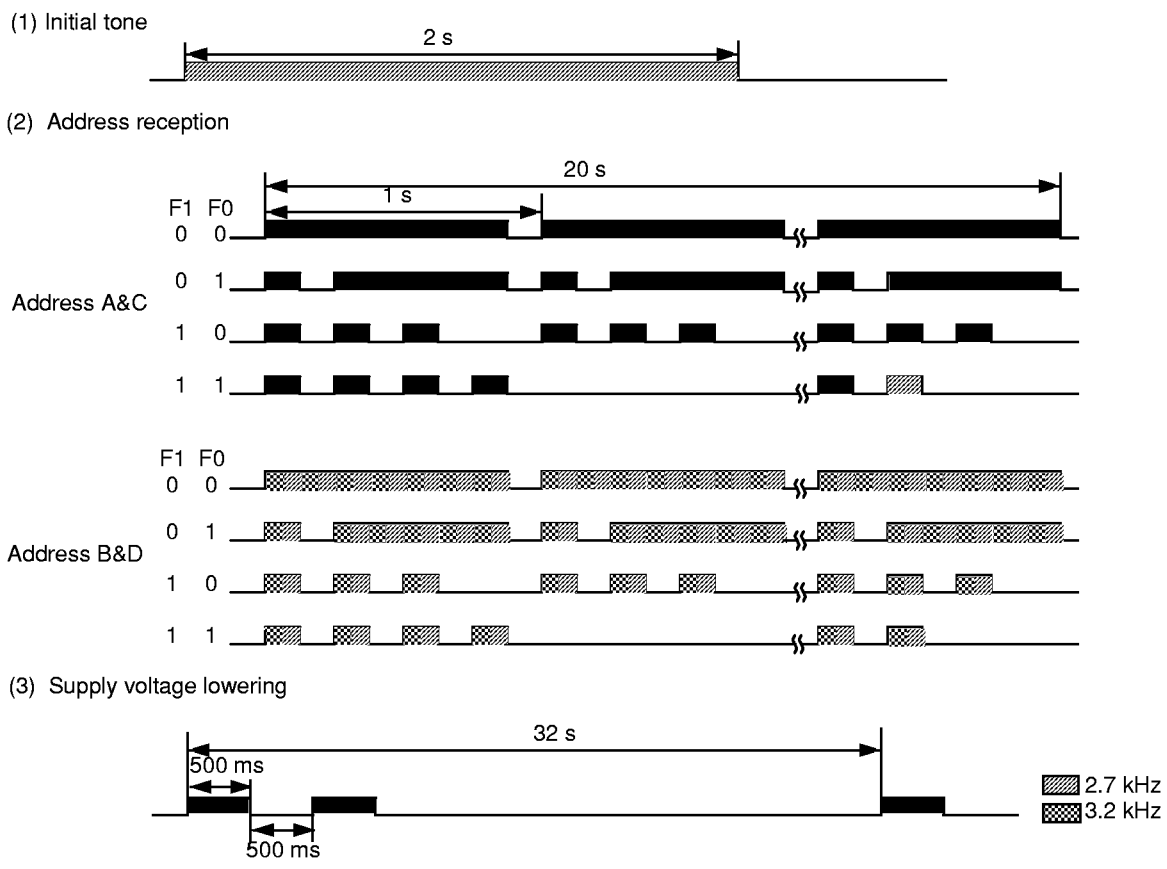


Figure 17 TONE-OUT output form