

- Quad 3.125 Gbps per Channel Transceiver Providing 20 Gbps Full Duplex Data Throughput
- Low Power Consumption 500 mW/Channel at 3.125 Gbps
- Selectable Synchronized or Independent Channel Operation
- Support Transmit Only, Receiver Only, Transceiver and Repeater Functions in a Single Chip Through Configuration Pins
- Selectable on Chip 8-Bit/10-Bit (8B/10B) Encoding/Decoding (ENDEC)
- Supports IEEE 802.3ae Proposed XGMII Parallel Interface
- Supports IEEE 802.3ae Proposed XAUI Serial Interface
- Receiver Differential Input Thresholds 200 mV
- Advanced 0.25- $\mu$ m CMOS Technology
- On-Chip 50- $\Omega$  Serial Receiver Termination
- No External Filter Capacitors Required
- LVPECL Compatible Differential Signaling Serial Interface
- Stub Series Terminated Logic for 2.5-V (SSTL\_2) I/O
- Able to Operate With a Single 2.5-V Power Supply
- On-Chip Pseudorandom Bit Stream (PRBS) Generation and Verification for Self Test
- IEEE 802.3 Management Data Interface (MDIO)
- IEEE 1149.1 JTAG Test Interface
- Hot Plug Protection
- Low Cost 289 Ball PBGA Package

## description

The TLK3104SA is a flexible four channel serial backplane transceiver, delivering high-speed bidirectional point-to-point data transmissions to provide up to 20 Gbps of full duplex data transmission capacity. The TLK3104SA supports a broad operating range of serial data rates from 2.5 Gbps to 3.125 Gbps. The primary application of this device is to provide building blocks for developing point-to-point baseband data transmission over controlled impedance media of approximately 50  $\Omega$ . The transmission media can be printed-circuit board traces, copper cables or fiber-optical media. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The TLK3104SA performs the parallel-to-serial, serial-to-parallel conversion, and clock extraction functions for a 10 gigabit ethernet physical layer interface. The TLK3104SA also provides a selectable 8-bit/10-bit (8b/10b) encode/decode function. The serial transmitter and receiver use differential low voltage pseudo-emitter controlled logic (LVPECL) compatible signaling.

The four transceivers in the TLK3104SA can be configured as either four separate links, or synchronized together as a single data path. The TLK3104SA supports both the 36-bit bidirectional 10-Gigabit media independent interface (XGMII) and the extended auxiliary unit interface (XAUI) currently in draft stage within IEEE 802.3ae 10-Gigabit ethernet task force.

The TLK3104SA supports the IEEE 802.3 defined management interface (MDIO) to allow ease in configuration and status monitoring of the link.

The TLK3104SA supports the IEEE 1149.1 defined JTAG test port for ease in board manufacturing test as well as a comprehensive series of built-in tests for self-test purposes including internal serial loopback and PRBS generation and verification.

The TLK3104SA operates with a single 2.5 V supply and dissipates less than 2.6 watts. The device is packaged in a 19  $\times$  19 mm, 289 pin plastic ball grid array (PBGA) package and is characterized for operation from 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2000, Texas Instruments Incorporated

**PRODUCT PREVIEW**

# TLK3104SA

## QUAD 3.125 Gbps SERIAL TRANSCEIVER

SCAS651 – AUGUST 2000

---

### description (continued)

The TLK3404SA is a member of the transceiver family of CMOS multigigabit transceivers, intended for use in high-speed bidirectional point-to-point data transmission systems. Other members of the transceivers family include:

- TLK2201 – A second generation single channel Gigabit ethernet 802.3 compliant SERDES with both ten bit interface (TBI) and a reduced five pin double data rate (DDR) interface, packaged in a 64-pin VQFP PowerPAD™ package.
- TLK1501 – A 0.6-Gbps to 1.6-Gbps transceiver with on chip 8-bit/10-bit ENDEC providing up to 1.28 Gbps of data bandwidth, packaged in a 64-pin VQFP PowerPAD™ package.
- TLK2500/TLK2501 – A 1.6-Gbps to 2.5-Gbps transceiver with on chip 8-bit/10-bit ENDEC providing up to 2 Gbps of data bandwidth, packaged in a 64-pin VQFP PowerPAD™ package.
- TLK2701 – A 2.5 Gbps to 2.7 Gbps transceiver with on-chip 8-bit/10-bit ENDEC, providing up to 2.16 Gbps of data bandwidth with k-character control, packaged in a 64-pin VQFP PowerPAD™ package.
- TLK3101 – A 2.5-Gbps to 3.125-Gbps transceiver with on chip 8-bit/10-bit ENDEC, providing up to 2.5 Gbps of data bandwidth, packaged in a 64-pin VQFP PowerPAD™ package.
- TLK3104SC – A 3-Gbps to 3.125-Gbps quad transceiver with on chip 8-bit/10-bit ENDEC, a 16-bit low voltage differential signaling (LVDS) operating at 622 Mbps parallel interface, packaged in 289 pin PBGA.

PRODUCT PREVIEW

PowerPAD is a trademark of Texas Instruments.

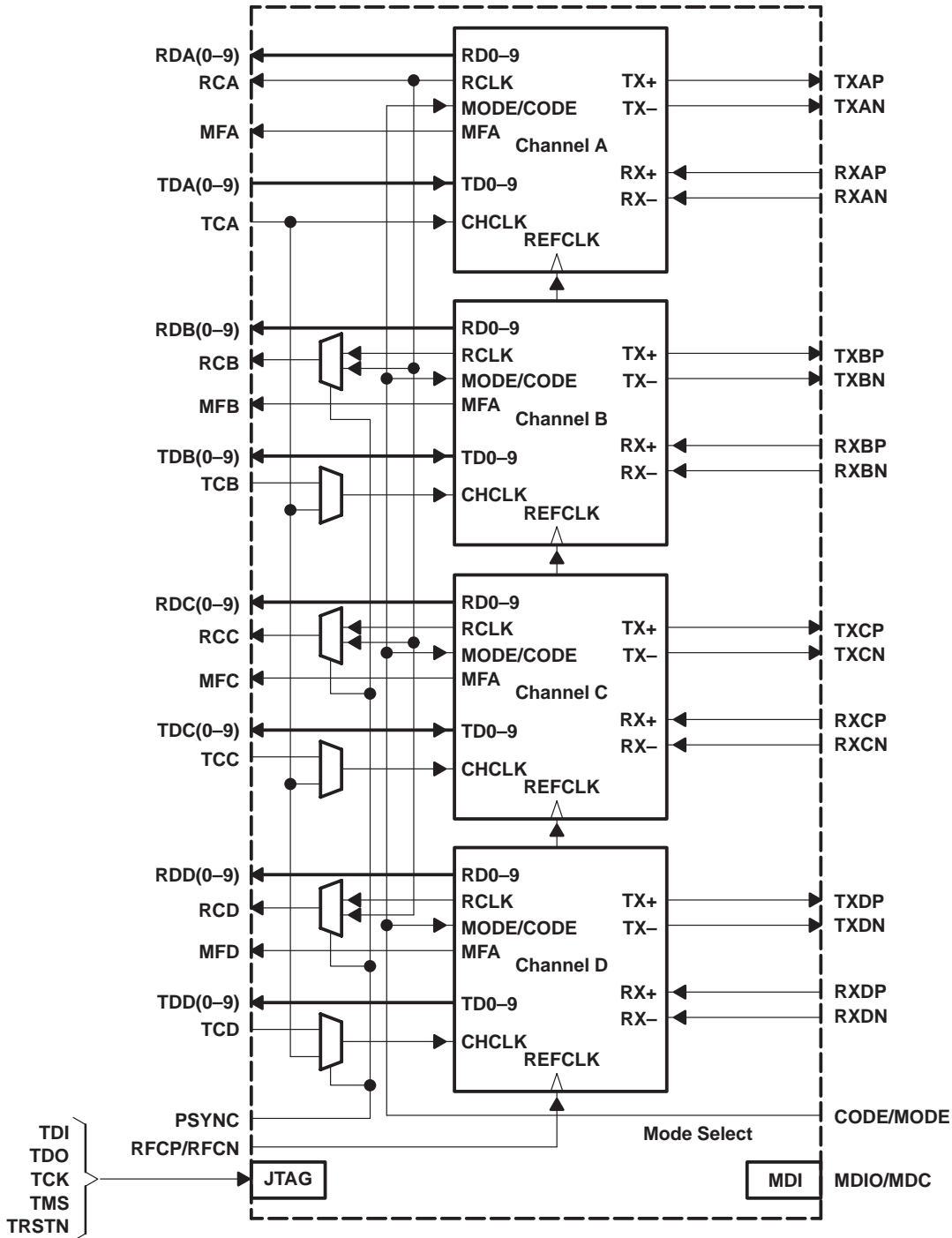
---



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

block diagram

The following block diagram provides a high level description of the TLK3104SA. For a detailed diagram of the individual channels, see Figure 1.



PRODUCT PREVIEW

# TLK3104SA QUAD 3.125 Gbps SERIAL TRANSCEIVER

SCAS651 – AUGUST 2000

The following is a more detailed block diagram description of each channel core.

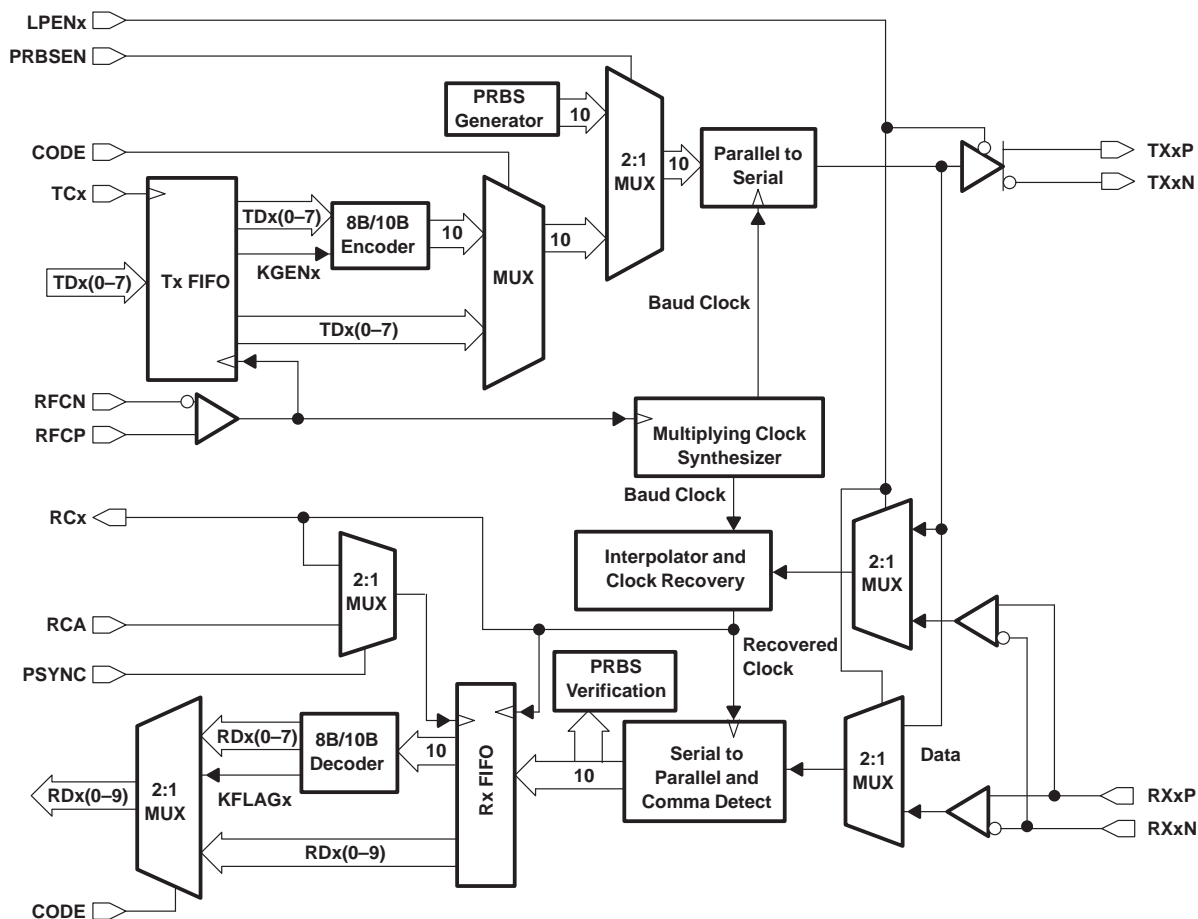


Figure 1. Block Diagram of Individual Channel

PRODUCT PREVIEW



## **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.