128K x 32 SRAM

SRAM MEMORY ARRAY

AVAILABLE AS MILITARY SPECIFICATIONS

- MIL-STD-883

FEATURES

- Fast Access Times of 10 to 25ns
- Overall Configuration: 128K x 32
- 4 Low Power CMOS 128K x 8 SRAMs in one MCM
- +3.3V power supply
- Internal Decoupling Capacitors
- Low Operating Power, 1/2 Previous Generation

OPTIONS — MARKINGS

• Operating Temperature Ranges	
Military (-55°C to +125°C)	XT
Industrial (-40°C to +85°C)	IT
• Timing	
10ns (Contact Factory)	-10
12ns	-12
15ns	-15
17ns	-17
20ns	-20
25ns	-25
• Package	
Ceramic Quad Flatpack	Q
Pin Grid Array	P
• Low Power Data Retention Mode	L

GENERAL DESCRIPTION

The Austin Semiconductor, Inc. AS8SLC128K32 is a high speed, 4MB CMOS SRAM multichip module (MCM) designed for full temperature range, 3.3V power supply, military, space, or high reliability mass memory and fast cache applications.

The device input and output TTL compatible. Writing is executed when the write enable (WE\) and chip enable (CS\) inputs are low. Reading is accomplished when WE\ is high and CS\ and output enable (OE\) are both low. Access time grades of 10ns, 12ns, 15ns, 17ns, 20ns and 25ns maximum are standard.

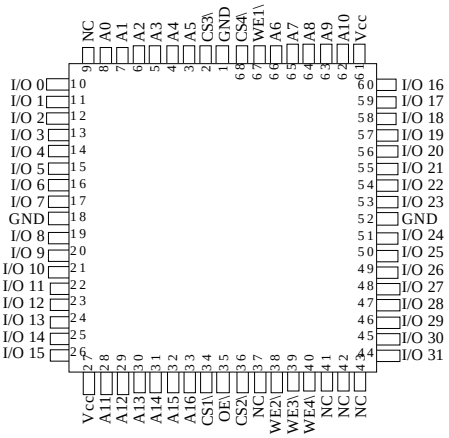
The products are designed for operation over the temperature range of -55°C to +125°C and screened under the full military environment.

For more products and information
please visit our web site at
www.austinsemiconductor.com

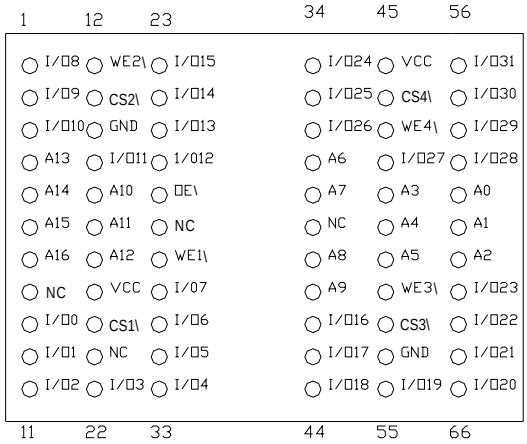
PIN ASSIGNMENT

(Top View)

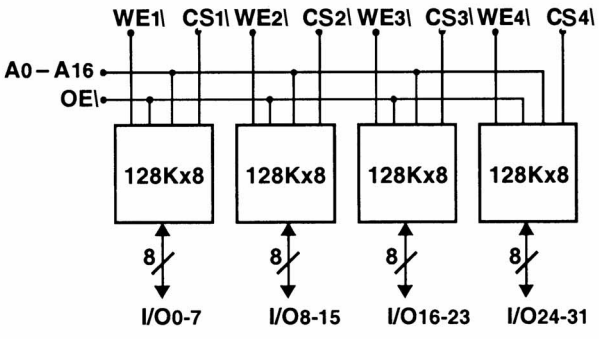
68 Lead CQFP (Q)



66 Lead PGA (P)



FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Voltage of Vcc Supply Relative to Vss.....-0.5V to +4.6V
Storage Temperature.....-65°C to +150°C
Short Circuit Output Current(per I/O).....20mA
Voltage on Any Pin Relative to Vss.....-.5V to Vcc+4.6V
Maximum Junction Temperature**.....+150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation on the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See the Application Information section at the end of this datasheet for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-55^oC \leq T_A \leq 125^oC$ and -40^oC to $+85^oC$; Vcc = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (logic 1) Voltage		V_{IH}	2.2	V_{CC}+0.3	V	1
Input Low (logic 1) Voltage		V_{IL}	-0.3	0.8	V	1
Input Leakage Current$_{ADD,OE}$	0V<V_{IN}<V_{CC}	I_{LI1}	-10	10	µA	
Input Leakage Current$_{WE,CE}$		I_{LI2}	-10	10	µA	
Output Leakage Current$_{I/O}$	Output(s) Disabled 0V<V_{OUT}<V_{CC}	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH}=-4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL}=8.0mA	V_{OL}		0.5	V	1

			MAX						
DESCRIPTION	CONDITIONS	SYMBOL	-10	-12	-15	-17	-20	UNITS	NOTES
High Speed Power Supply Current: Operating	CS\<V_{IL}; V_{CC} = MAX f = MAX = 1/ t_{RC} (MIN) Outputs Open, OE\ = V_{IH}	I_{CC1}	280	240	220	180	160	mA	2, 3,13
	Low Power (L)		240	210	200	180	160		
Low Speed Power Supply Current: Operating	CS\<V_{IL}; V_{CC} = MAX f = 1 MHz, OE\ = V_{IH}	I_{CC3}	---	---	---	---	---	mA	2
	Low Power (L)		80	60	60	60	60		
Power Supply Current: Standby	CS\>V_{IH}; V_{CC} = MAX f = MAX = 1/ t_{RC} (MIN) Outputs Open, OE\=V_{IH}	I_{SBT1}	100	80	80	80	80	mA	3, 13
	Low Power (L)		80	60	60	60	60		
CMOS Standby	V_{IN} = V_{CC} - 0.2V, or V_{SS} +0.2V V_{CC}=Max; f = 0Hz	I_{SBT2}	70	60	60	60	60	mA	
	Low Power (L)		50	36	36	36	36		

CAPACITANCE (V_{IN} = 0V, f = 1MHz, T_A = 25°C)*

SYMBOL	PARAMETER	MAX	UNITS
C_{ADD}	A0 - A16 Capacitance	40	pF
C_{OE}	OE\ Capacitance	40	pF
$C_{WE,}$ C_{CS}	WEx\ and CSx\ Capacitance	12	pF
C_{IO}	I/O 0- I/O 31 Capacitance	15	pF

NOTE:
*This parameter is sampled.

AC TEST CONDITIONS

TEST SPECIFICATIONS

Input pulse levels.....Vss to 3V
Input rise and fall times.....1ns/V
Input timing reference levels.....1.5V
Output reference levels.....1.5V
Output load.....See Figure 1, 2

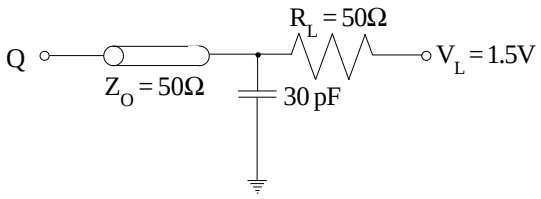


FIGURE 1

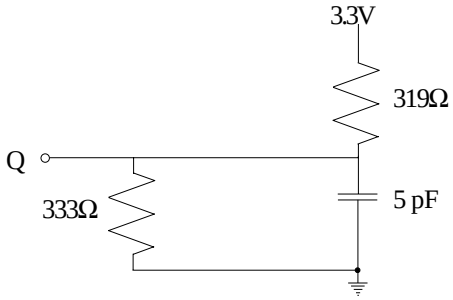


FIGURE 2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

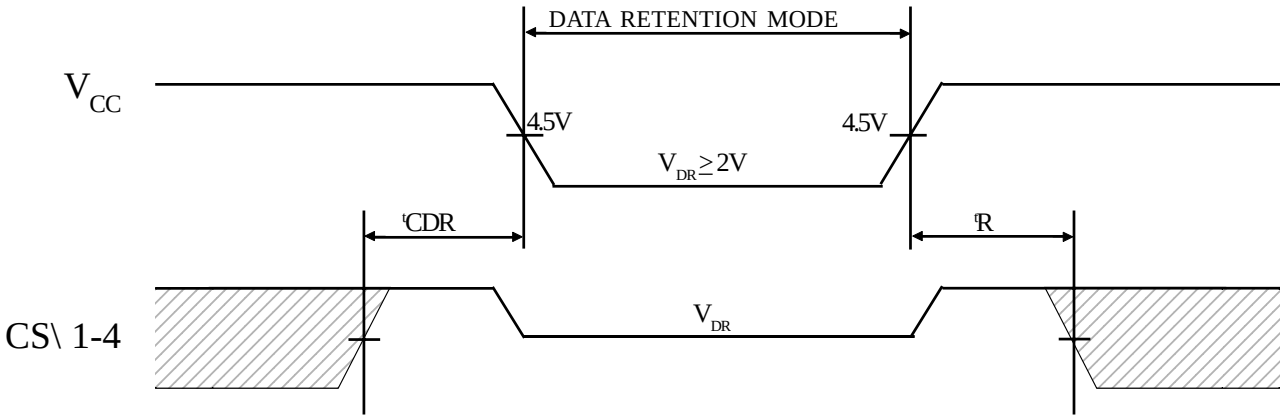
(NOTE 5) (-55°C≤T_A≤ 125°C and -40°C to +85°C; V_{CC} = 3.3V ±0.3V)

DESCRIPTION	SYMBOL	-10		-12		-15		-17		-20		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ CYCLE													
READ cycle time	^tRC	10		12		15		17		20		ns	
Address access time	^tAA		10		12		15		17		20	ns	
Chip select access time	^tACS		10		12		15		17		20	ns	
Output hold from address change	^tOH	1		2		2		2		2		ns	
Chip select to output in Low-Z	^tLZCS	1		2		2		2		2		ns	4,6,7
Chip select to output in High-Z	^tHZCS		5.5		6		7		7.5		8	ns	4,6,7
Output enable access time	^tAOE	0	5.5	0	6	0	7		7.5	0	8	ns	
Output enable to output in Low-Z	^tLZOE	0		0		0		0		0		ns	4,6
Output disable to output in High-Z	^tHZOE		5.5		6		7		7.5		8	ns	4,6
WRITE CYCLE													
WRITE cycle time	^tWC	10		12		15		17		20		ns	
Chip select to end of write	^tCW	9		10		10		11		12		ns	
Address valid to end of write	^tAW	9		10		10		11		12		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		ns	
WRITE pulse width, CS\ controlled	$^tWP1$	9		10		12		14		15		ns	
WRITE pulse width, WE\ controlled	$^tWP2$	9		10		12		14		15		ns	
Data setup time	^tDS	5		6		7		7.5		8		ns	
Data hold time	^tDH	1		1		1		1		1		ns	
Write disable to output in Low-z	^tLZWE	2		2		2		2		2		ns	4,6,7
Write enable to output in High-Z	^tHZWE	5		5		6		6.5		7		ns	4,6,7

LOW POWER CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} for Retention Data			V_{DR}	2		V	
Data Retention Current	All Inputs @ Vcc ± 0.2V or Vss ± 0.2V, CS\ = Vcc ± 0.2V	V_{CC} = 2V	I_{CCDR}		24	mA	
		V_{CC} = 3V	I_{CCDR}		32	mA	
Chip Deselect to Data Retention Time			t_{CDR}	0		ns	4
Operation Recovery Time			t_R	20		ms	4, 11

LOW V_{CC} DATA RETENTION WAVEFORM



NOTES

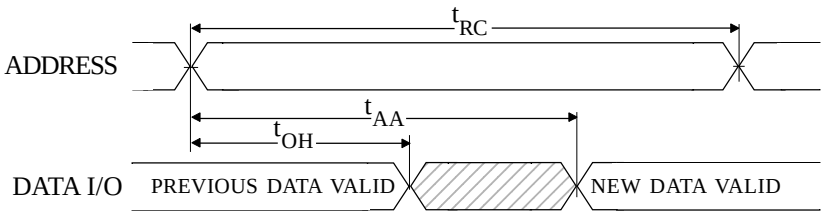
1. All voltages referenced to V_{SS} (GND).
2. Worst case address switching.
3. ICC is dependent on output loading and cycle rates.

$$\text{unloaded, and } f = \frac{1}{t_{RC(MIN)}} \text{ Hz.}$$

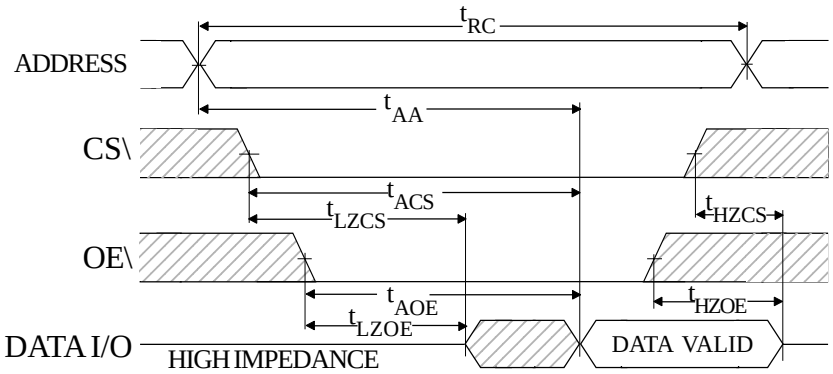
The specified value applies with the outputs

4. This parameter guaranteed but not tested.
5. Test conditions as specified with output loading as shown in Fig. 1 & 2 unless otherwise noted.
6. t_{HZCS}, t_{HZOE} and t_{HZWE} are specified with C_L = 5pF as in Fig. 2. Transition is measured +/- 200 mV typical from steady state voltage, allowing for actual tester RC time constant.
7. At any given temperature and voltage condition, t_{HZCS}, is less than t_{LZCS}, and t_{HZWE} is less than t_{LZWE}.
8. WE\ is HIGH for READ cycle.
9. Device is continuously selected. Chip selects and output enable are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. t_{RC} = READ cycle time.
12. Chip enable (CS\) and write enable (WE\) can initiate and terminate a WRITE cycle.
13. I_{CC} is for full 32 bit mode.

READ CYCLE NO. 1

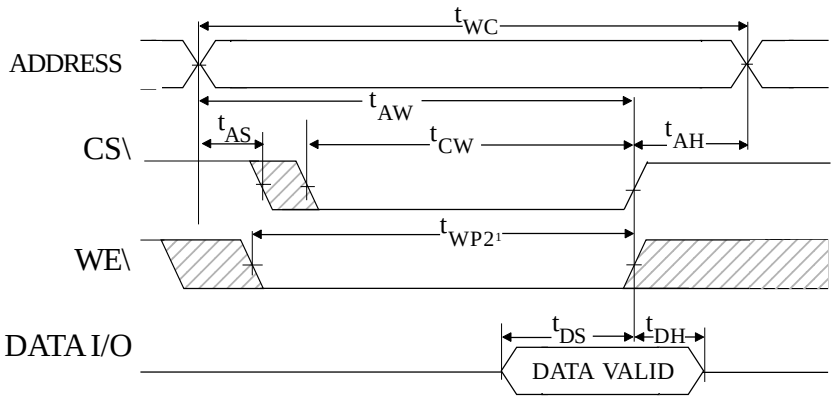


READ CYCLE NO. 2



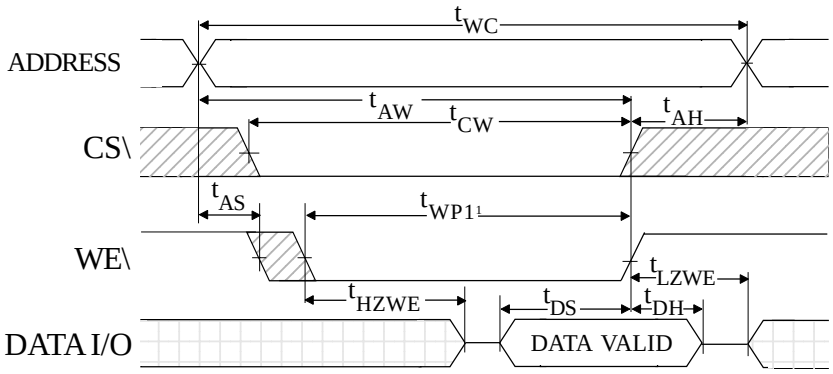
WRITE CYCLE NO. 1

(Chip Select Controlled)



WRITE CYCLE NO. 2

(Write Enable Controlled)

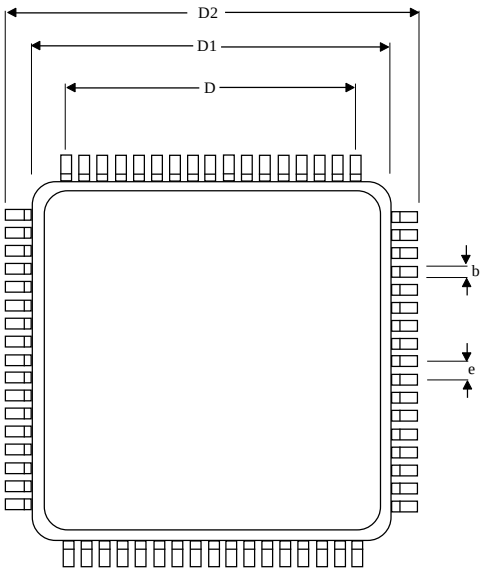


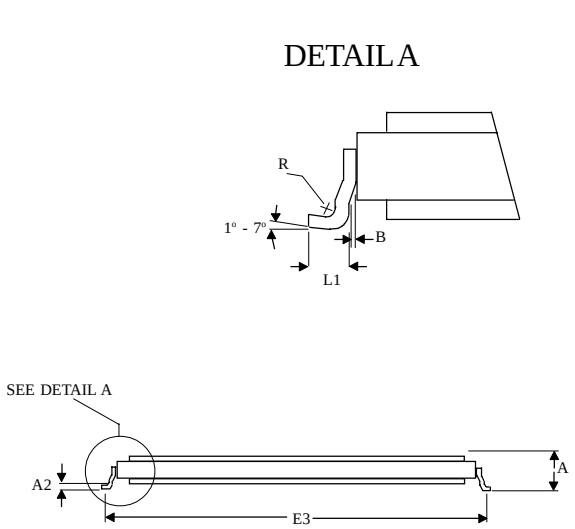
NOTES

1. All voltages referenced to V_{SS} (GND).

MECHANICAL DEFINITIONS*

ASI Case (Package Designator Q)



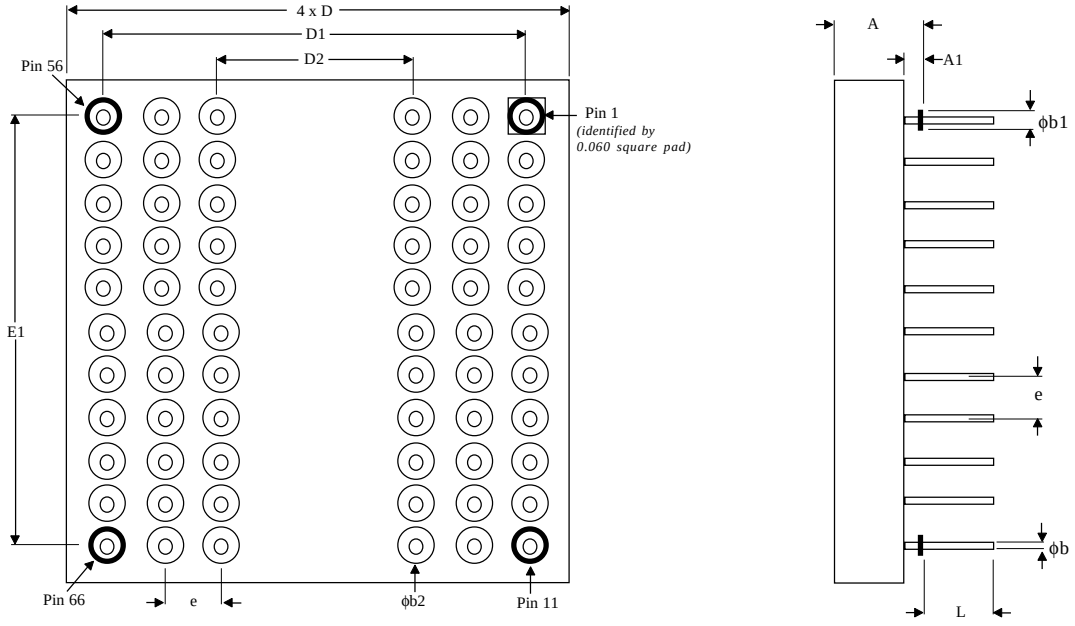


SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.123	0.200
A1	0.118	0.186
A2	0.005	0.015
B	0.010 REF	
b	0.013	0.017
D	0.800 BSC	
D1	0.870	0.890
D2	0.980	1.000
E	0.936	0.956
e	0.050 BSC	
R	0.010 TYP	
L1	0.035	0.045

All measurements are in inches.

MECHANICAL DEFINITIONS*

ASI Case (Package Designator P)



SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.135	0.195
A1	0.025	0.035
ϕb	0.016	0.020
ϕb1	0.045	0.055
ϕb2	0.065	0.075
D	1.064	1.086
D1/E1	1.000 BSC	
D2	0.600 BSC	
e	0.100 BSC	
L	0.145	0.155

All measurements are in inches.

ORDERING INFORMATION

EXAMPLE: AS8SLC128K32Q-20/883C

Device Number	Package Type	Speed ns	Options	Process
AS8SLC128K32	Q	-20	L	/*
AS8SLC128K32	Q	-25	L	/*
AS8SLC128K32	Q	-35	L	/*
AS8SLC128K32	Q	-45	L	/*
AS8SLC128K32	Q	-55	L	/*

EXAMPLE: AS8SLC128K32P-35L/IT

Device Number	Package Type	Speed ns	Options	Process
AS8SLC128K32	P	-20	L	/*
AS8SLC128K32	P	-25	L	/*
AS8SLC128K32	P	-35	L	/*
AS8SLC128K32	P	-45	L	/*
AS8SLC128K32	P	-55	L	/*

*AVAILABLE PROCESSES

XT = Military Temperature Rang -55°C to +125°C
IT = Industrial Temperature Range -40°C to +85°C
883C = Full Military Processing -55°C to +125°C

OPTION DEFINITIONS

L = 2V data retention/low power